READ2302G

High Drivability & High Slew Rate, Input Output Full Range, CMOS Dual Operational Amplifier

V_{IO}≤±6mV, SR=8V/μs, GBW=6MHz

R03DS0097EJ0200
Rev.2.00
Apr. 17, 2017

Description

The READ2302G is input and output full range dual CMOS Operational Amplifier realizing high drivability and high slew rate. This IC can be used in minimum operating supply voltage from 2.5V, and in wide ambient temperature range from -40ºC to +105ºC.

Available in ultra-small 8 pins TSSOP packages.

Features

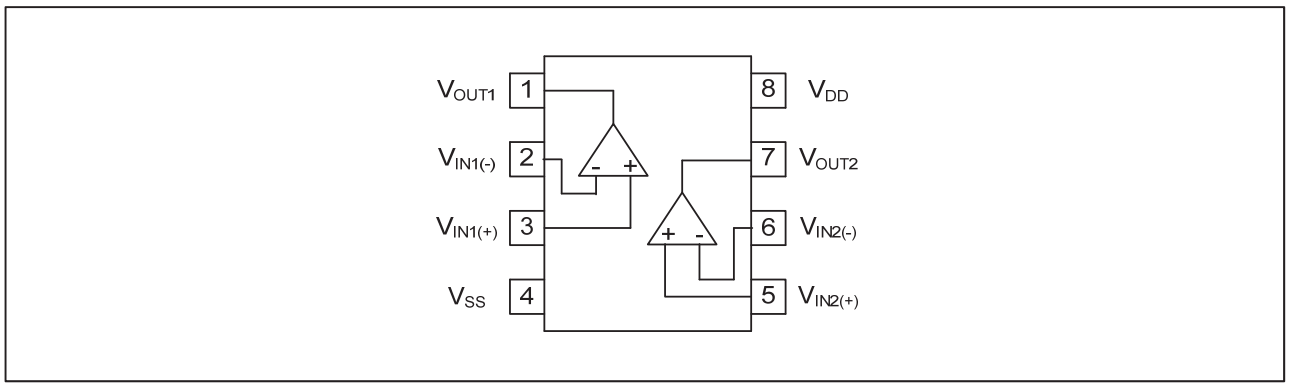
- Low voltage single supply operation — V_{DD} = 2.5V to 5.5V
- Low input offset voltage — V_{IO} ≤ ±6.0mV
- Low input bias current — I_B ≤ (1pA).
- Wide output voltage range — V_{OUT} : V_{SS}+0.1V to V_{DD}-0.1V(@Io=5mA)
- Supply current (per channel) — I_{DD} = 0.75mA Typ.
- High slew rate — SR = 8V/μs Typ.

( ) reference value of design

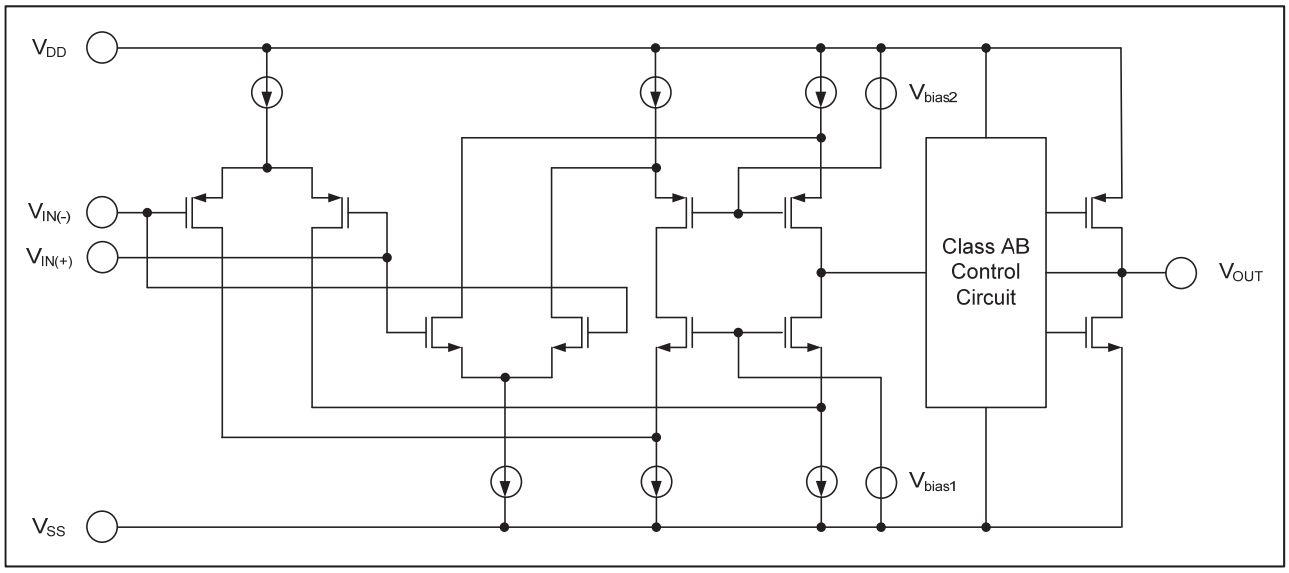
Product Line-up

Type name	Product type quality level	Package
READ2302GSP	High slew rate with Normal quality level	8 pins plastic TSSOP

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T_A=25 ºC >

Items	Symbol	Ratings	Unit
Supply voltage Note.1	V_{DD}	-0.3 to +6.5	V
Differential input voltage	V_{ID}	-V_{DD} to +V_{DD}	V
Input voltage Note.2	V_I	-0.3 to V_{DD} +0.3	V
Maximum output current	I_O	20	mA
Power dissipation Note.3	P_T	440	mW
Junction temperature	T_j	+150	ºC
Operating temp. range	T_A	-40 to +105	ºC
Storage temp. range	T_{stg}	-55 to +150	ºC

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm×100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern). Please take note that every package has derating rate's restriction reception.

Electrical Characteristics

<V_{DD}=5V, T_A=25 °C >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply voltage	V_{DD} - V_{SS}	2.5		5.5	V	
Input offset voltage	V_{IO}			±6.0	mV	
Input offset current	I_{IO}			(1)	pA	
Input bias current	I_B			(1)	pA	
Output high voltage	V_{OH}	V_{DD}-0.2			V	I_L = 10mA
Output low voltage	V_{OL}			V_{SS}+0.2	V	I_L = 10mA
Voltage gain	A_V	60	90		dB	R_L≥100kΩ
Channel supply current	I_{DD}/ch		0.75	1.5	mA	R_L=∞, I_O=0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V_{ICM}	V_{SS}		V_{DD}	V	
Gain bandwidth product	GBW		6		MHz	C_L=20pF
Slew rate	SR		8		V/μs	C_L=20pF

( ) reference value of design

Notes

Output terminal : The over-current protection feature is not built in the output terminal of this product.

Therefore, please insert resistance to output port.

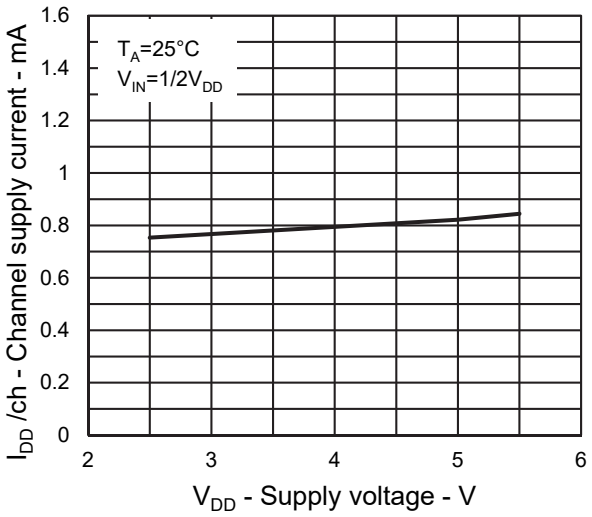
Input offset voltage : the amplifier circuit of the first block of operational amplifier.

A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply.

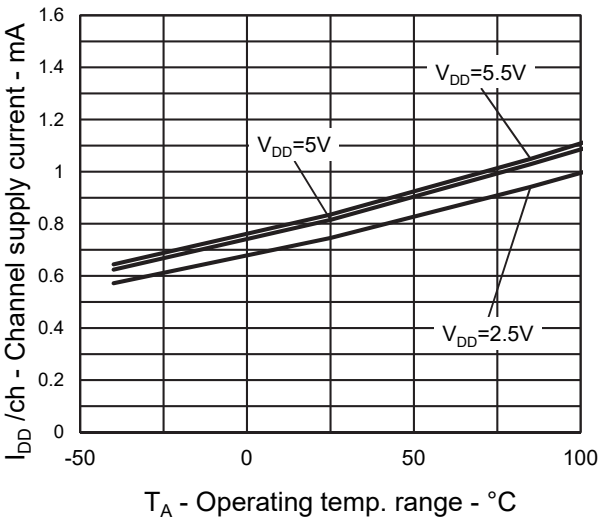
in case of input voltage of overlap point output port has a minute voltage shift or distortion.

Electrical Characteristics

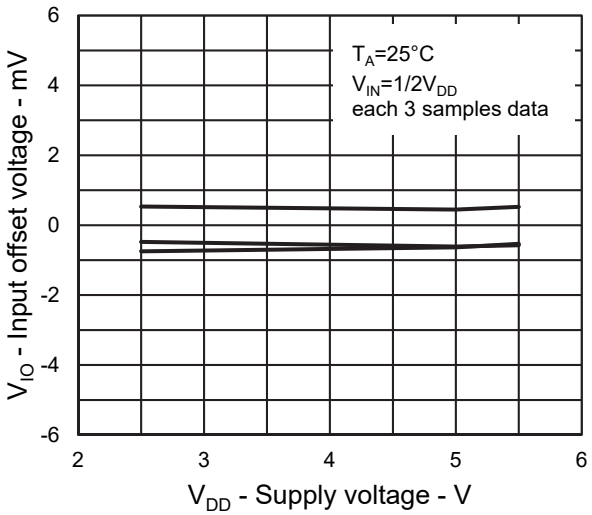
I_{DD} /ch vs. V_{DD}



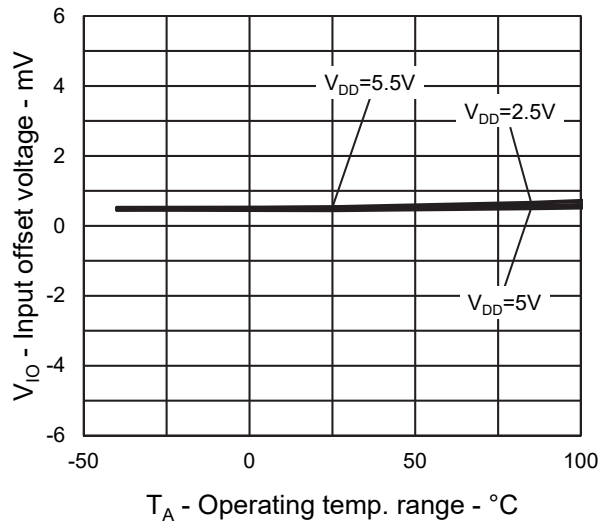
I_{DD} /ch vs. T_A



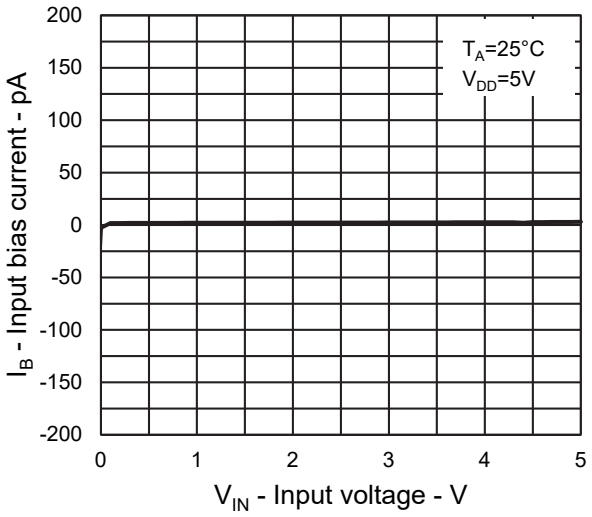
V_{IO} vs. V_{DD}



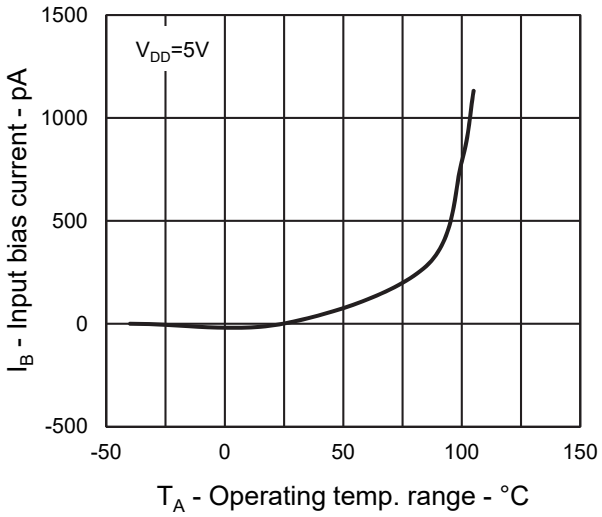
V_{IO} vs. T_A



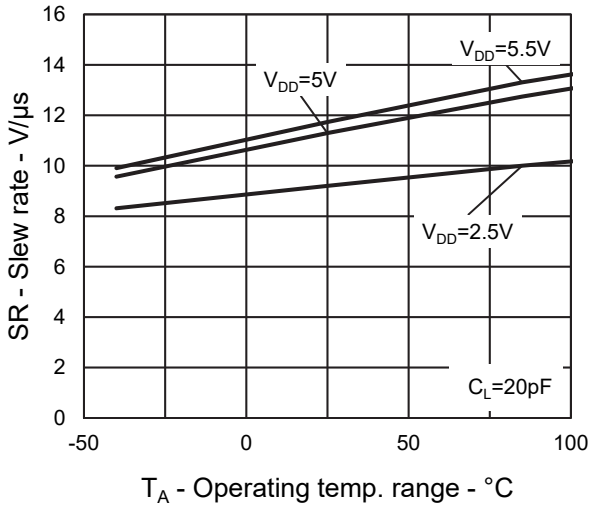
I_B vs. V_{IN}



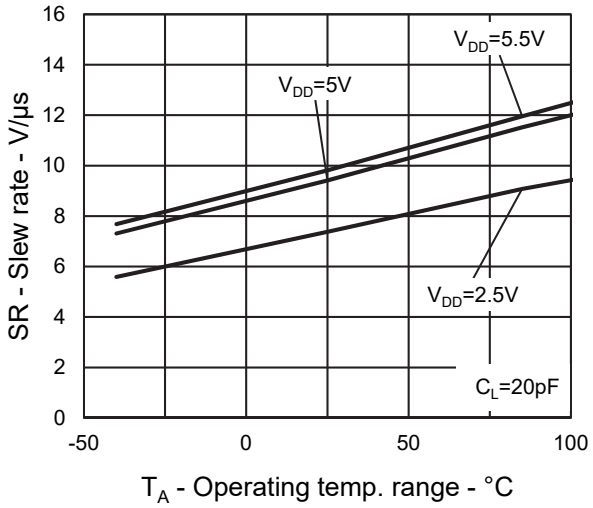
I_B vs. T_A



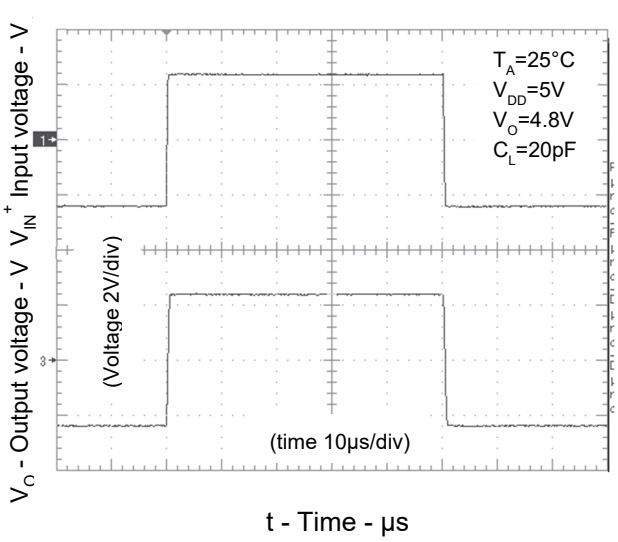
SR vs. T_A (Output rise time)



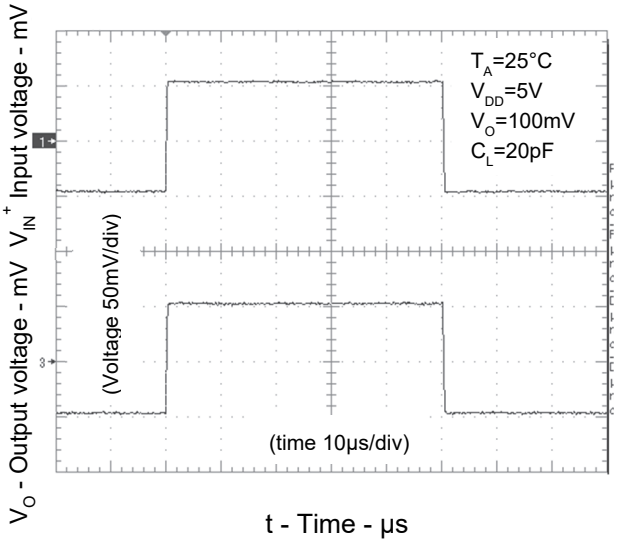
SR vs. T_A (Output fall time)



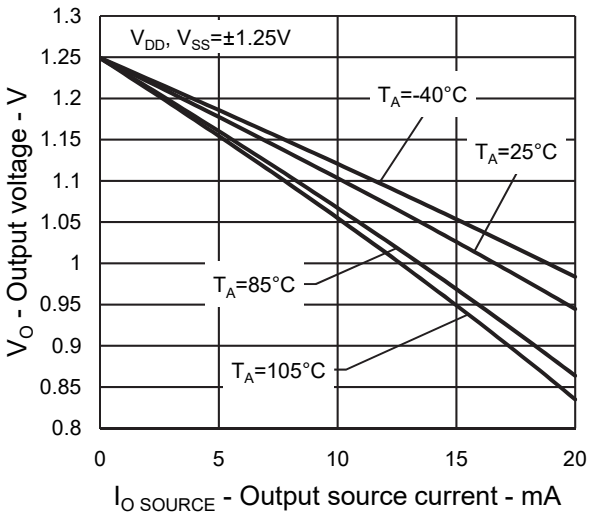
Pulse response



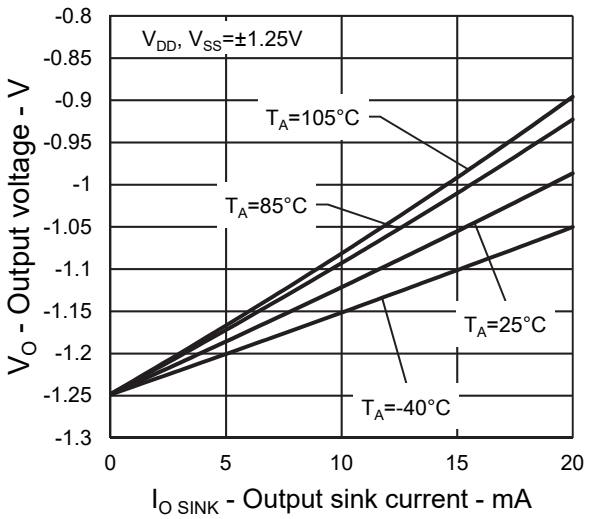
Pulse response



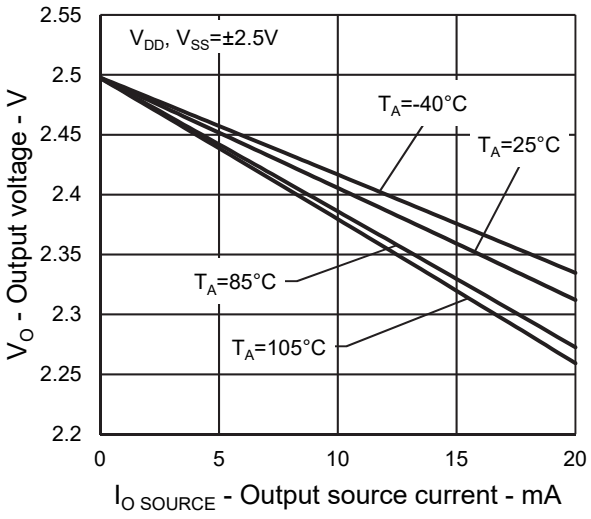
V_O vs. $I_{O\ SOURCE}$



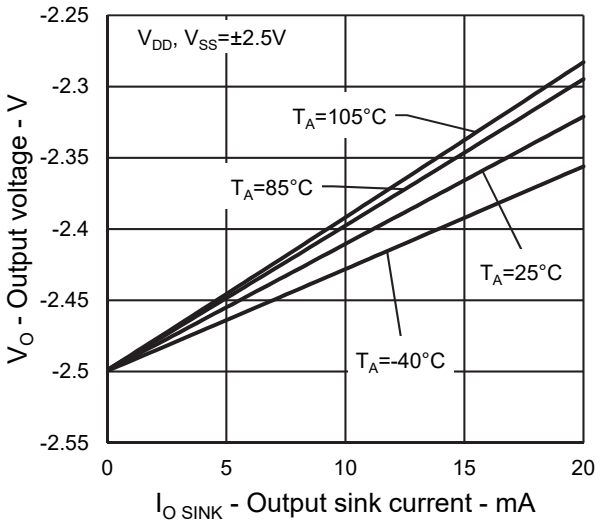
V_O vs. $I_{O\ SINK}$



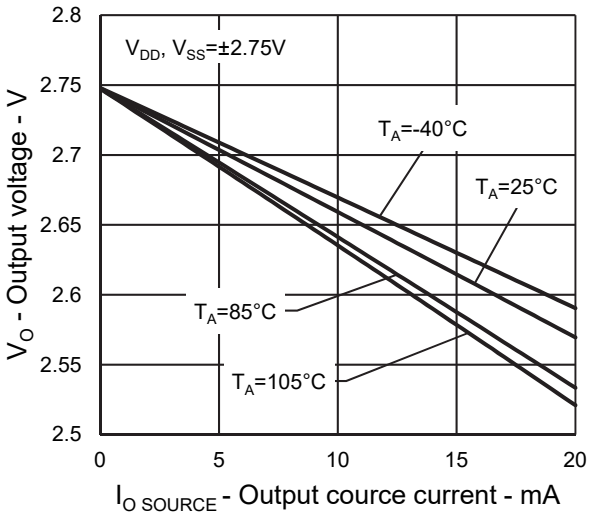
V_O vs. $I_{O\ SOURCE}$



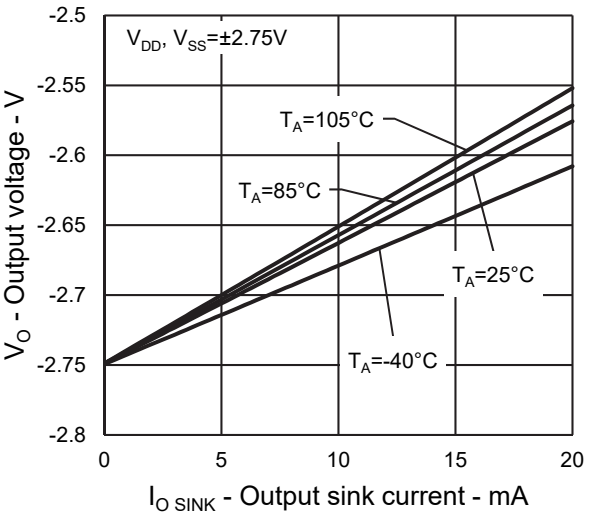
V_O vs. $I_{O\ SINK}$



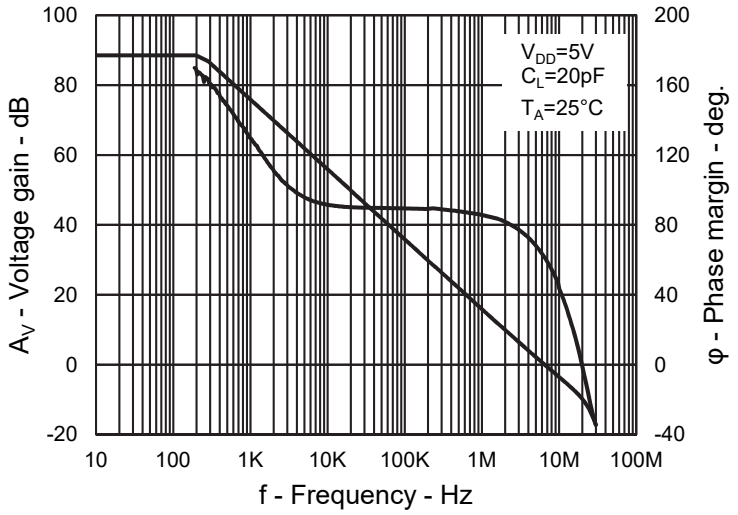
V_O vs. $I_{O\ SOURCE}$



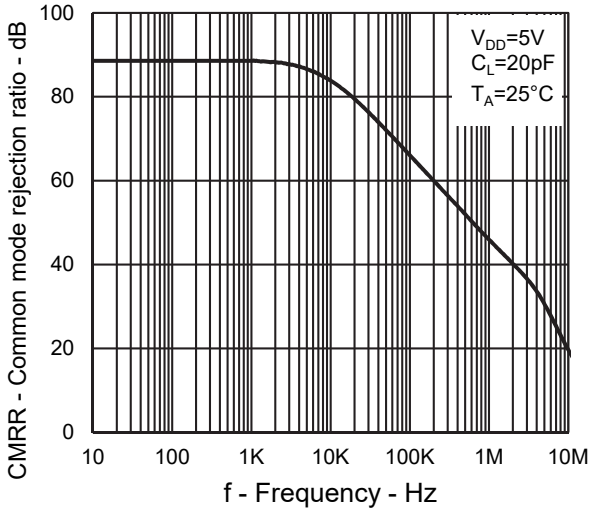
V_O vs. $I_{O\ SINK}$



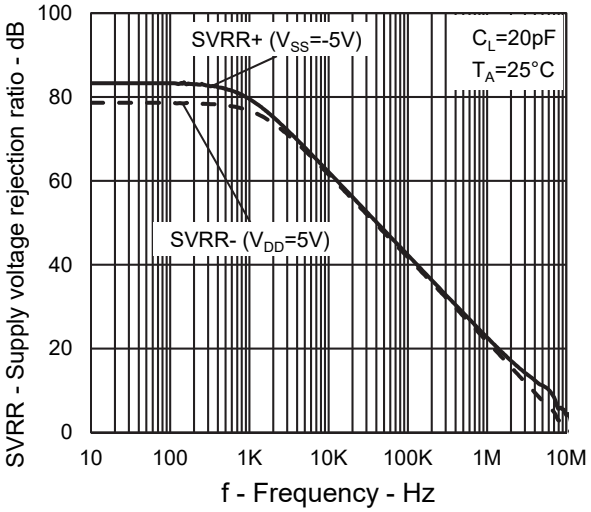
A_V, φ vs. f



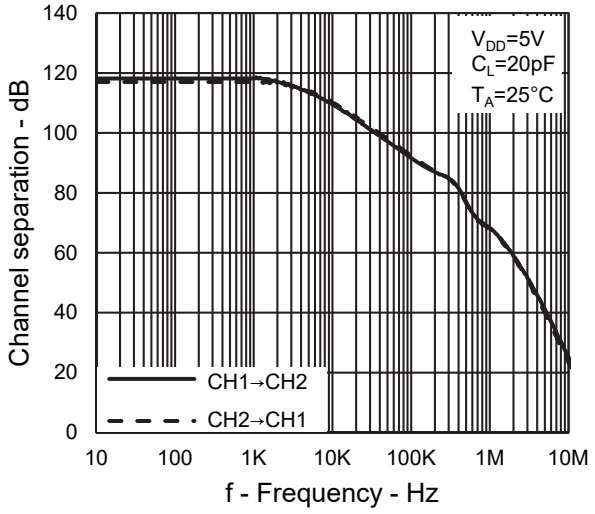
CMRR vs. f



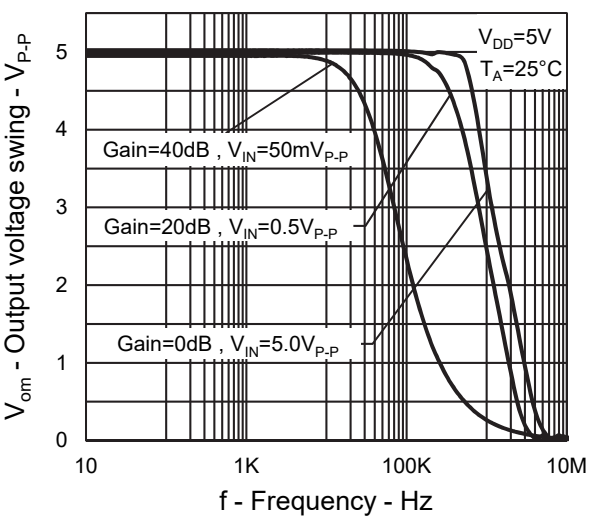
SVRR vs. f



Channel separation vs. f



V_{om} vs. f

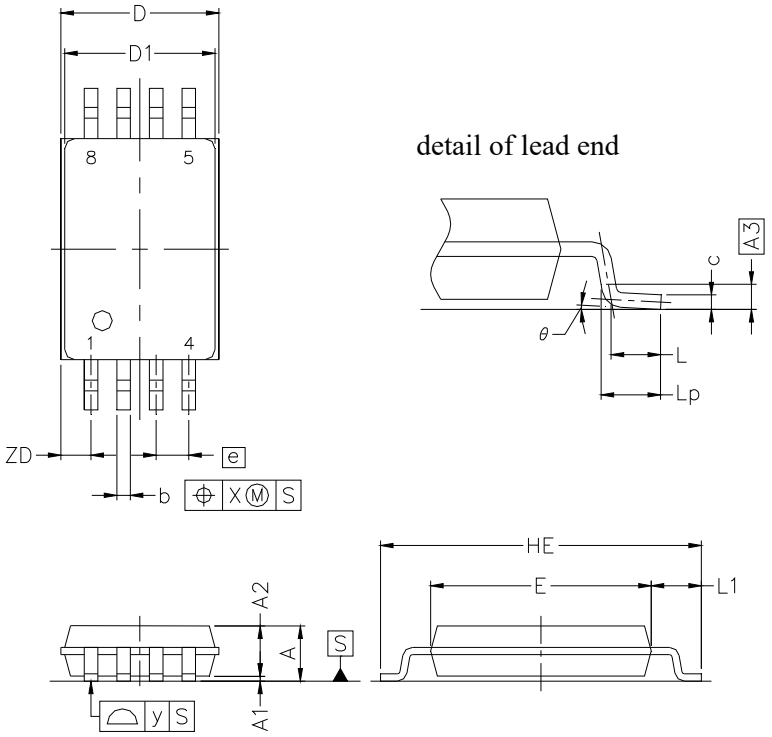


Package Dimensions

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	-

Unit:mm



ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 +0.06 -0.05
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
e	0.65
x	0.10
y	0.10
ZD	0.60

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

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9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将瑞萨电子产品或技术用于(1)与大规模杀伤性武器（例如核武器、化学武器、生物武器或运送此等武器的导弹，包括无人机(UAV)）的开发、设计、制造、使用、存储等相关的任何目的；(2)与常规武器的开发、设计、制造或使用相关的任何目的；(3)扰乱国际和平与安全的任何其他目的，并且不可向任何第三方销售、出口、租赁、转让、或让与瑞萨电子产品或技术，无论直接或间接知悉或者有理由知悉该第三方或任何其他方将从事上述活动。对瑞萨电子产品或技术进行出口、销售、转让 等时，必须遵守对于各方或交易主张司法管辖权的国家/地区政府公布和管理的任何适用出口管制法律法规。
10. 请知悉并同意，用户将承担由于不当使用或违反本文档（包括本注意事项）中所述条款与条件而导致的所有损失和损害，并且如果此等不当使用或违反是因为用户将瑞萨电子产品转售或提供给任何第三方使 用而致，则用户必须保证瑞萨电子不受损失。
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12. 如果对本文档所记载的信息或瑞萨电子产品有任何疑问，请向瑞萨电子的营业部门咨询。

（注1） 瑞萨电子：在本文档中指瑞萨电子株式会社及其控股子公司。
（注2） 瑞萨电子产品：指瑞萨电子开发或生产的任何产品。

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SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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