



Keywords: error amplifier compensation, active-clamp forward converter, peak-current-mode controller

APPLICATION NOTE 5780

Designing Active-Clamp Forward Converters Using Peak-Current-Mode Controllers

By: K S Bhanuprasad

© Aug 05, 2014, Maxim Integrated Products, Inc.

Abstract: Active-clamp forward converter design using MAX17598/MAX17599 is outlined. Design methodology and calculations for components value selection are presented.

Introduction

This application note describes the methodology of designing active-clamp forward converters using the [MAX17598/MAX17599](#) peak-current-mode controllers. This application note discusses both self driven and winding driven secondary synchronous MOSFETs in the active-clamp forward converter topology. Formulas for calculating component values and ratings are also presented.

In this application note, the following sections explain the design methodology of various components in the Active-Clamp Forward Converter topology.

1. Transformer Turns Ratio Selection
2. Output Inductor Selection
3. Primary Magnetizing Inductance Selection
4. Clamp Capacitor Selection
5. Input Capacitor Selection
 - a. Input Ceramic Capacitor Selection
 - b. Filter Capacitor Selection in AC-DC Applications
6. Primary n-MOSFET Selection
7. Current-Sense Resistor Selection
8. Primary p-MOSFET Selection
9. p-MOSFET Gate-Drive Circuit for Low-Side Active-Clamp Configuration
10. SLOPE Compensation
11. IN Supply Configuration
 - a. IN Supply Configuration for Offline/Telecom Power-Supply Design
 - b. IN Supply Configuration for Low-Voltage DC-DC Converters
12. Secondary Rectifier Configuration
 - a. Self-Driven Synchronous MOSFETs
 - b. Winding Driven Synchronous MOSFETs
 - c. DIODE Rectifier
13. Output Capacitor Selection

- 14. Error Amplifier Compensation Design in Nonisolated Applications
- 15. Thermal Considerations
- 16. Isolated Active-Clamp Forward Converter with Optocoupler Feedback
- 17. MAX17598 Typical Operating Circuit
- 18. Design Example-Active-Clamp Forward Converter Using MAX17598
- 19. Bill of Materials (BOM)

Typical Application Circuit

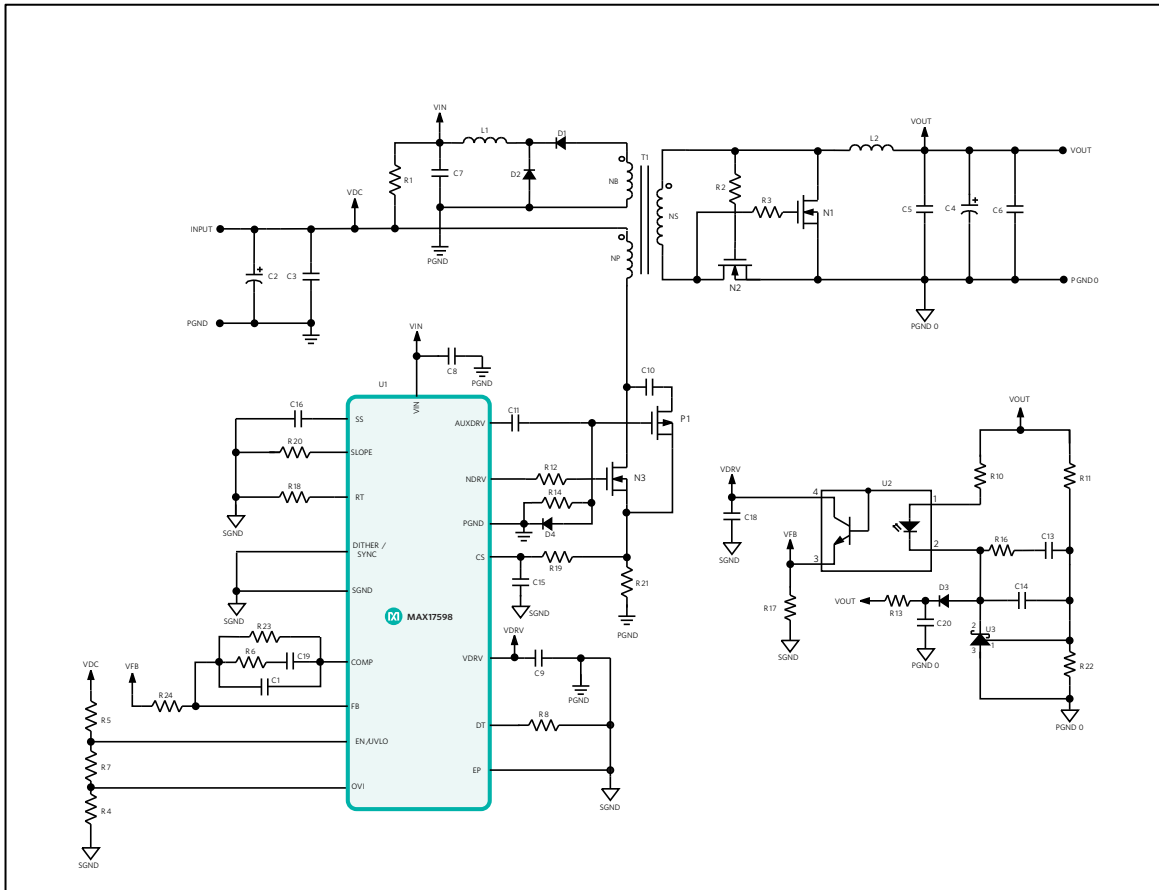


Figure 1. MAX17598 application schematic.

1. Transformer Turns Ratio Selection ($k = N_s/N_p$)

Transformer turns ratio is selected so the output voltage is well regulated across the input voltage range. The maximum operating duty cycle (D_{MAX}) is chosen to be less than the absolute maximum duty cycle of the MAX17598/MAX17599 ICs (72.5%, typical).

$$\text{Transformer turns ratio, } k = \frac{V_{OUT}}{V_{DCMIN} \times D_{MAX}}$$

where D_{MAX} (63%, typical) is the assumed maximum duty cycle at minimum input voltage

Minimum duty cycle at maximum input voltage can be calculated as, $D_{MIN} = \frac{V_{OUT}}{V_{DCMAX} \times k}$

Typical duty cycle at nominal input voltage can be calculated as, $D_{TYP} = \frac{V_{OUT}}{V_{DCTYP} \times k}$

where V_{OUT} is output voltage, V_{DCMIN} , V_{DCTYP} , and V_{DCMAX} are minimum, nominal, and maximum input voltages, respectively.

2. Output Inductor Selection

The output inductance is calculated assuming a maximum peak-to-peak output current ripple (ΔI_{SEC}), which occurs at maximum input voltage. The output inductance can be calculated as follows:

$$L_2 = \frac{V_{OUT} \times (1 - D_{MIN})}{I_{OUT} \times \% \Delta I_{SEC} \times f_{SW}} \quad \text{Henry}$$

where $\% \Delta I_{SEC}$ (0.6, typical) is the ratio of peak-to-peak output inductor current ripple to the average output current at maximum input voltage, I_{OUT} is rated output current in Amperes, f_{SW} is the switching frequency in Hz

The maximum and minimum peak-to-peak output current ripple, maximum secondary peak current can be back calculated for the chosen value of L_2 as follows:

$$\text{Minimum peak-to-peak output inductor current ripple, } \Delta I_{SEC,MIN} = \frac{V_{OUT} \times (1 - D_{MAX})}{L_2 \times f_{SW}} \quad \text{Ampere}$$

$$\text{Maximum peak-to-peak output inductor current ripple, } \Delta I_{SEC,MAX} = \frac{V_{OUT} \times (1 - D_{MIN})}{L_2 \times f_{SW}} \quad \text{Ampere}$$

$$\text{Maximum output peak current, } I_{SEC,PEAK} = I_{OUT} + \frac{\Delta I_{SEC,MAX}}{2} \quad \text{Ampere}$$

3. Primary Magnetizing Inductance Selection

The converter is a peak current-mode controller that controls the peak current as seen by the current-sense resistor, which is the sum of the reflected load current and magnetizing current. It is necessary that the magnitude of reflected load current is always more than the magnetizing current for stable converter operation and well regulated output. This condition is always satisfied, if the magnitude of reflected load current at the input minimum is more than the magnetizing current. Hence, peak-to-peak primary magnetizing current is assumed to be half of the reflected load current at minimum input voltage,

$$\Delta I_{MAG} = \frac{\Delta I_{SEC,MIN} \times k}{2} \quad \text{Ampere}$$

With the assumed peak-to-peak magnetizing current, magnetizing inductance can be calculated as:

$$L_{MAG} = \frac{V_{DCMAX} \times D_{MIN}}{\Delta I_{MAG} \times f_{SW}} \quad \text{Henry}$$

If selected L_{MAG} value is chosen to be different from the above calculated value, then new peak-to-peak magnetizing current ripple can be calculated as follows:

$$\Delta I_{MAG} = \frac{V_{DCMAX} \times D_{MIN}}{L_{MAG} \times f_{SW}} \quad \text{Ampere}$$

$$\text{Maximum primary peak current, } I_{PRI,PEAK} = I_{SEC,PEAK} \times k + \frac{\Delta I_{MAG}}{2} \quad \text{Ampere}$$

4. Clamp Capacitor Selection

The clamp capacitor (C10) helps in resetting the flux in the transformer core as well as helps absorb leakage inductance energy, and forms a complex pole-zero pair with the magnetizing inductance (L_{MAG}) of the transformer, at a frequency f_R .

$$f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C_{10}}}$$

The value of the clamp capacitor for a 20% voltage ripple is calculated as:

$$C_{10} = \frac{\Delta I_{MAG} \times (1 - D_{MIN})^2}{1.6 \times V_{DCMAX} \times f_{SW}} \quad \text{Farad}$$

The voltage stress on the clamp capacitor can be calculated as:

$$V_{C10} = \frac{V_{DCMAX}}{1 - D_{MIN}} \quad \text{Volt}$$

The C10 should be rated for at least 1.4x the calculated worst-case V_{C10} stress.

5. Input Capacitor Selection

Capacitor Selection Based on Switching Ripple (DC-DC Applications)

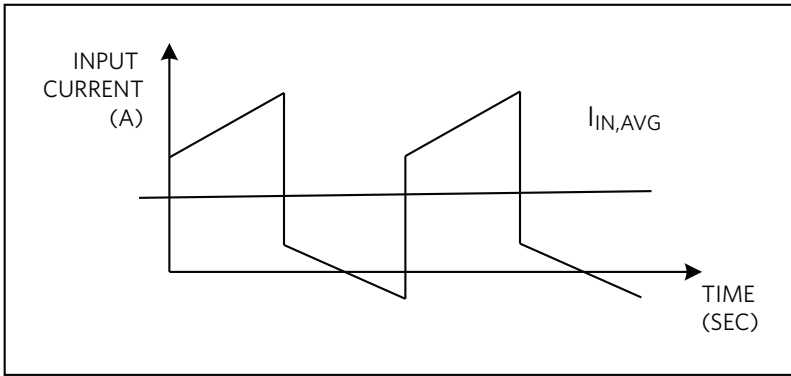


Figure 2. Input current waveform.

The maximum average input current drawn from the input power supply at minimum input voltage can be calculated as:

$$I_{IN,AVG} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{DCMIN}} \quad \text{Ampere}$$

Let the voltage ripple present on the input capacitor is 2% of the minimum input voltage and is given as:

$$\Delta V_{DC,RIPPLE} = 0.02 \times V_{DCMIN} \text{ (Typical)} \quad \text{Volts}$$

The value of the input ceramic capacitor with the above assumed ripple voltage can be calculated as follows:

$$C_3 = \frac{I_{IN,AVG} \times (1 - D_{MAX})}{\Delta V_{DC,RIPPLE} \times f_{SW}} \quad \text{Farad}$$

where η is the expected efficiency (0.9 to 0.95) of the converter, $\Delta V_{DC,RIPPLE}$ is the ripple present on the input capacitor.

Use an electrolytic capacitor in parallel with the input ceramic capacitor to mitigate input oscillations present due to input lead inductance.

a. Capacitor Selection Based on Rectified Line Voltage Ripple in AC-DC Applications (MAX17598)

In the forward converter topology, the DC bus capacitor supplies the input power when the diode bridge rectifier is off. The voltage discharge on the input capacitor, due to the input average current, should be within the limits specified.

Assuming 25% ripple present on input DC capacitor, the input capacitor can be calculated as follows:

$$C_2 = \frac{2.25 \times P_{LOAD}}{\eta \times f_{Line} \times V_{IN,PK}^2} \quad \text{Farad}$$

where

P_{LOAD} = Rated output power.

η = Typical converter efficiency (0.9 to 0.95) at $V_{ac,min}$ and I_{LOAD} . $V_{IN,PK} = \sqrt{2} \times V_{ac,min}$ = peak voltage at minimum input AC voltage.

$V_{ac,min}$ = Minimum AC input voltage.

f_{Line} = Line frequency.

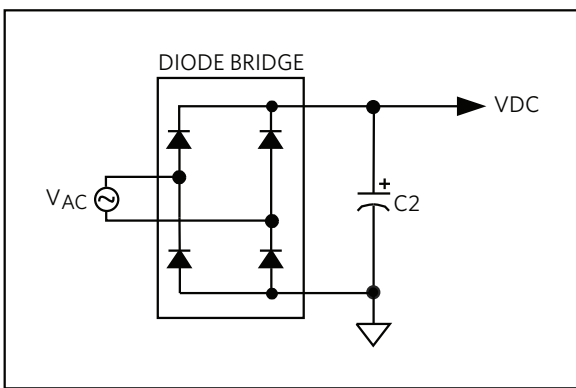


Figure 3. Input capacitor selection.

b. Capacitor Selection Based on Holdup Time Requirements in AC-DC Applications (MAX17598)

For a given output power (P_{HOLDUP}) that needs to be delivered during holdup time (t_{HOLDUP}), the DC bus voltage at which the AC supply fails (V_{DCFAIL}), and the minimum DC bus voltage at which the converter can regulate the output voltages (V_{DCMIN}), the input capacitor (C_{IN}) is estimated as:

$$C_2 = \frac{3 \times P_{HOLDUP} \times t_{HOLDUP}}{(V_{DCFAIL}^2 - V_{DCMIN}^2)} \quad \text{Farad}$$

The input capacitor RMS current for AC-DC applications can be calculated as:

$$I_{INRMS} = \frac{2.7 \times P_{LOAD}}{\eta \times V_{IN,PK}} \quad \text{Ampere}$$

6. Primary n-MOSFET Selection

n-MOSFET selection criteria include maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction

temperature limits. The n-MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage:

$$V_{N3,DS} = \frac{V_{DCMAX}}{1 - D_{MIN}} \quad \text{Volt}$$

The N3 should be rated for at least 1.3x the calculated worst-case $V_{N3,DS}$ stress.

Maximum RMS current through n-MOSFET can be calculated as below:

$$I_{N3,RMS} = I_{IN,TON} \times \sqrt{D_{MAX}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I}{I_{IN,TON}} \right)^2} \quad \text{Ampere}$$

where:

$\Delta I = \Delta I_{SEC,MIN} \times k + \Delta I_{MAG}$, peak-to-peak input current ripple at minimum input voltage

$$I_{IN,TON} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{DCMIN} \times D_{MAX}} \quad \text{Ampere}$$

7. Current-Sense Resistor Selection

Current-sense resistor R_{21} is used to set the peak current limit and can be calculated as:

$$R_{21} = \frac{0.305}{1.2 \times I_{PRI,PEAK}} \quad \Omega$$

The power dissipation in the resistor is calculated as follows:

$$P_{R21} = I_{N3,RMS}^2 \times R_{21} \quad \text{W.}$$

The R21 power rating should be at least 2x the value calculated above.

8. Primary p-MOSFET Selection

The p-MOSFET P1 conducts when the main n-MOSFET N3 is turned off with a programmable delay. During this period there is no transfer of energy to the output and the magnetizing energy is circulated within the primary circuit. The maximum drain voltage and RMS current rating of the p-MOSFET are given below:

The drain voltage rating of the p-MOSFET is:

$$V_{P1,DS} = \frac{V_{DCMAX}}{1 - D_{MIN}} \quad \text{Volt}$$

The P1 should be rated for at least 1.3x the calculated worst-case $V_{P1,DS}$ stress.

The RMS current rating of the p-MOSFET is:

$$I_{P1,RMS} = \Delta I_{MAG} \times \sqrt{\frac{1 - D_{MIN}}{12}} \quad \text{Ampere}$$

9. p-MOSFET Gate-Drive Circuit for Low-Side Active-Clamp Configuration

The MAX17598/MAX17599 ICs are designed with NDRV and AUXDRV output signals that are essentially in phase with each other, with a programmable dead time between them that is set using resistor R8. Since, the AUXDRV signal is used to drive a p-MOSFET in a low-side active-clamp configuration that is discussed in this application note, the signal needs to be level shifted below ground for complete turn-on of P-MOSFET. A resistor, capacitor, and diode combination (R14-C11-D4) as shown in **Figure 4** is used to drive the p-MOSFET.

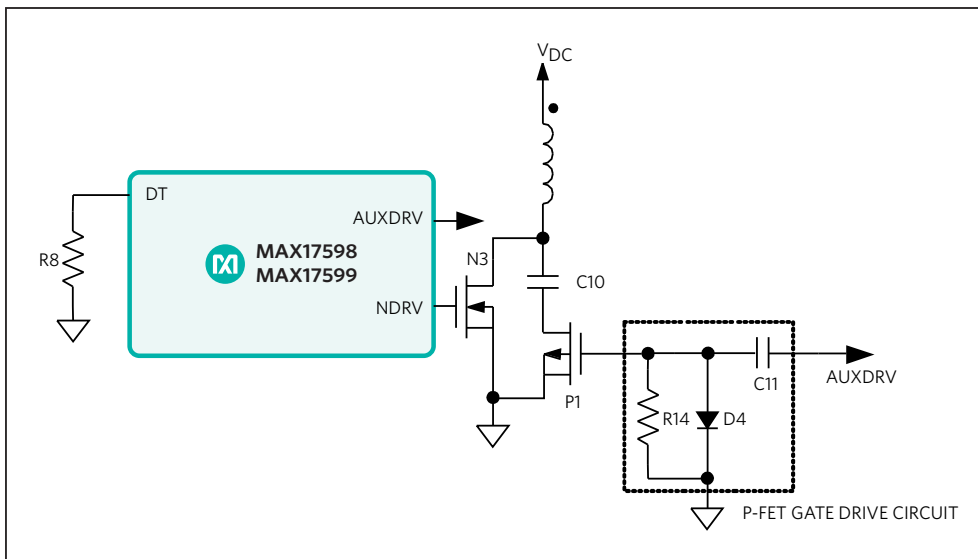


Figure 4. p-MOSFET gate-drive circuit.

C₁₁: typical value in the range of 47nF to 100nF

R₁₄ is selected so the time constant is much greater than the switching period to maintain the voltage across C₁₁ relatively constant during the turn-OFF period. Use the following equation to calculate the value of R₁₄:

$$R_{14} = \frac{100}{C_{11} \times f_{SW}} \quad \Omega$$

D₄: Select a Schottky or fast recovery diode with maximum reverse voltage equal to V_{DRV}

10. SLOPE Compensation

The MAX17598/MAX17599 can operate at a maximum duty cycle of 72.5%, slope compensation is required to prevent sub-harmonic instability that occurs naturally in continuous conduction mode, peak current-mode-controlled converters operating at duty cycles greater than 50%. A minimum slope signal is added internally to the sensed current signal, even for converters operating below 50% duty to provide stable, jitter-free operation.

Use the following formula to calculate the amount of slope required for operating duty cycles greater than 50%.

$$S_E = \left(0.82 \times \frac{V_{OUT}}{L_2} \times k - \frac{V_{INMIN}}{L_{MAG}} \right) \times R_{21} \times 10^3$$

where L_2 is output inductance, L_{MAG} is primary magnetizing inductance expressed in μH , S_E is in $\frac{\text{mV}}{\mu\text{s}}$

If S_E is less than $50 \frac{\text{mV}}{\mu\text{s}}$, then slope resistor should be left open to enable internal minimum slope compensation. If S_E is more than $50 \frac{\text{mV}}{\mu\text{s}}$, then calculate the slope resistor using the following formula:

$$R_{20} = \frac{S_E - 8}{1.55} \text{ k}\Omega, \text{ Where } S_E \text{ in } \frac{\text{mV}}{\mu\text{s}}, R_{20} \text{ in k}\Omega$$

11. Bias Supply Configuration

The bias power supply for the MAX17598/MAX17599 at the V_{IN} pin needs to be generated based on the input voltage range specifications, and power dissipation/efficiency considerations.

a. Bias Supply Configuration for Offline/Telecom Power-Supply Design (MAX17598)

For offline and Telecom input power-supply ranges, a simple RC circuit is used to start up the MAX17598. In **Figure 5**, V_{DC} represents the rectified AC line for offline applications and the 36V to 72V DC bus for telecom applications. In both cases, to sustain the operation of the circuit, the input supply to the IC is bootstrapped with a bias winding N_B , diodes D_1 , D_2 , filter inductor L_1 , and C_7 as shown in Figure 5. Basically, C_7 charges to the UVLO rising threshold (20V, typical) with R_1 , and the MAX17598 starts to generate NDRV gate pulses at this point using energy from C_7 causing its voltage to fall. This also causes pulses to appear at the bias winding N_B . The voltage on C_7 will be sustained, if the bias-winding pulses are able to prevent the V_{IN} voltage from falling below the UVLO falling threshold (7V, typical) by charging up C_7 . (Refer to the [MAX17598/MAX17599 data sheet](#) for details on the principle of operation and design method for R_1 and C_7).

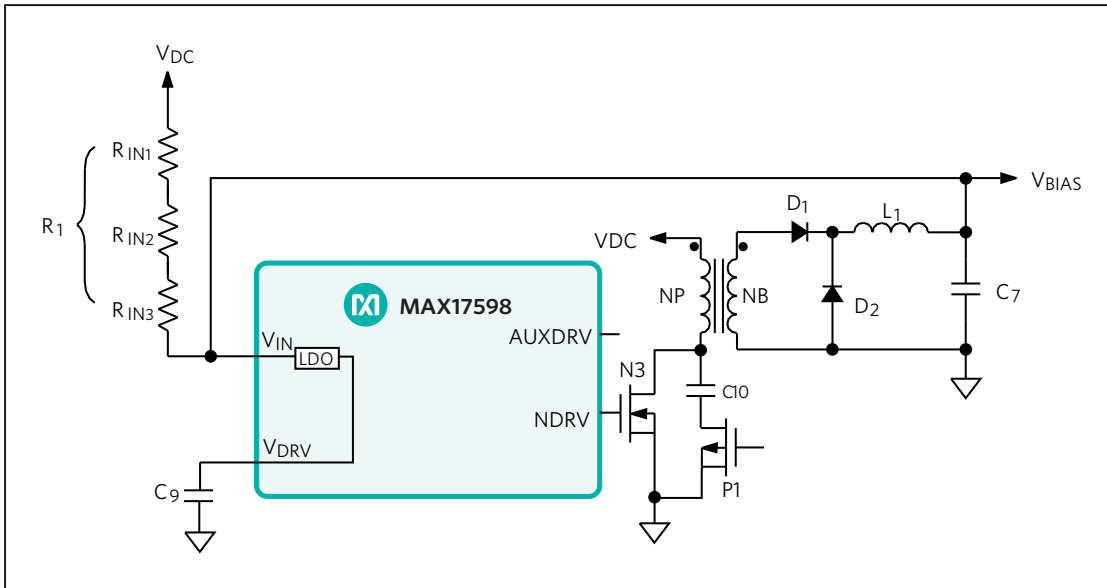


Figure 5. Bias supply configuration for offline/telecom power-supply design.

i. BIAS-Winding Turns Ratio Calculation (N_B/N_P)

The transformer turns ratio ($K_B = N_B/N_P$) can be calculated as follows:

$$K_B = \frac{V_{BIAS}}{D_{MAX} \times V_{DCMIN}}$$

where V_{BIAS} is the steady-state voltage on the IN pin. Typically V_{BIAS} is chosen as 12V.

ii. BIAS Inductor (L_1) Selection

The inductor for the bias-winding feedback configuration can be chosen as follows:

$$L_1 = \frac{V_{BIAS} \times (1 - D_{MIN})}{0.003 \times f_{SW}} \quad \text{Henry}$$

b. Bias Supply Configuration for Low-Voltage DC-DC Applications (MAX17599)

The MAX17599 is optimized for low-voltage DC-DC applications with a UVLO V_{IN} wake-up level of 4.1V (typ) with 200mV hysteresis. The bias winding configuration is needed in such low-voltage DC-DC applications (4.5V to 13.2V for example) when it is acceptable to have the additional complexity of the bias winding and associated components for the sake of efficiency improvement. For low power applications, the total current required to supply the IC and the gate currents for external MOSFETs may be small enough to permit an approach where the input voltage can be directly used for IC supply, as shown in **Figure 6**. See section 15 for details on thermal considerations for the MAX17598/MAX17599.

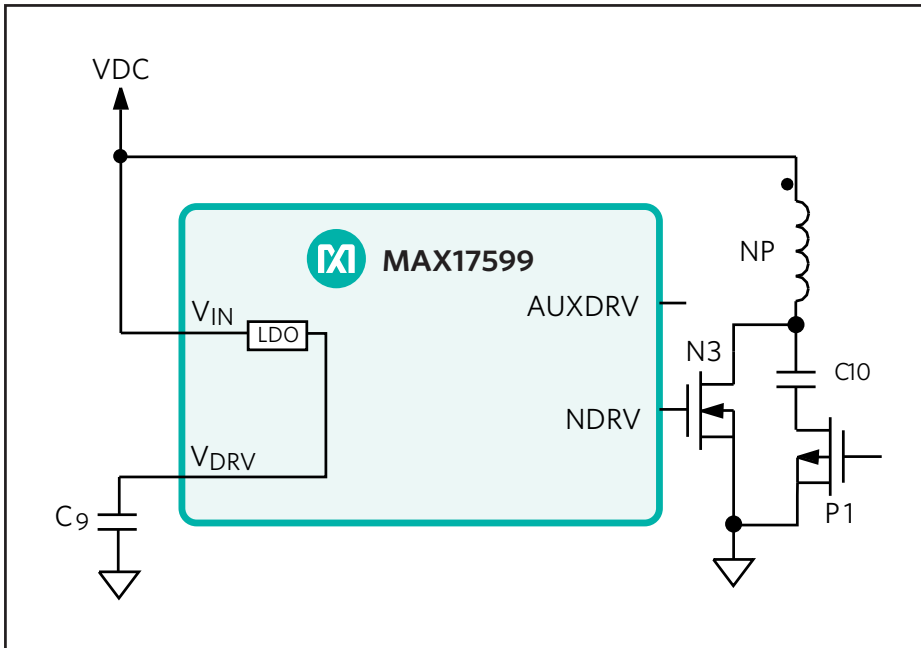


Figure 6. Bias supply configuration for low-voltage isolated DC-DC designs.

Two bias winding approaches suitable for low voltage (18V to 36V for example) DC-DC power supplies are shown in **Figure 7** and **Figure 8**. Figure 7 shows a “forward converter” type bias winding approach similar to that outlined for the Max17598. Figure 8 shows an alternate approach that uses a peak rectified bias winding. These approaches reduce power dissipation in the internal LDO and help improve efficiency. In both cases, R_z , Z_1 , Q_1 , and D_5 are needed to start the IC and sustain the supply before the bias-winding output powers up. The peak rectified approach produces a V_{BIAS} voltage that varies with input supply, and therefore suffers from higher power dissipation at high line conditions. The “forward converter” type bias winding approach produces a relatively constant V_{BIAS} voltage and keeps power dissipation in the device to a minimum under all line conditions.

For a 7.5V zener Z_1 , the value of R_z can be calculated as:

$$R_z = 9 \times (V_{DCMIN} - 7.5)K\Omega$$

$$C_7 = 10 [Q_G + (0.003/f_{sw})] \text{ Farad}$$

where

Q_G : Total gate charge of N_3 and P_1

f_{sw} : Switching frequency in Hz

Q_1 : Choose a small footprint transistor with blocking voltage greater than V_{DCMAX} and collector current in the order of 10mA.

D_5 : 1N4148

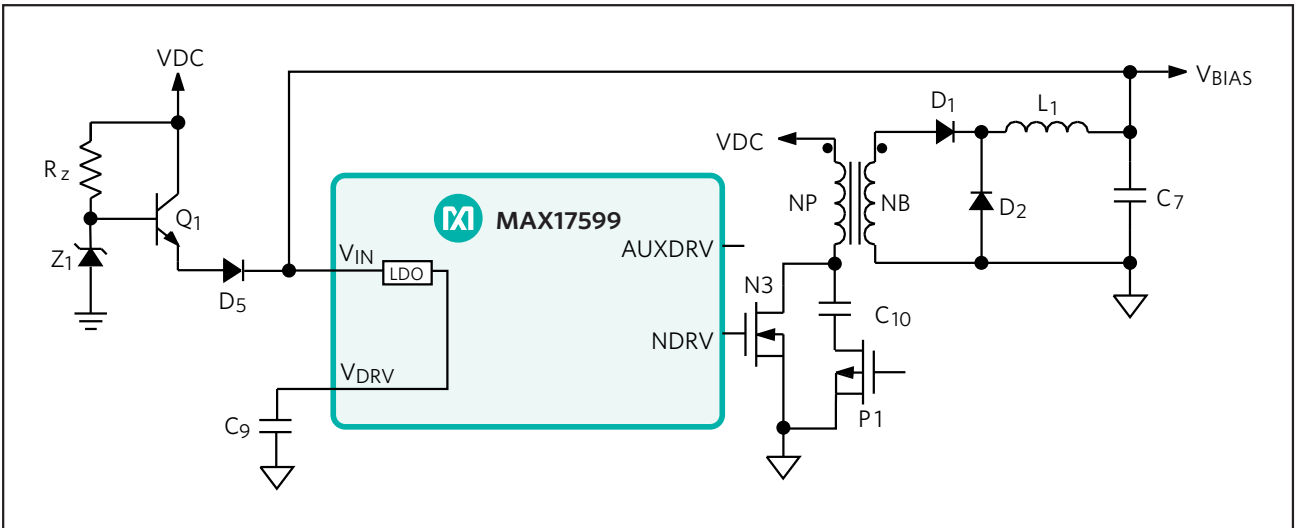


Figure 7. Forward converter type bias-winding supply configuration for low-voltage isolated DC-DC designs.

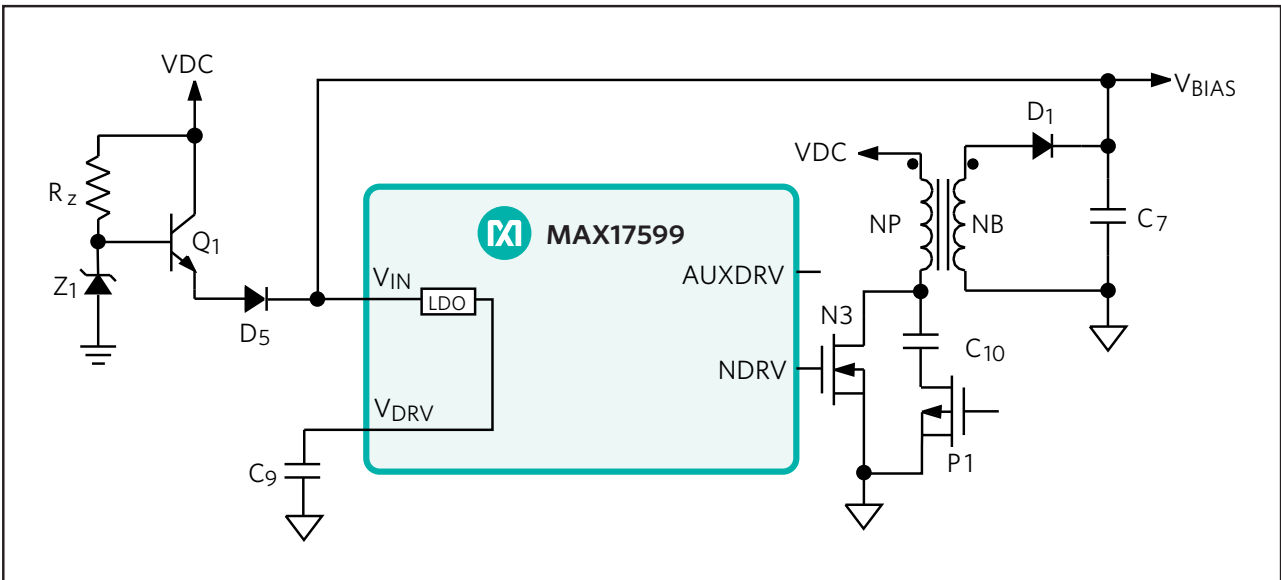


Figure 8. "Peak rectified" bias-winding supply configuration for low-voltage isolated DC-DC designs.

12. Secondary Rectifier Selection

The secondary-side rectification can be achieved either by using MOSFETs or diodes as explained below.

a. Self-Driven Secondary Synchronous MOSFETs (N1, N2) Selection

Secondary rectification using synchronous MOSFETs is shown in

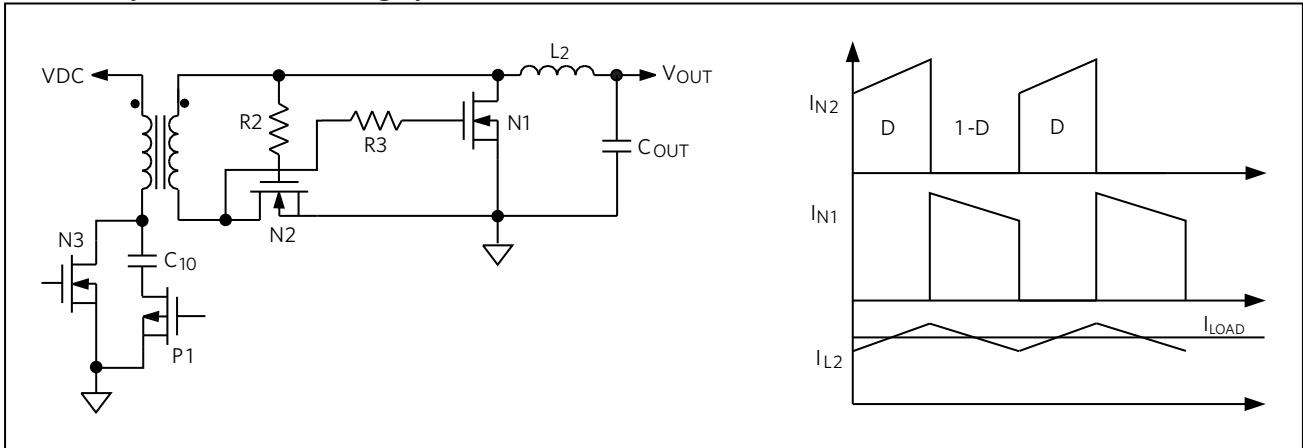


Figure 9. When the primary n-FET (N3) is turned ON, the input power is transferred instantaneously to the output through forward conducting MOSFET N2. During the turn-OFF period, the output inductor current freewheels through MOSFET N1. Synchronous rectification is highly recommended in high output current applications to improve overall efficiency by reducing the secondary rectifier losses.

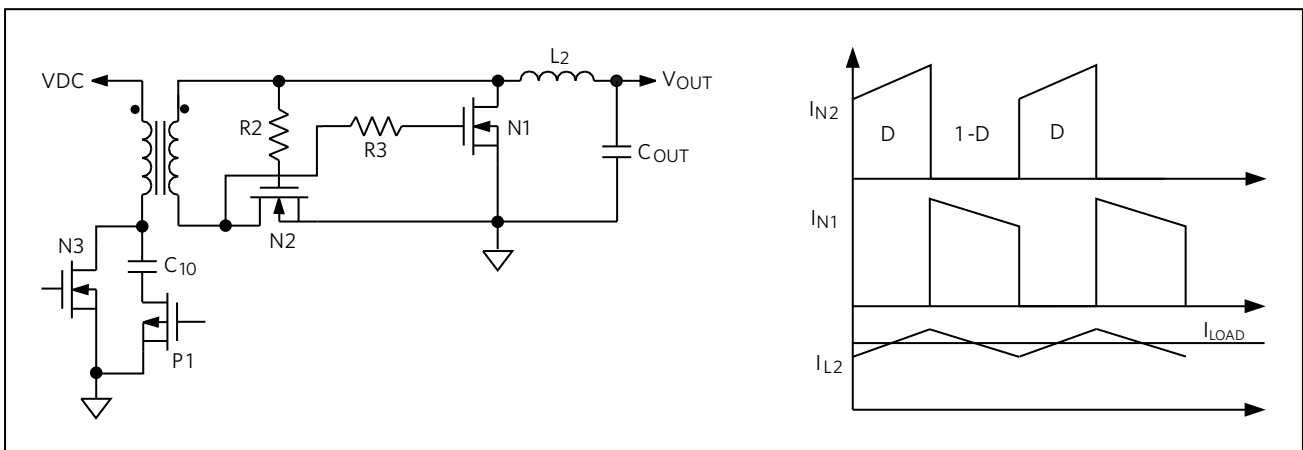


Figure 9. Self-driven synchronous MOSFET rectification circuit and waveforms.

Control MOSFET

The maximum drain voltage of control MOSFET N2 on the secondary is given as:

$$V_{DS,N2} = k \times \frac{V_{DCMIN} \times D_{MAX}}{1 - D_{MAX}} \quad \text{Volt}$$

The N2 should be rated for at least 1.3x the calculated worst-case $V_{DS,N2}$ stress.

The maximum RMS current rating of control MOSFET N2 on the secondary is given as:

$$I_{RMS,N2} = I_{OUT} \times \sqrt{D_{MAX}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{SEC,MIN}}{I_{OUT}} \right)^2} \quad \text{Ampere}$$

The maximum applied gate voltage to control MOSFET N2 is given as:

$$V_{N2,GATE} = k \times V_{DCMAX} \quad \text{Volt}$$

Freewheeling MOSFET

The maximum drain voltage of the freewheeling FET on the secondary is given as:

$$V_{DS,N1} = k \times V_{DCMAX} \quad \text{Volt}$$

The N1 should be rated for at least 1.3x the calculated worst-case $V_{DS, N1}$ stress.

The maximum RMS current rating of the freewheeling FET on the secondary is given as:

$$I_{RMS,N1} = I_{OUT} \times \sqrt{1 - D_{MIN}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{SEC,MAX}}{I_{OUT}} \right)^2} \quad \text{Ampere}$$

The maximum applied gate voltage to the freewheeling FET is given as:

$$V_{N1,GATE} = k \times \frac{V_{DCMIN} \times D_{MAX}}{1 - D_{MAX}} \quad \text{Volt}$$

The $V_{N1, GATE}$ and $V_{N2, GATE}$ should be less than the maximum operating gate voltage (15V, typically) of the MOSFET. It is advantageous to keep this value as low as possible to minimize the gate-drive losses of the MOSFET.

Note: Designer should add an external gate resistors (R2, R3) in the gate paths of secondary MOSFETs(N2, N1), to damp the ringing due to secondary leakage inductance (L_{leak}) and the gate capacitance (C_{gate}). The range for the gate resistors is given below.

$$R_{gate(min)} = \sqrt{\frac{L_{leak}}{C_{gate}}} \quad R_{gate(max)} = Tc / (5 * C_{gate})$$

where $Tc = (I_{SEC,PEAK} \times L_{LEAK} \times N_p) / (V_{DCMAX} \times N_s)$, $I_{SEC,PEAK}$ (refer section 2) and L_{LEAK} is secondary-side leakage inductance

However the precise value of the gate resistor will depend upon the specifics of the each application, and should be optimized in the lab. Typical values for gate resistors range from 4.7Ω to 22Ω.

Most applications need a RC snubber as well across the secondary MOSFETs to minimize the drain node ringing. RC snubber design is out of scope for this application note. Use any standard practice for RC snubber design.

b. Winding Driven Secondary Synchronous MOSFETs (N1, N2)

In self-driven synchronous rectification, the maximum gate voltage of the control MOSFET N2 is the same as the maximum drain voltage of the freewheeling MOSFET N1 and vice-versa. Also, the drain voltage of the secondary synchronous MOSFETs depends on the input voltage, duty cycle and turns ratio. The drain voltages and gate voltages increase with input and output voltages, which imposes constraints on self-driven synchronous rectification. In such applications, the synchronous MOSFETs are driven from a third winding (NG) as shown in **Figure 10**. An example specification for such a situation would be a 12V output from an 18V to 36V input source. It should be noted that drive winding NG should be tightly coupled to secondary winding NS to avoid undesirable oscillations on the gate voltage waveforms. A resistor in series with NG (not shown here) can be included in the prototype schematic, and used if needed, for the necessary damping of gate-voltage oscillations that may be required in practice.

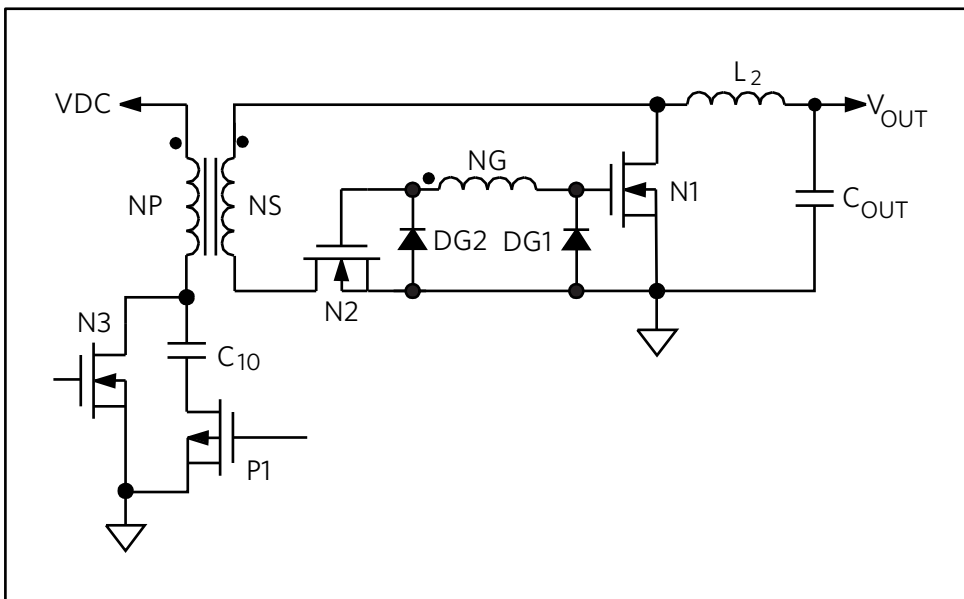


Figure 10. Winding driven synchronous MOSFET rectification.

Turns ratio ($k_{gate} = \frac{N_G}{N_P}$) in the winding driven topology can be calculated as follows:

$$k_{gate} = \frac{V_{GATE,MAX}}{V_{DCMAX}}$$

where $V_{GATE,MAX}$ is the maximum gate voltage (typical 15V) at maximum input voltage.

NOTE: Extra care is needed in transformer design to minimize the leakage inductance with the gate winding.

c. Secondary DIODE Rectifier (DS1, DS2) Selection

Secondary rectification using diodes is shown in **Figure 11**. When primary MOSFET N3 is ON, the input power is transferred to the output through diode DS2. During the turn-OFF period, inductor current freewheels through the DS1 diode. In high output current applications, secondary diode rectification is not recommended due to high diode conduction losses.

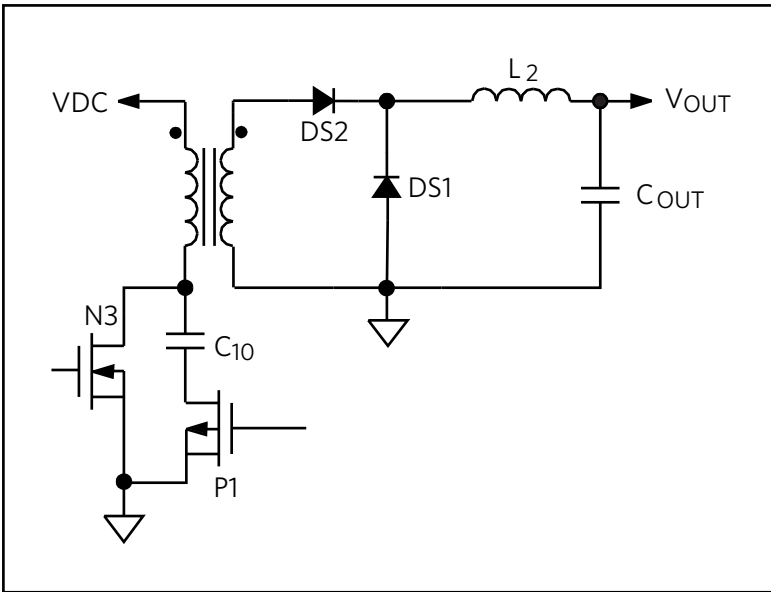


Figure 11. Secondary DIODE rectification.

The voltage rating of the DS2 diode is:

$$V_{DS2} = k \times \frac{V_{DCMIN} \times D_{MAX}}{1 - D_{MAX}} \text{ Volt}$$

The DS2 should be rated for at least 1.3x the calculated worst-case V_{DS2} stress.

The current rating of diode DS2 is:

$$I_{DS2} = D \times I_{OUT} \quad \text{Ampere}$$

The DS2 should be rated for at least 1.3x the calculated worst-case I_{DS2} stress.

The voltage rating of the DS1 diode is:

$$V_{DS1} = k \times V_{DCMAX} \quad \text{Volt}$$

The DS1 should be rated for at least 1.3x the calculated worst-case V_{DS1} stress.

The current rating of the DS1 diode is:

$$I_{DS1} = (1 - D) \times I_{OUT} \quad \text{Ampere}$$

The DS1 should be rated for at least 1.3x the calculated worst-case I_{DS1} stress.

13. Output Capacitor Selection

Output capacitance value can be calculated based on either steady-state voltage ripple or transient voltage ripple.

If the design consideration is the steady-state voltage ripple, then the output capacitance can be calculated as follows:

$$C_{OUT} = \frac{\Delta I_{SEC,MAX}}{8 \times \Delta V_{COUT,SS} \times f_{SW}} \quad \text{Volt}$$

Apart from the capacitive component of the voltage ripple, R_{ESR} of the output capacitance also contributes the steady-state voltage ripple, which is selected as follows:

$$R_{ESR} = \frac{\Delta V_{COUT,SS}}{\Delta I_{SEC,MAX}}$$

where $\Delta I_{SEC,MAX}$ is the maximum peak-to-peak output current ripple on the inductor.

$\Delta V_{COUT,SS}$ is the steady-state voltage ripple typically chosen 1% of the output voltage.

$$\Delta I_{SEC,MAX} = \frac{V_{OUT} \times (1 - D_{MIN})}{L_2 \times f_{SW}}$$

If the design consideration is the transient steady-state voltage ripple, then the output capacitor is usually sized to support a step load of 25% of the rated output current (I_{OUT}) in isolated applications so that the output-voltage deviation ($\Delta V_{OUT,TR}$) is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT,TR}} \quad \text{Farad}$$

where

C_{OUT} is the total capacitance required at the output (C4, C5, C6 in the schematic).

Response time of the controller $t_{RESPONSE}$ is given as:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}} \right) \quad \text{seconds}$$

The complex pole-zero pair frequency formed due to clamp capacitor and magnetizing inductance of the converter is given as:

$$f_R = \frac{1 - D_{MAX}}{2 \times \pi \times \sqrt{L_{MAG} \times C_{10}}} \quad \text{Hz}$$

Choose $f_C = \frac{f_R}{5}$ limited to 10kHz.

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation during transient, and f_C is the target closed-loop crossover frequency.

RMS current rating of the output capacitor can be calculated as follows:

$$I_{COUT,RMS} = \frac{\Delta I_{SEC,MAX}}{2 \times \sqrt{3}} \quad \text{Ampere}$$

Note: If an electrolytic capacitor is chosen at the output, the ESR of the output capacitor forms a zero with the output capacitance. It is recommended to select an ESR value so the zero location is at least twice the crossover frequency, so as not to have any effect on bandwidth. Select the electrolytic/tantalum output capacitor with ESR as given below:

$$R_{ESR} \leq \frac{1}{4 \times \pi \times f_C \times C_{OUT}} \quad \Omega$$

where f_C is the target crossover frequency, C_{OUT} is the total output capacitance at the output, R_{ESR} is the ESR of the output electrolytic capacitor.

14. Error Amplifier Compensation Design

For nonisolated designs, output voltage feedback and the loop compensation network are connected as shown in **Figure 12**.

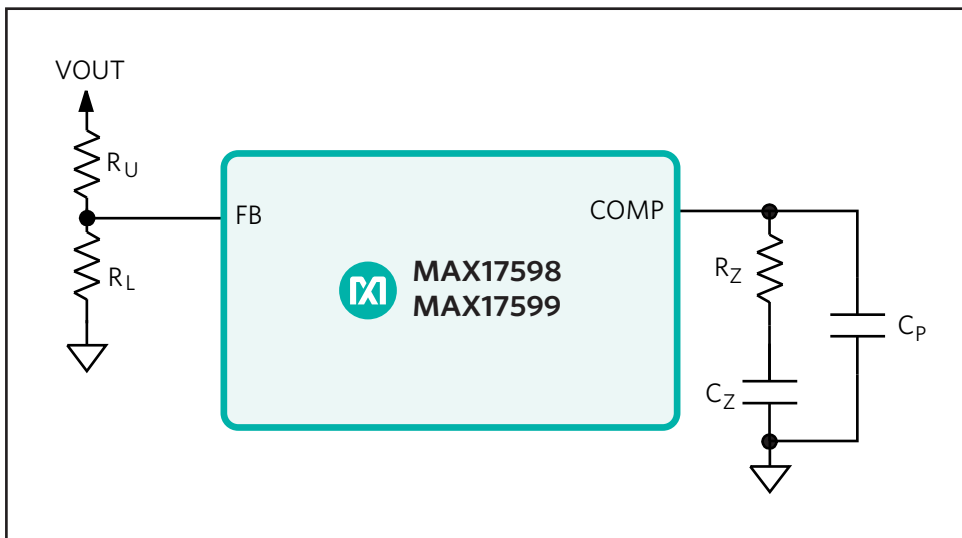


Figure 12. Loop compensation arrangement for nonisolated designs.

$$S_e = 50 \times 10^3 + \frac{V_{DC,TYP} \times R_{21}}{L_{MAG}}$$

$$S_n = k \times R_{21} \times \left(\frac{k \times V_{DC,TYP} - V_{OUT}}{L_2} \right)$$

$$m = 1 + \frac{S_e}{S_n}$$

$$G_{DC} = \frac{V_{OUT}}{2 \times k \times I_{OUT} \times R_{21}} \times \frac{1}{1 + \frac{V_{OUT}}{I_{OUT} \times L_2 \times f_{SW}} \times (m \times (1 - D_{TYP}) - 0.5)}$$

The loop compensation values are calculated as follows:

$$R_Z = \frac{400 \times V_{OUT}}{G_{DC}} \times \sqrt{\frac{1 + \left(\frac{f_C}{f_P}\right)^2}{1 + \left(\frac{f_C}{f_Z}\right)^2}} \quad \Omega$$

$$C_Z = \frac{1}{2\pi \times R_Z \times f_P} \quad \text{Farad}$$

$$C_P = \frac{1}{\pi \times R_Z \times f_{SW}} \quad \text{Farad}$$

where:

$$f_P = \frac{1}{2\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} + \frac{(m \times (1 - D_{TYP}) - 0.5)}{2\pi \times L_2 \times C_{OUT} \times f_{SW}}, \quad \text{Hz}$$

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}, \quad \text{Hz}$$

$$f_C = \frac{f_R}{5} \text{ limited to 10kHz, where } f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG}} \times C_{10}} \quad \text{Hz}$$

f_{SW} is switching frequency in Hz, k is the transformer turns ratio.

R_U value is chosen based on minimum load and efficiency. For a typical value of $R_U = 49.9\text{k}\Omega$, calculate R_L using equation:

$$R_L = \frac{R_U}{\left(\frac{V_{OUT}}{1.21} - 1\right)}$$

15. Isolated Active-Clamp Forward Converter with Optocoupler Feedback

Optocoupler feedback is used in isolated forward converter design for precise control of isolated output voltage. This section describes the different configurations of a controller and outlines a procedure to calculate compensating network component values. The overall scheme of optocoupler feedback is shown in **Figure 13**.

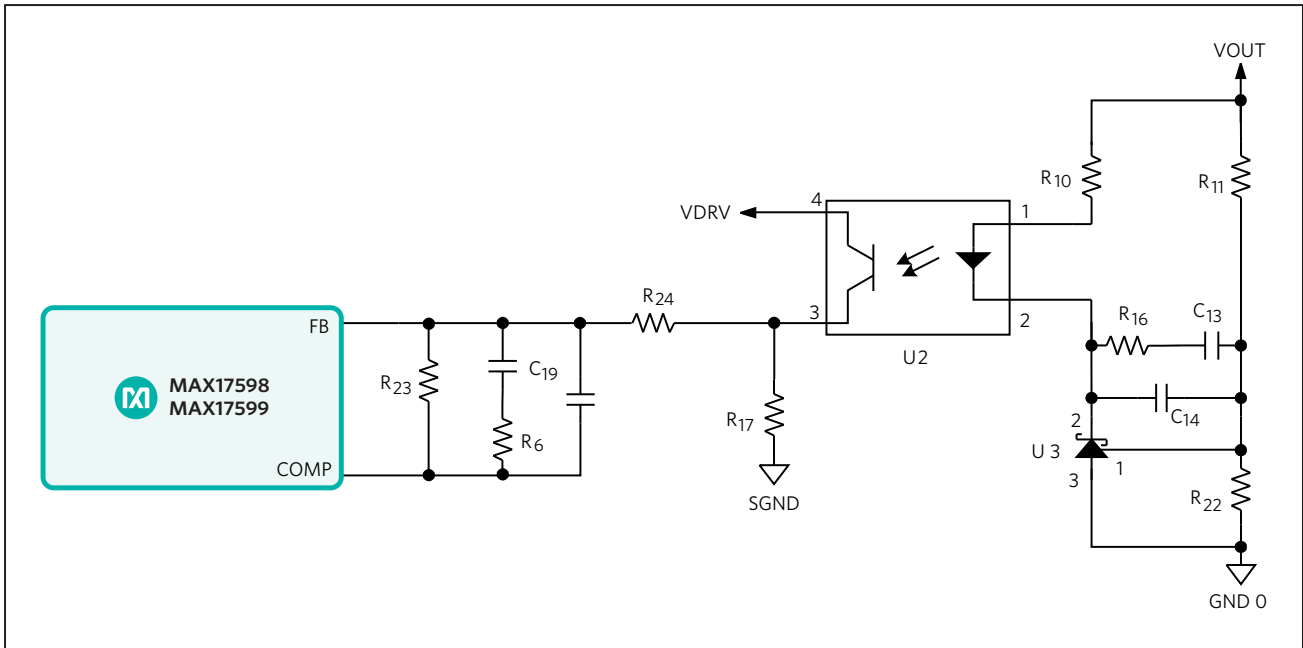


Figure 13. Optocoupler feedback for isolated designs.

Use $R_{17} = 470\Omega$ (typ), for an optocoupler transistor current of 1mA. Select $R_1 = 49.9k\Omega$ (range of values, 33k Ω to 68k Ω) and $R_2 = 22k\Omega$ (range of values, 15k Ω to 47k Ω) (typical values), to use the full range of available COMP voltage. U3 is a low-voltage adjustable shunt regulator with a 1.24V reference voltage. Calculate R_{LED} using the equation below, based on output voltage V_{OUT} .

$$R_{10} = 400 \times CTR \times (V_{OUT} - 2.7) \Omega$$

The bandwidth of typical optocouplers limits the achievable closed-loop bandwidth of optoisolated converters. Considering these limitations, the closed-loop crossover frequency may be chosen, at the nominal input voltage as follows:

$$f_c = \frac{f_R}{5} \text{ limited to 10kHz}$$

Closed-loop compensation values are designed based on the open-loop gain at the desired crossover frequency, f_c . The open-loop gain at, f_c is calculated using the following expression:

$$G_{PLANT} = G_{DC} \times \sqrt{\frac{1 + \left(\frac{f_c}{f_z}\right)^2}{1 + \left(\frac{f_c}{f_p}\right)^2}}$$

Use the above equation for G_{PLANT} in further calculations in isolated controller design configurations.

Three controller configurations are suggested, based on open-loop gain and the value of R_{LED} . For typical designs, the current transfer ratio (CTR) of the optocoupler designs can be assumed to be

unity. It is known that the comparator and gate-driver delays associated with the input voltage variations affects the optocoupler CTR. Depending on the opto-coupler selected, variations in CTR cause wide variations in bandwidth of the closed-loop system across the input-voltage operating range. It is recommended to select an optocoupler with less CTR variations across the operating range.

Choose $R_{11} = 49.9\text{k}\Omega$, calculate R_{22} using:

$$R_{22} = \frac{R_{11}}{\left(\frac{V_{OUT}}{1.24} - 1\right)}$$

Configuration 1: When $\left(G_{PLANT} \times CTR \times \frac{R_{17}}{R_{10}} \times \frac{R_{23}}{R_{24}}\right) \leq 0.8$

$$R_{16} = \left(\frac{R_{10} \times R_{24}}{G_{PLANT} \times CTR \times R_{17} \times R_{23}} - 1\right) \times R_{11} \quad \Omega$$

$$C_{13} = \frac{1}{2\pi \times (R_{11} + R_{16}) \times f_p} \quad \text{Farad}$$

$$C_{14} = \frac{1}{\pi \times f_{SW} \times R_{16}} \quad \text{Farad}$$

where $CTR = 1$, $R_{11} = 49.9\text{k}\Omega$, $R_{23} = 49.9\text{k}\Omega$, $R_{24} = 22\text{k}\Omega$, $R_{17} = 470\Omega$

The schematic for this controller configuration is depicted in **Figure 14**.

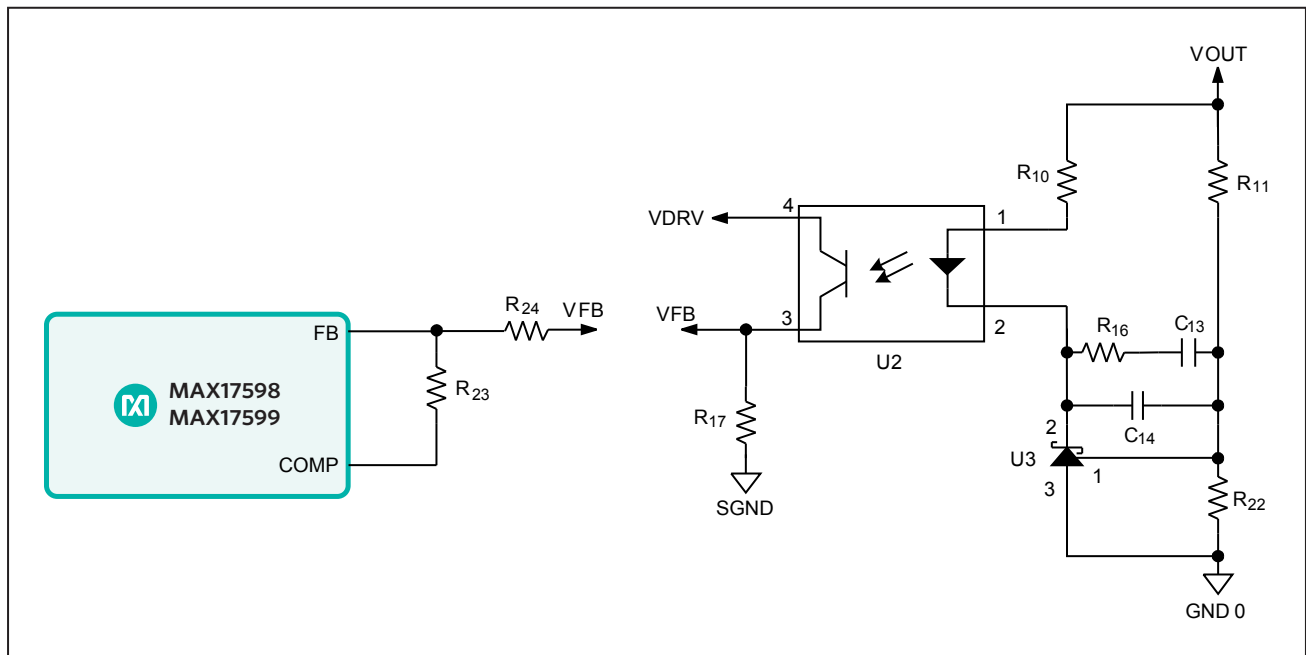


Figure 14. Controller configuration 1.

Configuration 2: When $\left(G_{PLANT} \times CTR \times \frac{R_{17}}{R_{10}} \times \frac{R_{23}}{R_{24}} \right) \geq 1.2$

$$R_6 = \frac{R_{23}}{\left(\frac{G_{PLANT} \times CTR \times R_{17} \times R_{23}}{R_{10} \times R_{24}} - 1 \right)} \Omega$$

$$C_{19} = \frac{10}{\pi \times R_6 \times f_C} \text{ Farad}$$

$$C_1 = \frac{(R_{23} + R_6)}{\pi \times R_{23} \times f_{SW} \times R_6} \text{ Farad}$$

$$C_{14} = \frac{1}{2\pi \times R_{11} \times f_P} \text{ Farad}$$

where $CTR = 1$, $R_{11} = 49.9\text{k}\Omega$, $R_{23} = 49.9\text{k}\Omega$, $R_{24} = 22\text{k}\Omega$, $R_{17} = 470\Omega$

The schematic for this controller configuration is depicted in **Figure 15**.

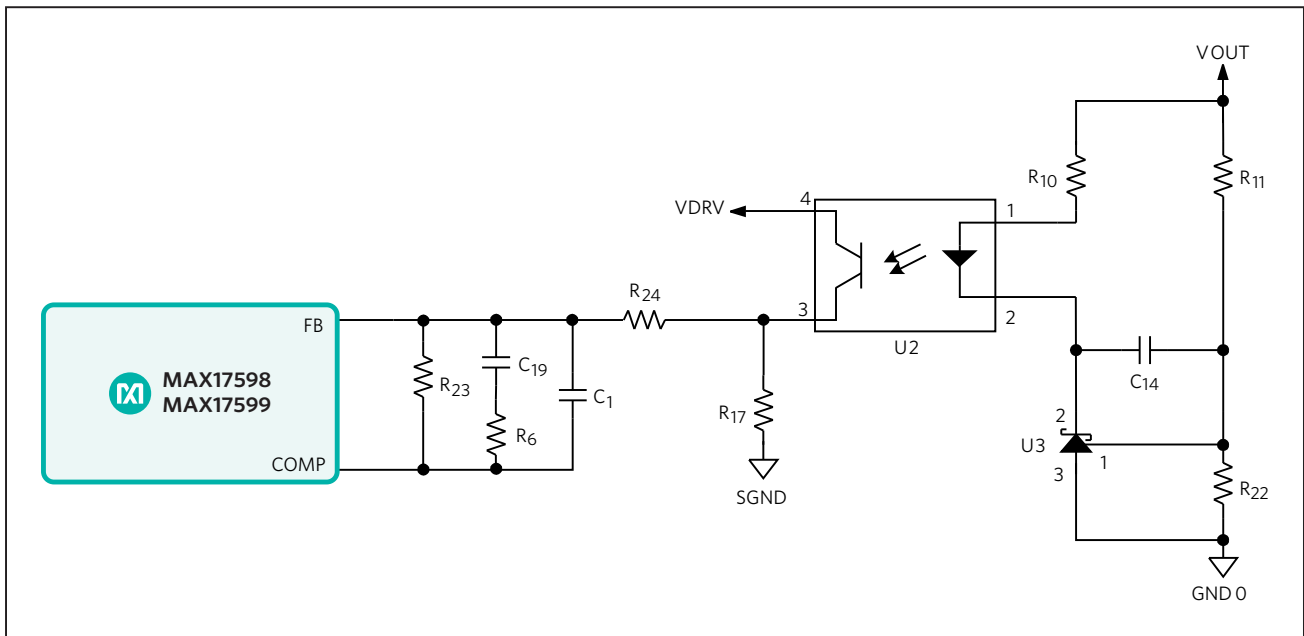


Figure 15. Controller configuration 2.

Configuration 3: When $0.8 < \left(G_{PLANT} \times CTR \times \frac{R_{17}}{R_{10}} \times \frac{R_{23}}{R_{24}} \right) < 1.2$

$$C_1 = \frac{1}{\pi \times R_{23} \times f_{SW}} \text{ Farad}$$

$$C_{14} = \frac{1}{2\pi \times R_{11} \times f_P} \text{ Farad}$$

where $CTR = 1$, $R_{11} = 49.9\text{k}\Omega$, $R_{23} = 49.9\text{k}\Omega$, $R_{24} = 22\text{k}\Omega$, $R_{17} = 470\Omega$

The schematic for this controller configuration is depicted in **Figure 16**.

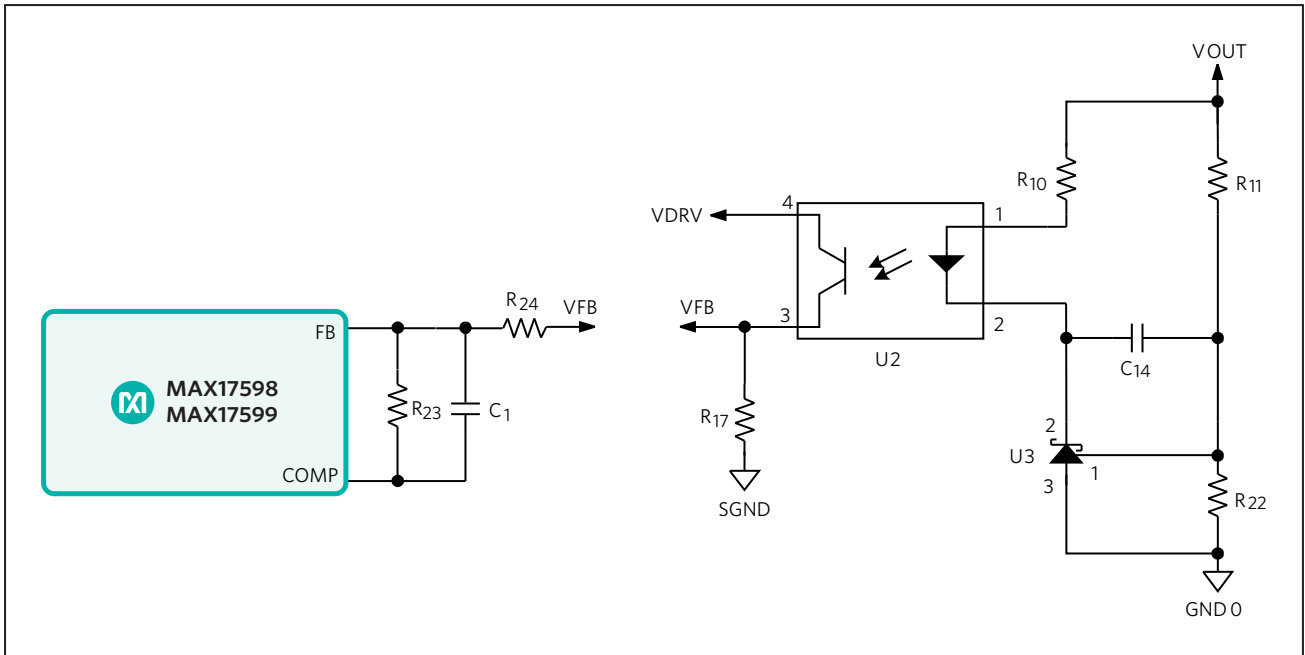


Figure 16. Controller configuration 3.

16. Thermal Considerations

Power losses occur in the device due to gate-switching currents that need to be delivered to the external MOSFETs, and due to the quiescent current consumed by the device for internal circuit operation.

If V_{DC} is directly used to power V_{IN} , calculate the approximate MAX17598/MAX17599 IC losses as follows:

$$P_{IN_LDO} = [(Q_{GATE} \times f_{SW}) + 0.003] \times V_{DCMAX} \text{ Watt}$$

If V_{BIAS} is used to power the V_{IN} , use the following equation to calculate the approximate MAX17598 IC losses:

$$P_{IN_LDO} = [(Q_{GATE} \times f_{SW}) + 0.003] \times V_{BIAS_MAX}$$

where:

Q_{Gate} = Total gate charge of N3 and P1

V_{BIAS_MAX} = Maximum Bias voltage

V_{DCMAX} = Maximum input DC bus voltage

Estimate the MAX17598/MAX17599 junction temperature using the following equation and ensure that this value does not exceed 125°C:

$$T_J = [P_{IN_LDO} \times Rth_{JA}] + T_A$$

18. Design Example: Active-Clamp Forward Converter Using the MAX17598

Technical Specifications

Input voltage range: 36 VDC to 72 VDC

Output voltage: 3.3V

Rated output current: 8A

Switching frequency: 350kHz

a. Transformer Turns Ratio Selection (k)

The maximum duty cycle is assumed to be 0.46 in the present EV kit configuration.

$$k = \frac{V_{OUT}}{V_{DCMIN} \times D_{MAX}} = 0.2$$

where $V_{DCMIN} = 36V$, $D_{MAX} = 0.46$, $V_{OUT} = 3.3V$

$$D_{MIN} = \frac{V_{OUT}}{V_{DCMAX} \times k} = 0.229$$

$$D_{TYP} = \frac{V_{OUT}}{V_{DCTYP} \times k} = 0.3438$$

b. Secondary Inductor Selection (L2)

$$L_2 = \frac{V_{OUT} \times (1 - D_{MIN})}{I_{OUT} \times \% \Delta I_{SEC} \times f_{SW}} = 15 \mu H$$

where $\% \Delta I_{SEC} = 0.6$.

$$\Delta I_{SEC,MIN} = \frac{V_{OUT} \times (1 - D_{MAX})}{L_{OUT} \times f_{SW}} = 3.4A$$

$$\Delta I_{SEC,MAX} = \frac{V_{OUT} \times (1 - D_{MIN})}{L_{OUT} \times f_{SW}} = 4.85A$$

$$I_{SEC,PEAK} = I_{OUT} + \frac{\Delta I_{SEC,MAX}}{2} = 10.43A$$

c. Magnetizing Inductance Calculation

$$\Delta I_{MAG} = \frac{\Delta I_{SEC,MIN} \times k}{2} = 0.34A$$

$$L_{MAG} = \frac{V_{DCMAX} \times D_{MIN}}{\Delta I_{MAG} \times f_{SW}} = 138.6 \mu H$$

Selected value of magnetizing inductance, $L_{MAG} = 100 \mu H$.

$$\Delta I_{MAG} = \frac{V_{DCMAX} \times D_{MIN}}{L_{MAG} \times f_{SW}} = 0.471 A$$

$$I_{PRI,PEAK} = I_{SEC,PEAK} \times k + \frac{\Delta I_{MAG}}{2} = 2.32 A$$

d. Sense Resistor Selection

$$R_{21} = \frac{0.305}{1.2 \times I_{PRI,PEAK}} = 0.1 \Omega$$

e. BOOST Capacitor Selection

$$C_{10} = \frac{\Delta I_{MAG} \times (1 - D_{MIN})^2}{8 \times 0.2 \times V_{DCMAX} \times f_{SW}} = 6.9 nF$$

$$\text{Minimum } V_{C_{10}} = 1.4 \times \frac{V_{DCMAX}}{1 - D_{MIN}} = 130 V$$

f. Input Capacitor Selection

Efficiency of the converter, $\eta = 0.92$

$$I_{IN,AVG} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{DCMIN}} = 0.797 A$$

$$\Delta V_{IN,RIPPLE} = 0.02 \times V_{DCMIN}$$

$$C_3 = \frac{I_{IN,AVG} \times (1 - D_{MAX})}{\Delta V_{DC,RIPPLE} \times f_{SW}} = 1.7 \mu F$$

The 22 μ F electrolytic capacitor is used in parallel with 2.2 μ F ceramic capacitor.

g. Output Capacitor Selection

$$f_R = \frac{1 - D_{MAX}}{2 \times \pi \times \sqrt{L_{MAG} \times C_{10}}} = 103.5 kHz$$

$$f_c = \frac{f_R}{5} = 20.7 \text{kHz}$$

Choose, $f_c = 10 \text{kHz}$

$$t_{\text{RESPONSE}} \cong \left(\frac{0.33}{f_c} + \frac{1}{f_{\text{SW}}} \right) = 36.19 \mu\text{s}$$

Choose I_{STEP} equal to 25% of output current, $I_{\text{STEP}} = 2\text{A}$, $\Delta V_{\text{OUT}} = 3\%$ of output voltage, which is equal to 99mV.

$$C_{\text{OUT}} = \frac{I_{\text{STEP}} \times t_{\text{RESPONSE}}}{2 \times \Delta V_{\text{OUT}}} = 366 \mu\text{F}$$

Output capacitance chosen after derating, $C_{\text{OUT}} = 400 \mu\text{F}$.

$$I_{\text{COUT,RMS}} = \frac{\Delta I_{\text{SEC,MAX}}}{2 \times \sqrt{3}} = 1.4\text{A}$$

$$\Delta V_{\text{COUT}} = \frac{\Delta I_{\text{SEC,MAX}}}{8 \times C_{\text{CERAMIC}} \times f_{\text{SW}}} = 23\text{mV}$$

where C_{CERAMIC} is the total ceramic capacitance used at the output excluding the electrolytic/tantalum capacitance. This is due to the assumption that the polarized capacitor offers high impedance to the switching ripple compared to the total impedance offered by ceramic capacitance.

In this design, 2 x 47 μF ceramic capacitors are used. Considering 20% derating of the ceramic capacitors, the total ceramic output capacitance would be $C_{\text{CERAMIC}} = 2 \times 47 \mu\text{F} \times 0.8 = 75.2 \mu\text{F}$.

h. Primary n-MOSFET Selection

$$V_{\text{DS,N3}} = \frac{V_{\text{INMAX}}}{1 - D_{\text{MIN}}} = 93.38\text{V}$$

$$\Delta I = \Delta I_{\text{SEC,MIN}} \times k + \Delta I_{\text{MAG}} = 1.15\text{A}$$

$$I_{\text{IN,TON}} = \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{\eta \times V_{\text{DCMIN}} \times D_{\text{MAX}}} = 1.73\text{A}$$

$$I_{\text{RMS,N3}} = I_{\text{IN,TON}} \times \sqrt{D_{\text{MAX}}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I}{I_{\text{IN,TON}}} \right)^2} = 1.2\text{A}$$

i. Primary p-MOSFET Selection

$$V_{DS,P1} = \frac{V_{DCMAX}}{1 - D_{MIN}} = 93.38V$$

$$I_{RMS,P1} = \Delta I_{MAG} \times \sqrt{\frac{1 - D_{MIN}}{12}} = 0.12A$$

j. p-FET Gate-Drive Circuit for Low-Side Active-Clamp Configuration

$$C_{11} = 47nF$$

$$R_{14} = \frac{100}{C_{11} \times f_{SW}} = 12k\Omega$$

$$R_9 = 0\Omega$$

k. Secondary Rectifier Selection

In this design, self-driven synchronous MOSFETs are used for secondary rectification.

$$V_{DS,N2} = k \times \frac{V_{DCMIN} \times D_{MAX}}{1 - D_{MAX}} = 6.1V$$

$$I_{RMS,N2} = I_{OUT} \times \sqrt{D_{MAX}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{SEC,MIN}}{I_{OUT}} \right)^2} = 5.47A$$

$$V_{DS,N1} = k \times V_{DCMAX} = 14.4V$$

$$I_{RMS,N1} = I_{OUT} \times \sqrt{1 - D_{MIN}} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{SEC,MAX}}{I_{OUT}} \right)^2} = 7.13A$$

l. SLOPE compensation

$$S_E = \left(0.82 \times \frac{V_{OUT}}{L_2} \times k - \frac{V_{DCMIN}}{L_{MAG}} \right) \times R_{21} \times 10^3 = 0.08 \frac{mV}{\mu s}$$

Since S_E is less than $50 \frac{mV}{\mu s}$, SLOPE resistor is left OPEN.

m. BIAS Winding Turns Ratio Selection ($K_B = N_B/N_P$)

$$K_B = \frac{V_{BIAS}}{D_{MAX} \times V_{DCMIN}} = 0.725$$

where $V_{BIAS} = 12V$.

n. BIAS Inductor (L_{BIAS}) Selection

$$L_1 = \frac{V_{BIAS} \times (1 - D_{MIN})}{0.003 \times f_{SW}} = 8.8mH$$

Selected value of bias inductor is 10mH.

o. Bias Capacitor (C_{START}) Calculation

$$C_7 = 0.09 \times \left[7.4 \times C_{VDRV} + 0.04 \times I_{IN} \times C_{SS} + \left(I_{IN} + \frac{Q_{GATE} \times f_{SW}}{10^6} \right) \times t_{SS} \right] = 5.2\mu F$$

where $C_{VDRV} = 1.47\mu F$, $I_{IN} = 2mA$, $C_{SS} = 100nF$, $t_{SS} = 5ms$, $Q_{GATE} = 16.6nC$.

p. Compensator Design

For compensator design, choose $R_{23} = 49.9k\Omega$, $R_{24} = 22k\Omega$, $R_{17} = 470\Omega$, $CTR = 1$.

$$R_{10} = 400 \times CTR \times (V_{OUT} - 2.7) = 240\Omega$$

$$S_e = 50 \times 10^3 + \frac{V_{DCTYP} \times R_{21}}{L_{MAG}} = 98,000$$

$$S_n = k \times R_{21} \times \left(\frac{k \times V_{DCTYP} - V_{OUT}}{L_{OUT}} \right) = 84,000$$

where $V_{INTYP} = 48V$

$$m = 1 + \frac{S_e}{S_n} = 2.167$$

$$G_{DC} = \frac{V_{OUT}}{2 \times k \times I_{OUT} \times R_{21}} \times \frac{1}{1 + \frac{V_{OUT}}{I_{OUT} \times L_2 \times f_{SW}} \times (m \times (1 - D_{TYP}) - 0.5)} = 5.98$$

$$F_P = \frac{1}{2\pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} + \frac{(m \times (1 - D_{TYP}) - 0.5)}{2\pi \times L_{OUT} \times C_{OUT} \times f_{SW}} = 1.66kHz$$

$$F_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} = 44.2kHz$$

where R_{ESR} for the selected tantalum capacitor is $9m\Omega$.

$$G_{PLANT} = G_{DC} \times \frac{\sqrt{1 + \left(\frac{f_C}{f_Z}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_P}\right)^2}} = 1$$

$$G_{PLANT} \times CTR \times \frac{R_{17}}{R_{10}} \times \frac{R_{23}}{R_{24}} = 4.44$$

Since loop gain is greater than 1.2, second configuration shown in the isolated compensation design should be used for this application.

$$R_6 = \frac{R_{23}}{\left(\frac{G_{\text{PLANT}} \times \text{CTR} \times R_{17} \times R_{23}}{R_{10} \times R_{24}} - 1 \right)} = 14.5\text{k}\Omega$$

$$C_{19} = \frac{10}{\pi \times R_6 \times f_c} = 22\text{nF}$$

$$C_1 = \frac{(R_{23} + R_6)}{\pi \times R_{23} \times f_{\text{SW}} \times R_6} = 80\text{pF}$$

$$C_{14} = \frac{1}{2\pi \times R_{11} \times f_p} = 1.9\text{nF}$$

where R_{11} is the top resistor in the potential divider circuit at the output, $R_{11} = 49.9\text{k}\Omega$.

19. Bill of Materials

Designation	Qty	Description
C1	1	100pF ±20%, 25V X7R ceramic capacitor (0603) AVX 06033C101MAT2A
C2	1	22µF ±20%, 100V aluminum electrolytic capacitor (8mm diameter) Panasonic EEEFK2A220P
C3	1	2.2µF ±10%, 100V X7R ceramic capacitor (1210) Murata GRM32ER72A225K
C4	1	330µF ±20%, 6.3V aluminum electrolytic capacitor (7.3mm x 4.3mm x 2.8mm) SANYO 6TPF330M9L
C5, C6	2	47µF ±10%, 6.3V X7R ceramic capacitors (1210) Murata GCM32ER70J476K
C7, C20	2	4.7µF ±10%, 50V X7R ceramic capacitors (1206) Murata GRM31CR71H475K
C8, C18	2	0.47µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E474K
C9	1	1µF ±10%, 25V X7R ceramic capacitor (0805) Murata GRM219R71E105K
C10	1	22nF ±10%, 250V X7R ceramic capacitor (0805) TDK C2012X7R2E223K
C11	1	0.047µF ±10%, 25V X7R ceramic capacitor (0603) Murata GRM188R71E473K
C12	0	SHORT (PC TRACE)
C13, C17	0	Not installed capacitors (0603)
C14	1	2.2nF ±10%, 50V X7R ceramic capacitor (0603) TDK C1608X7R1H222K
C15	1	1nF ±10%, 25V X7R ceramic capacitor (0603) Murata GRM188R71E102K

C16	1	0.1 μ F \pm 10%, 16V X7R ceramic capacitor (0603) Murata GRM188R71C104K
C19	1	33nF \pm 10%, 25V X7R ceramic capacitor (0603) Murata GRM188R71E333K
D1-D4	4	100V, 300mA fast switching diodes (SOD-123) Diodes Inc. 1N4148W-7-F
L1	1	10mH, 20mA inductor (6.6mm x 4.45mm) API Delevan SDS680R-106M
L2	1	1.5 μ H, 16.8A inductor Coil Craft SER1410-152ME
N1, N2	2	25V, 58A n-channel MOSFETs (PG-TDSON-8) Infineon BSC050NE2LS
N3	1	150V, 4.1A n-channel MOSFET (SO-8) Fairchild FDS86242
P1	1	-150V, -530mA p-channel MOSFET (SOT23-3) Vishay Siliconix Si2325DS-T1-GE3
R1	1	221k Ω \pm 1% resistor (0805)
R2, R3, R9, R12	4	0 Ω \pm 5% resistors (0603)
R4	1	24.9k Ω \pm 1% resistor (0603)
R5	1	1.6M Ω \pm 1% resistor (0805)
R6, R13	2	10k Ω \pm 1% resistors (0603)
R7	1	35.7k Ω \pm 1% resistor (0603)
R8	1	20k Ω \pm 1% resistor (0603)
R10	1	221 Ω \pm 1% resistor (0603)
R11, R23	2	49.9k Ω \pm 1% resistors (0603)
R14	1	10k Ω \pm 1% resistor (0603)
R15, R16, R20	0	Not installed resistors (0603)
R17	1	470 Ω \pm 1% resistor (0603)
R18	1	28.7k Ω \pm 1% resistor (0603)
R19	1	100 Ω \pm 1% resistor (0603)
R21	1	0.1 Ω \pm 1% resistor (1206) Panasonic ERJ-8BWFR100V
R22	1	30k Ω \pm 1% resistor (0603)
R24	1	22k Ω \pm 1% resistor (0603)
T1	1	100 μ H, 1.5A 1:0.2:0.7 transformer (EFD20) Coil Craft MA5638-BL
U1	1	Peak current mode, active-clamped forward PWM controller (16-pin TQFN 3mm x 3mm x 0.8mm) Maxim MAX17598ATE+
U2	1	Phototransistor (4-pin, SO) Avago ACPL-217-56AE
U3	1	Shunt regulator 1.24V \pm 0.5% (SOT23-3) Diodes Inc. TLV431BFTA

NOTE:

1. The design methodology for active-clamp forward converter using MAX17599 is same as the MAX17598.
2. To evaluate the above design order the [MAX17598EVKIT](#)