PCN Number:	20180413002	PCN Date:	April 16, 2018
Title:	Datasheet for DP83822HF, DP83822IF, DP83822H, DP83822I		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DP83822HF, DP83822IF, DP83822H, DP83822I

SNLS505C – AUGUST 2016 – REVISED APRIL 2018

Changes from Revision B (March 2018) to Revision C — **Page**

- Changed TX_D[1:0] back to TX_D[3:0] 29
- Changed RX_D[1:0] back to RX_D[3:0] 29

Changes from Revision A (August 2016) to Revision B — **Page**

- Updated data sheet text and format to the latest TI documentation and translations standards 1
- Updated description of pin 24 and changed pin type from: I/O, PD to: I/O 6
- Added *MII: 100BASE-TX Transmit Latency Timing* table 14
- Added *MII: 100BASE-TX Receive Latency Timing* table 14
- Device Power-Up Timing diagram modified to include start voltage limits 15
- Added the *100BASE-TX Transmit Latency Timing* graphic 22
- Added the *100BASE-TX Receive Latency Timing* graphic 22
- Changed the *Functional Block Diagram* 25
- Changed TX_D[3:0] to TX_D[1:0] 29
- Changed RX_D[3:0] to RX_D[1:0] 29
- Added note to the *100BASE-FX Receive* section and changed the SD_DIS pin to SD_EN 40
- Changed RX_ER strap function from: AMDIX_EN (SD_DIS) to: AMDIX_EN (SD_EN) 48
- Changed the default and switched 0 and 1 functions for the RMII Recovered Clock Async FIFO Bypass bit in RCSR register (0X0017) 64
- Changed the 0x7D BIST IPG length from: 125 bytes to: 500 bytes 67
- Added 0 and 1 functions for the MLED Polarity Swap bit in the MLEDCR register (0x0025) 68
- Added Line Driver Class Selection (LDCSEL) register 75
- Changed 0x0465 register from: General Configuration to: Fiber General Configuration and switched the Active HIGH and LOW polarities for 1 and 0 78
- Changed the 100Base-FX Signal Detect Polarity bit description note 78
- Changed Pattern Start Point bit default from: 0 to: 01100 86
- Added the *Detailed Design Procedure* section for the TPI Network Circuit typical application 90
- Added note to the *Oscillator* section 92
- Changed the *Power Connections* graphic 95

The datasheet number will be changing.

Device Family	Change From:	Change To:
DP83822HF, DP83822IF, DP83822H, DP83822I	SNLS505A	SNLS505C

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DP83822HF

Reason for Change:

To accurately reflect device characteristics.
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):
No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.
Changes to product identification resulting from this PCN:
None.
Product Affected:

DP83822HFRHBR	DP83822HFRHBT	DP83822HRHBR	DP83822HRHBT
DP83822IFRHBR	DP83822IFRHBT	DP83822IRHBR	DP83822IRHBT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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