

## SNx5HVD1176 PROFIBUS® RS-485 Transceivers

### 1 Features

- Optimized for PROFIBUS® Networks
  - Signaling Rates up to 40 Mbps
  - Differential Output Exceeds 2.1 V (54-Ω Load)
  - Low Bus Capacitance of 10 pF (Max)
- Meets the Requirements of TIA/EIA-485-A
- ESD Protection Exceeds ±10-kV HBM
- Fail-Safe Receiver for Bus Open, Short, Idle
- Up to 160 Transceivers on a Bus
- Low Skew During Output Transitions and Driver Enabling and Disabling
- Common-Mode Rejection up to 50 MHz
- Short-Circuit Current Limit
- Hot Swap Capable
- Thermal Shutdown Protection

### 2 Applications

- Process Automation
  - Chemical Production
  - Brewing and Distillation
  - Paper Mills
- Factory Automation
  - Automobile Production
  - Rolling, Pressing, Stamping Machines
  - Networked Sensors
- General RS-485 Networks
  - Motor and Motion Control
  - HVAC and Building Automation Networks
  - Networked Security Stations

### 3 Description

The SNx5HVD1176 devices are half-duplex differential transceivers with characteristics optimized for use in PROFIBUS (EN 50170) applications. The driver output differential voltage exceeds the PROFIBUS requirements of 2.1 V with a 54-Ω load. A signaling rate of up to 40 Mbps allows technology growth to high data-transfer speeds. The low bus capacitance provides low signal distortion.

The SN65HVD1176 and SN75HVD1176 devices meet or exceed the requirements of ANSI standard TIA/EIA-485-A (RS-485) for differential data transmission across twisted-pair networks. The driver outputs and receiver inputs are tied together to form a half-duplex bus port with one-fifth unit load, which allows up to 160 nodes on a single bus. The receiver output stays at logic high when the bus lines are shorted, left open, or when no driver is active. The driver outputs are in high impedance when the supply voltage is below 2.5 V to prevent bus disturbance during power cycling or during live insertion to the bus. An internal current limit protects the transceiver bus pins in short-circuit fault conditions by limiting the output current to a constant value. Thermal shutdown circuitry protects the device against damage due to excessive power dissipation caused by faulty loading and drive conditions.

The SN75HVD1176 device is characterized for operation at temperatures from 0°C to 70°C. The SN65HVD1176 device is characterized for operation at temperatures from –40°C to 85°C.

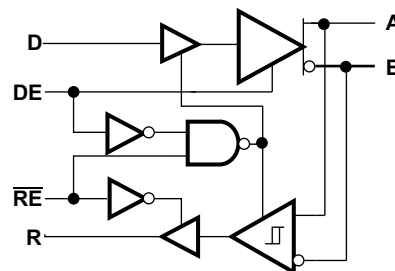
For an isolated version of this device, see the ISO1176 device ([SLLS897](#)) with integrated digital isolators.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1176 SN75HVD1176	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description .....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>16</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>18</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information .....	<b>18</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.2 Typical Application .....	<b>18</b>
<b>6 Specifications</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>22</b>
6.1 Absolute Maximum Ratings .....	<b>3</b>	<b>11 Layout</b> .....	<b>22</b>
6.2 ESD Ratings .....	<b>3</b>	11.1 Layout Guidelines .....	<b>22</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	11.2 Layout Example .....	<b>22</b>
6.4 Thermal Information .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>23</b>
6.5 Electrical Characteristics .....	<b>5</b>	12.1 Third-Party Products Disclaimer .....	<b>23</b>
6.6 Supply Current .....	<b>6</b>	12.2 Documentation Support .....	<b>23</b>
6.7 Power Dissipation .....	<b>6</b>	12.3 Related Links .....	<b>23</b>
6.8 Switching Characteristics .....	<b>6</b>	12.4 Community Resources .....	<b>23</b>
6.9 Typical Characteristics .....	<b>9</b>	12.5 Trademarks .....	<b>23</b>
<b>7 Parameter Measurement Information</b> .....	<b>10</b>	12.6 Electrostatic Discharge Caution .....	<b>23</b>
<b>8 Detailed Description</b> .....	<b>16</b>	12.7 Glossary .....	<b>23</b>
8.1 Overview .....	<b>16</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>23</b>
8.2 Functional Block Diagram .....	<b>16</b>		

## 4 Revision History

<b>Changes from Revision G (June 2015) to Revision H</b>	<b>Page</b>
• Changed $V_{ID} \geq 0.02\text{ V}$ To: $V_{ID} \geq -0.02\text{ V}$ in <a href="#">Table 2</a> .....	<b>17</b>

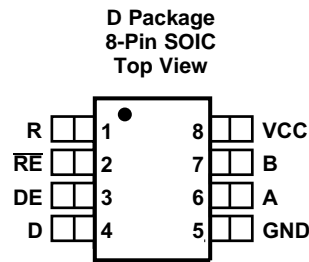
  

<b>Changes from Revision F (June 2013) to Revision G</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Power Dissipation</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Added storage temperature to the <i>Absolute Maximum Ratings</i> table .....	<b>3</b>
• Added Psi JT and Psi JB values to the <i>Thermal Information</i> table .....	<b>4</b>
• Deleted redundant $I_{O(OFF)}$ and $I_{OZ}$ lines from the <i>Electrical Characteristics</i> table .....	<b>5</b>
• Deleted redundant $C_{OD}$ line from the <i>Electrical Characteristics</i> table .....	<b>5</b>

<b>Changes from Revision E (August 2008) to Revision F</b>	<b>Page</b>
• Changed RE to $\overline{RE}$ in the pinout and Logic Diagram .....	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output/receiver input (complementary to B)
B	7	Bus input/output	Driver output/receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
VCC	8	Supply	3-V to 5.5-V supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating junction temperature range unless otherwise noted<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(2)</sup>	-0.5	7	V
	Voltage at any bus I/O terminal	-9	14	V
	Voltage input, transient pulse, A and B, (through 100 $\Omega$ , see <a href="#">Figure 20</a> )	-40	40	V
	Voltage input at any D, DE or $\overline{RE}$ terminal	-0.5	7	V
$I_O$	Receiver output current	-10	10	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-40	130	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Bus terminals and GND	±10000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V	
	Voltage at either bus I/O terminal	A, B		-7	12	V
V <sub>IH</sub>	High-level input voltage	D, DE, $\overline{RE}$		2	V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage			0	0.8	V
V <sub>IL</sub>	Differential input voltage	A with respect to B		-12	12	V
I <sub>O</sub>	Output current	Driver		-70	70	mA
		Receiver		-8	8	mA
T <sub>J</sub>	Junction temperature <sup>(1)</sup>	SN65HVD1176		-40	130	°C
		SN75HVD1176		0	130	°C
R <sub>L</sub>	Differential load resistance			54		Ω
1/t <sub>U1</sub>	Signaling rate				40	Mbps

(1) See the [Power Dissipation](#) table for more information on maintenance of this requirement.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65HVD1176, SN75HVD1176		UNIT	
		D (SOIC)			
		8 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	Low-K board <sup>(3)</sup> , no air flow		208.3	°C/W
		High-K board <sup>(4)</sup> , no air flow		104.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance			45.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	High-K board		45.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter			5.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter			45.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The intent of R<sub>θJA</sub> specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
- (3) JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
- (4) JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.

## 6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DRIVER</b>							
$V_O$	Open-circuit output voltage	A or B	No load	0		$V_{CC}$	V
$ V_{OD(SS)} $	Steady-state differential output voltage magnitude	$R_L = 54 \Omega$	See Figure 6	2.1	2.9		V
		With common-mode loading, ( $V_{TEST}$ from $-7$ V to $12$ V) See Figure 7		2.1	2.7		V
$\Delta V_{OD(SS)} $	Change in steady-state differential output voltage between logic states	See Figure 6 and Figure 11		-0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 10		2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See Figure 10		-0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 10			0.5		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	$R_L = 54 \Omega$ , $C_L = 50$ pF See Figure 11				10%	$V_{OD(PP)}$
$I_I$	Input current	D, DE		-50		50	$\mu$ A
$I_{OS(P)}$	Peak short-circuit output current	DE at $V_{CC}$ , See Figure 13	$V_{OS} = -7$ V to $12$ V	-250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current	DE at $V_{CC}$ , See Figure 13	$V_{OS} > 4$ V, Output driving low	60	90	135	mA
			$V_{OS} < 1$ V, Output driving high	-135	-90	-60	mA
<b>RECEIVER</b>							
$V_{IT(+)}$	Positive-going differential input voltage threshold	See Figure 14	$V_O = 2.4$ V, $I_O = -8$ mA		-80	-20	mV
$V_{IT(-)}$	Negative-going differential input voltage threshold		$V_O = 0.4$ V, $I_O = 8$ mA	-200	-120		mV
$V_{HYS}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				40		mV
$V_{OH}$	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA, See Figure 14		4	4.6		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA, See Figure 14			0.2	0.4	V
$I_A, I_B$	Bus pin input current	$V_I = -7$ V to $12$ V, Other input = $0$ V	$V_{CC} = 4.75$ V to $5.25$ V	-160		200	$\mu$ A
$I_{A(OFF)}, I_{B(OFF)}$			$V_{CC} = 0$ V	-160		200	
$I_I$	Receiver enable input current	$\overline{RE}$		-50		50	$\mu$ A
$I_{OZ}$	High-impedance - state output current	$\overline{RE} = V_{CC}$		-1		1	$\mu$ A
$R_I$	Input resistance			60			k $\Omega$
$C_{ID}$	Differential input capacitance	Test input signal is a 1.5-MHz sine wave with amplitude $1 V_{PP}$ , capacitance measured across A and B			7	10	pF
$C_{MR}$	Common mode rejection	See Figure 16			4		V

(1) All typical values are at  $V_{CC} = 5$  V and  $25^\circ\text{C}$ .

## 6.6 Supply Current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Supply Current <sup>(1)</sup>	Driver and receiver, $\overline{RE}$ at 0 V, DE at V <sub>CC</sub> , All other inputs open, no load		4	6	mA
		Driver only, $\overline{RE}$ at V <sub>CC</sub> , DE at V <sub>CC</sub> , All other inputs open, no load		3.8	6	mA
		Receiver only, $\overline{RE}$ at 0 V, DE at 0 V, All other inputs open, no load		3.6	6	mA
		Standby only, $\overline{RE}$ at V <sub>CC</sub> , DE at 0 V, All other inputs open		0.2	5	μA

(1) Over recommended operating conditions

## 6.7 Power Dissipation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
P <sub>D</sub>	Device power dissipation	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF, 0 V to 3 V, 15 MHz, 50% duty cycle square wave input, driver and receiver enabled		277	318	mW
T <sub>A</sub>	Ambient air temperature	SN65HVD1176	Low-K board, no air flow, P <sub>D</sub> = 318 mW	–40	64	°C
			High-K board, no air flow, P <sub>D</sub> = 318 mW	–40	89	°C
		SN75HVD1176	Low-K board, no air flow, P <sub>D</sub> = 318 mW	0		°C
			High-K board, no air flow, P <sub>D</sub> = 318 mW	0		°C
T <sub>SD</sub>	Thermal shut down junction temperature			150		°C

(1) All typical values are with V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

## 6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DRIVER</b>						
t <sub>PLH</sub>	Propagation delay time low-level-to-high-level output	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF, See <a href="#">Figure 8</a>	4	7	10	ns
t <sub>PHL</sub>	Propagation delay time high-level-to-low-level output		4	7	10	ns
t <sub>sk(p)</sub>	Pulse skew   t <sub>PLH</sub> – t <sub>PHL</sub>		0	2		ns
t <sub>r</sub>	Differential output rise time		2	3	7.5	ns
t <sub>f</sub>	Differential output fall time		2	3	7.5	ns
t <sub>t(MLH), t<sub>t(MHL)</sub></sub>	Output transition skew	See <a href="#">Figure 9</a>		0.2	1	ns
t <sub>p(AZH), t<sub>p(BZH)</sub></sub>	Propagation delay time, high-impedance-to-active output	R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF See <a href="#">Figure 12</a>	$\overline{RE}$ at 0 V	10	20	ns
t <sub>p(AZL), t<sub>p(BZL)</sub></sub>				10	20	ns
t <sub>p(AHZ), t<sub>p(BHZ)</sub></sub>	Propagation delay time, active-to- high-impedance output			0.55	1.5	ns
t <sub>p(ALZ), t<sub>p(BLZ)</sub></sub>					2.5	ns
$\frac{ t_{p(AZL)} - t_{p(BZH)} }{ t_{p(AZH)} - t_{p(BZL)} }$ $\frac{ t_{p(ALZ)} - t_{p(BHZ)} }{ t_{p(AHZ)} - t_{p(BLZ)} }$				Enable skew time		
$\frac{ t_{p(ALZ)} - t_{p(BHZ)} }{ t_{p(AHZ)} - t_{p(BLZ)} }$	Disable skew time					
t <sub>p(AZH), t<sub>p(BZH)</sub></sub>	Propagation delay time, high-impedance-to-active output (from sleep mode)	R <sub>L</sub> = 110 Ω, C <sub>L</sub> = 50 pF See <a href="#">Figure 12</a>	$\overline{RE}$ at 5 V	1	4	μs
t <sub>p(AHZ), t<sub>p(BHZ)</sub></sub>				30	50	ns
t <sub>p(ALZ), t<sub>p(BLZ)</sub></sub>	Propagation delay time, active-output-to high-impedance (to sleep mode)					
t <sub>(CFB)</sub>	Time from application of short-circuit to current foldback	See <a href="#">Figure 13</a>		0.5		μs

(1) All typical values are at V<sub>CC</sub> = 5 V and 25°C.

## Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	$T_A = 25^\circ\text{C}$ , See <a href="#">Figure 13</a>	100			$\mu\text{s}$

**Switching Characteristics (continued)**

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>RECEIVER</b>						
$t_{PLH}$	Propagation delay time, low-to-high level output	See <a href="#">Figure 15</a>		20	25	ns
$t_{PHL}$	Propagation delay time, high-to-low level output			20	25	ns
$t_{sk(p)}$	Pulse skew   $t_{PLH} - t_{PHL}$			1	2	ns
$t_r$	Receiver output voltage rise time			2	4	ns
$t_f$	Receiver output voltage fall time			2	4	ns
$t_{PZH}$	Propagation delay time, high-impedance-to-high-level output	DE at $V_{CC}$ , See <a href="#">Figure 18</a>			20	ns
$t_{PHZ}$	Propagation delay time, high-level-to-high-impedance output				20	ns
$t_{PZL}$	Propagation delay time, high-impedance-to-low-level output	DE at $V_{CC}$ , See <a href="#">Figure 19</a>			20	ns
$t_{PLZ}$	Propagation delay time, low-level-to-high-impedance output				20	ns
$t_{PZH}$	Propagation delay time, high-impedance-to-high-level output (standby to active)	DE at 0 V, See <a href="#">Figure 17</a>		1	4	$\mu$ s
$t_{PHZ}$	Propagation delay time, high-level-to-high-impedance output (active to standby)			13	20	ns
$t_{PZL}$	Propagation delay time, high-impedance-to-low-level output (standby to active)	DE at 0 V, See <a href="#">Figure 17</a>		2	4	$\mu$ s
$t_{PLZ}$	Propagation delay time, low-level-to-high-impedance output (active to standby)			13	20	ns



## 6.9 Typical Characteristics

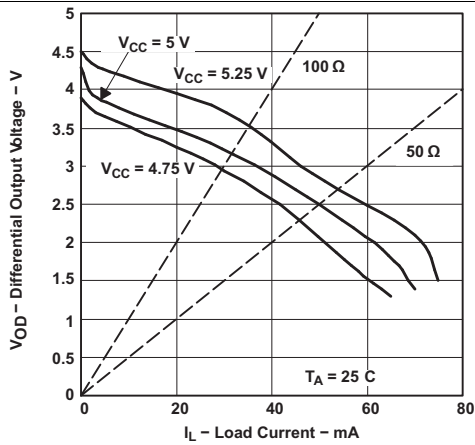


Figure 1. Differential Output Voltage vs Load Current

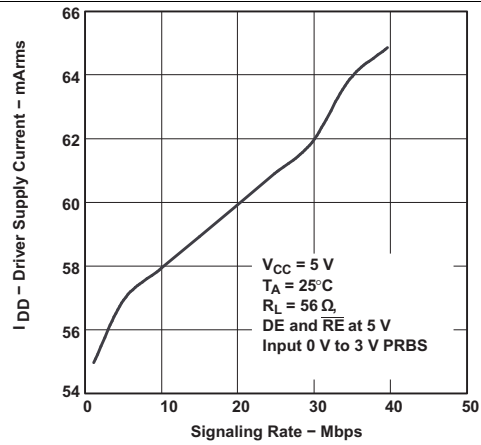


Figure 2. Driver Supply Current vs Signaling Rate

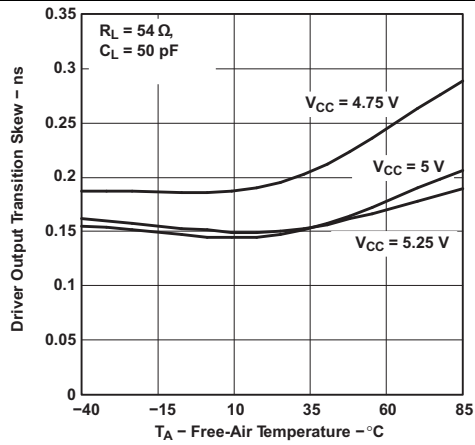


Figure 3. Driver Output Transition Skew vs Free-Air Temperature

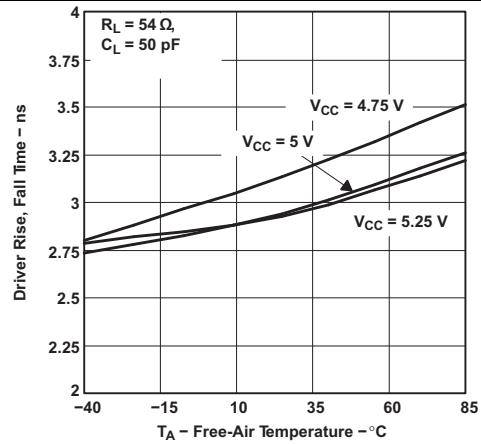


Figure 4. Driver Rise, Fall Time vs Free-Air Temperature

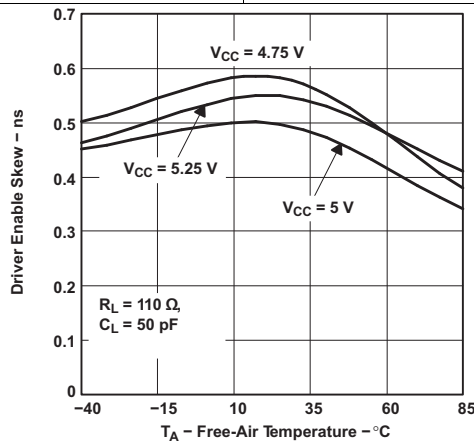


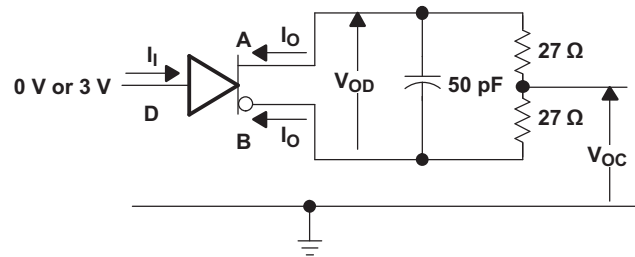
Figure 5. Driver Enable Skew vs Free-Air Temperature

## 7 Parameter Measurement Information

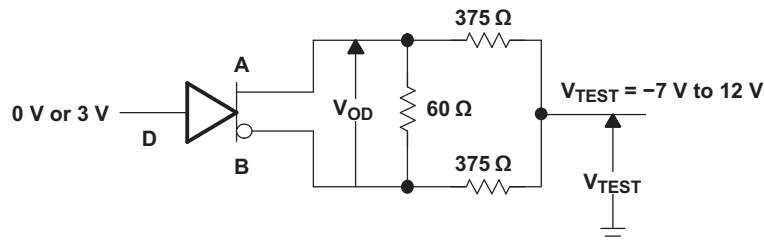
### NOTE

Test load capacitance includes probe and jig capacitance (unless otherwise specified).

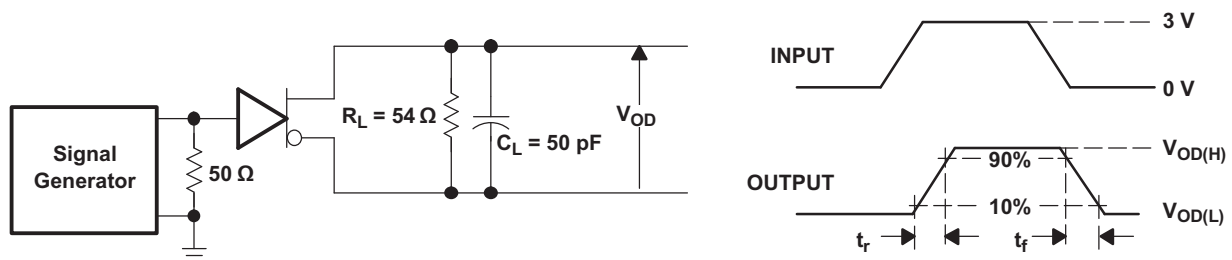
Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle,  $Z_o = 50 \Omega$  (unless otherwise specified).



**Figure 6. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$  Without Common-Mode Loading**



**Figure 7. Driver Test Circuit,  $V_{OD}$  With Common-Mode Loading**



**Figure 8. Driver Switching Test Circuit and Rise/Fall Time Measurement**

Parameter Measurement Information (continued)

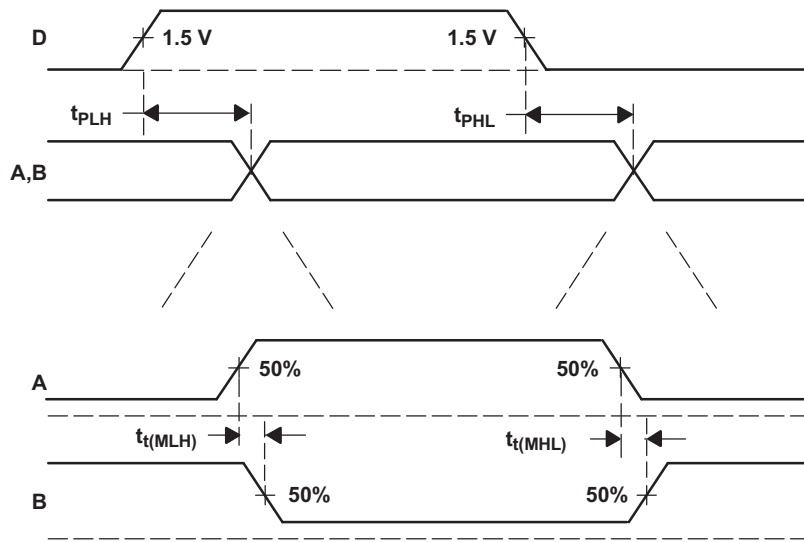


Figure 9. Driver Switching Waveforms for Propagation Delay and Output Midpoint Time Measurements

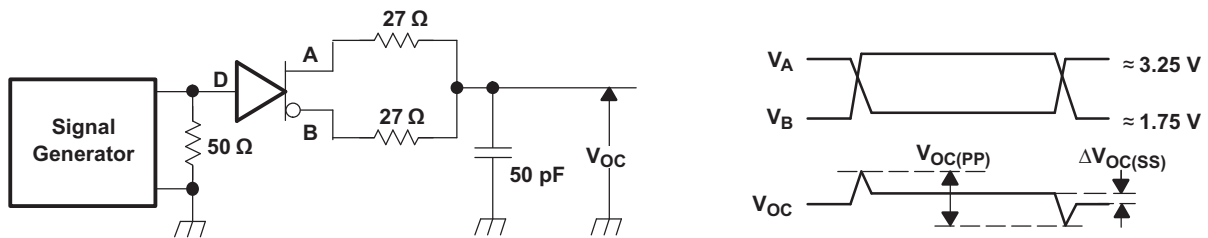
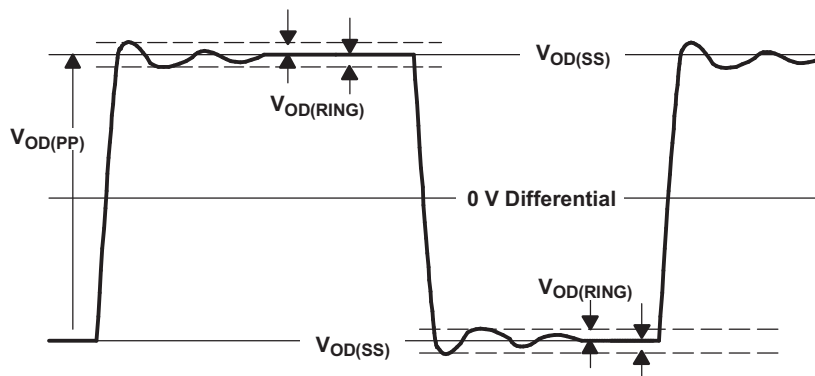


Figure 10. Driver  $V_{OC}$  Test Circuit and Waveforms



- (1)  $V_{OD(RING)}$  is measured at four points on the output waveform, corresponding to overshoot and undershoot from the  $V_{OD(H)}$  and  $V_{OD(L)}$  steady state values.

Figure 11.  $V_{OD(RING)}$  Waveform and Definitions

Parameter Measurement Information (continued)

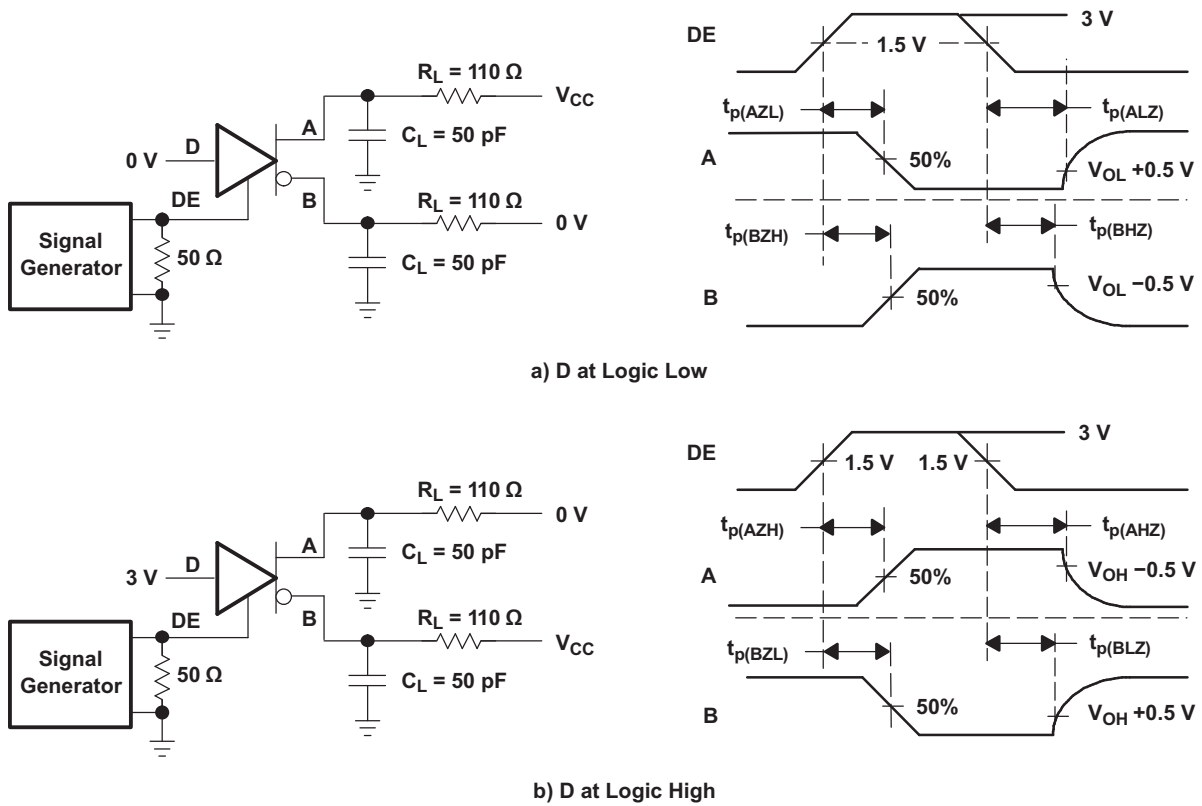


Figure 12. Driver Enable/Disable Test

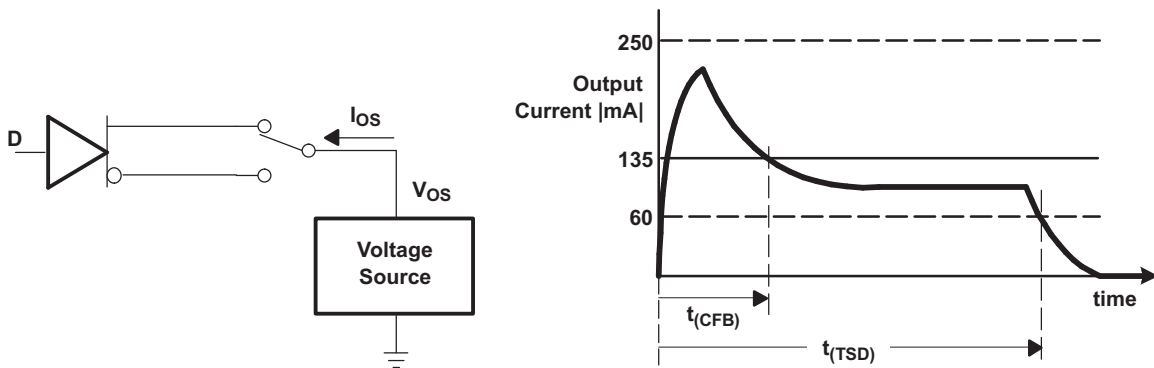


Figure 13. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time  $t = 0$ )

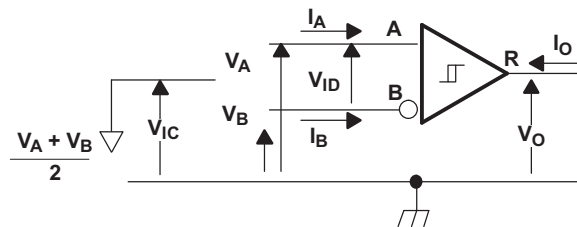


Figure 14. Receiver DC Parameter Definitions

Parameter Measurement Information (continued)

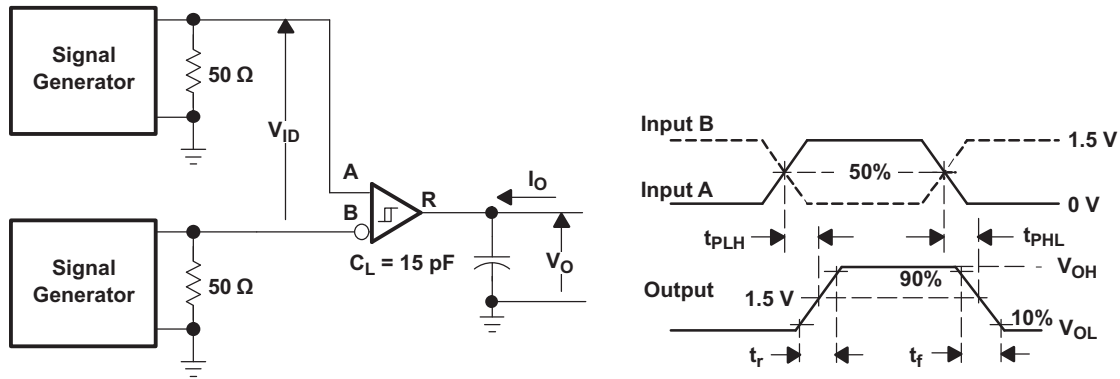


Figure 15. Receiver Switching Test Circuit and Waveforms

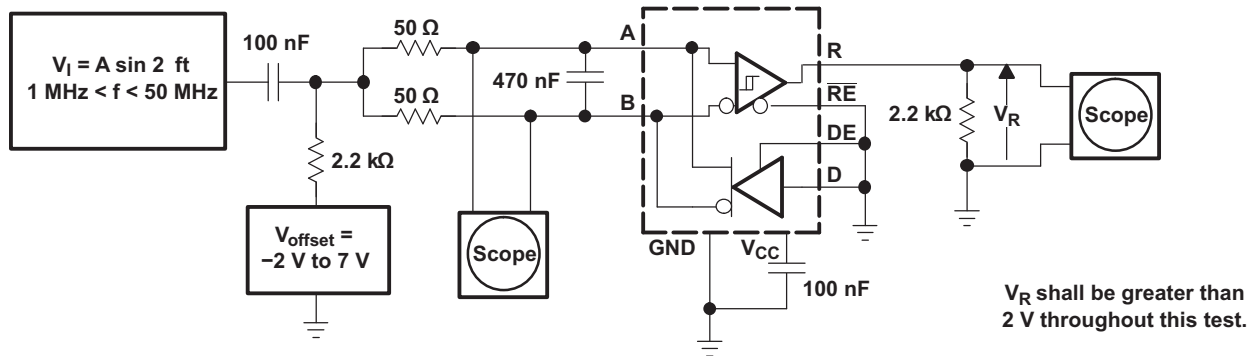


Figure 16. Receiver Common-Mode Rejection Test Circuit

Parameter Measurement Information (continued)

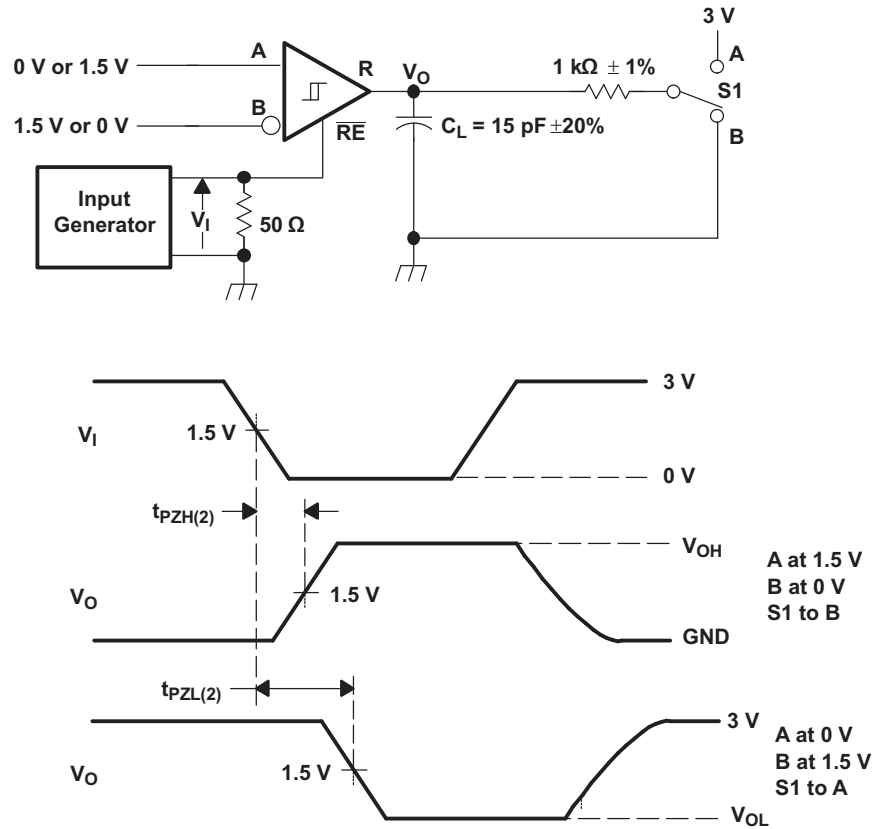


Figure 17. Receiver Enable Time From Standby (Driver Disabled)

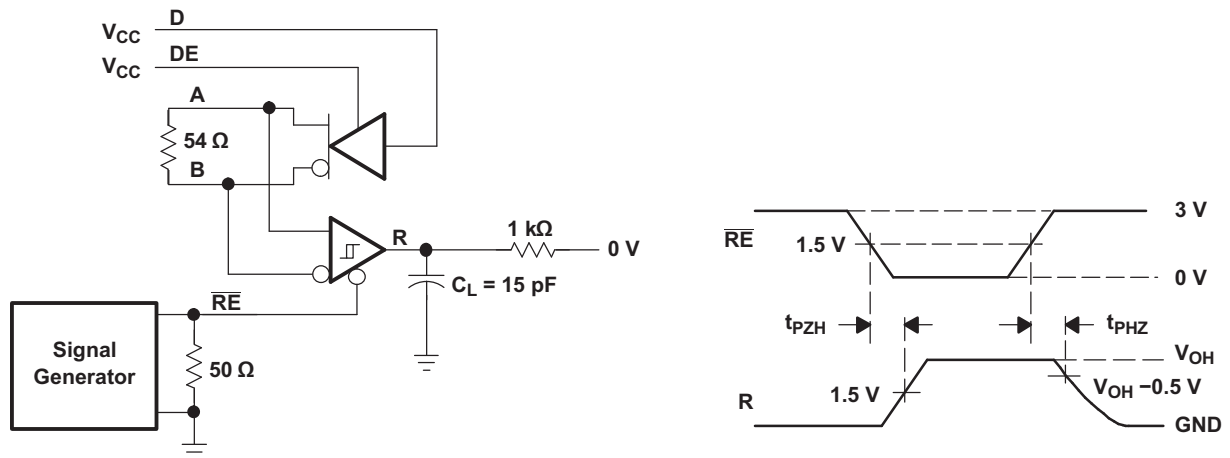


Figure 18. Receiver Enable Test Circuit and Waveforms, Data Output High (Driver Active)

Parameter Measurement Information (continued)

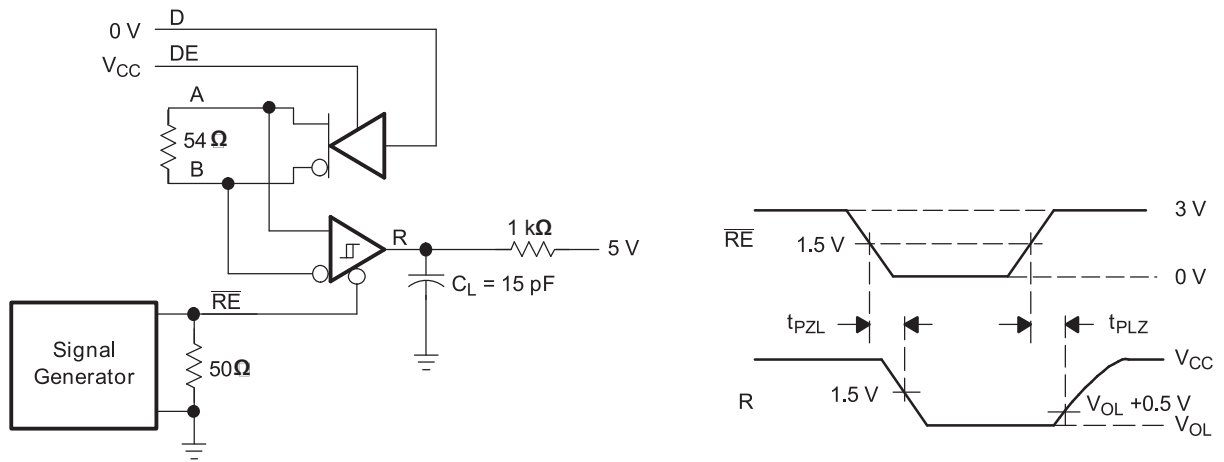


Figure 19. Receiver Enable Test Circuit and Waveforms, Data Output Low (Driver Active)

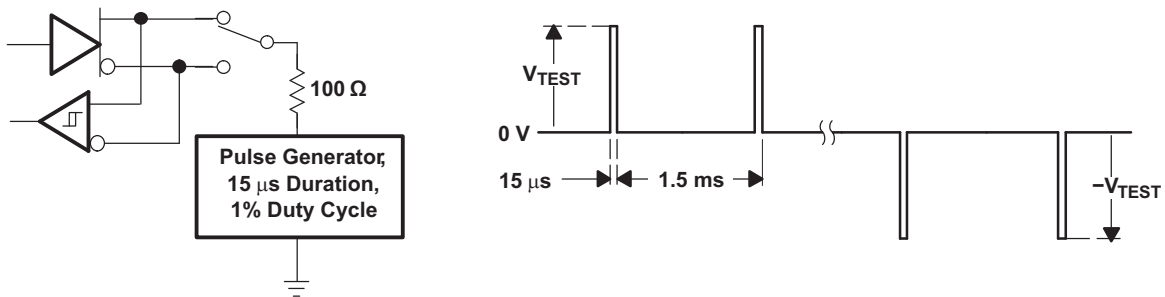


Figure 20. Test Circuit and Waveforms, Transient Overvoltage Test

## 8 Detailed Description

### 8.1 Overview

The SNx5HVD1176 device is a 5-V, half-duplex, RS-485 transceiver optimized for use in PROFIBUS (EN50170) applications and suitable for data transmission up to 40 Mbps.

The driver output differential voltage exceeds the PROFIBUS requirement of 2.1 V with a 54-Ω load, and the low transceiver output capacitance of 10 pF supports the PROFIBUS requirements for maximum bus capacitance across various data rates.

This device has an active-high driver enable and an active-low receiver enable. A standby current of less than 5 μA can be achieved by disabling both driver and receiver.

### 8.2 Functional Block Diagram

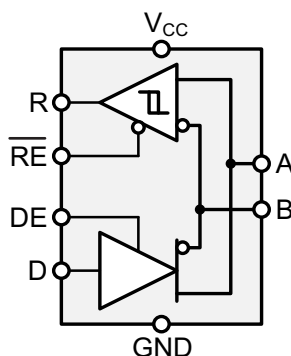


Figure 21. Logic Diagram (Positive Logic)

### 8.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±10-kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SN65HVD1176 device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 40 mV.

### 8.4 Device Functional Modes

Table 1. Driver Function Table<sup>(1)</sup>

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

(1) H = high level, L = low level, X = don't care,  
Z = high impedance (off)



Table 2. Receiver Function Table<sup>(1)</sup>

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq -0.02\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < -0.02\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
X	OPEN	Z
Open Circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, X = don't care, Z = high impedance (off), ? = indeterminate

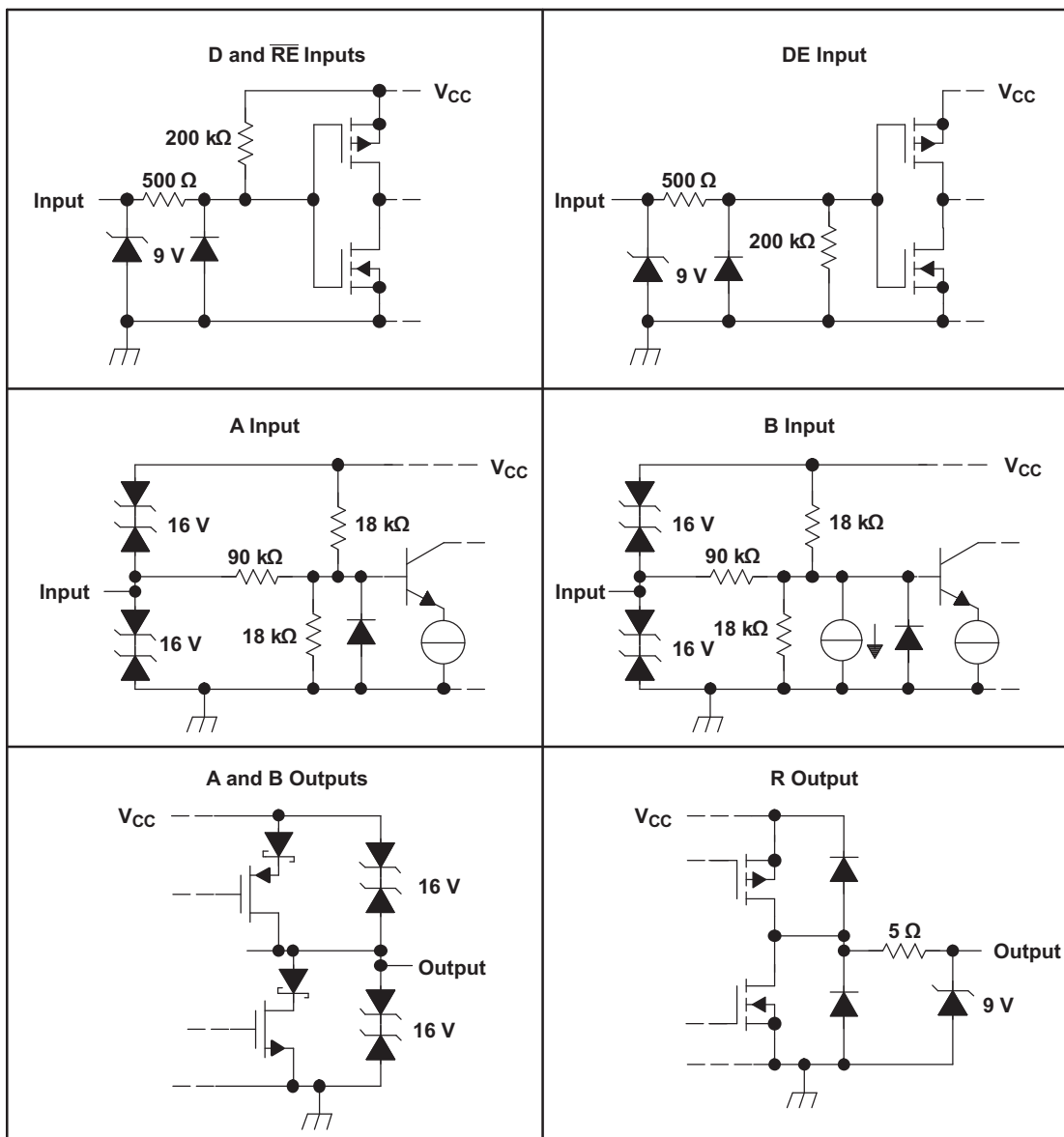


Figure 22. Equivalent Input and Output Schematic Diagrams

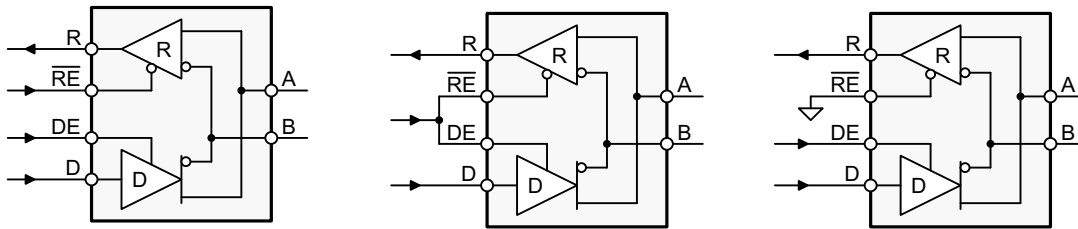
## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN65HVD1176 device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver- and receiver-enable pins allow for the configuration of different operating modes.



**Figure 23. Half-Duplex Transceiver Configurations**

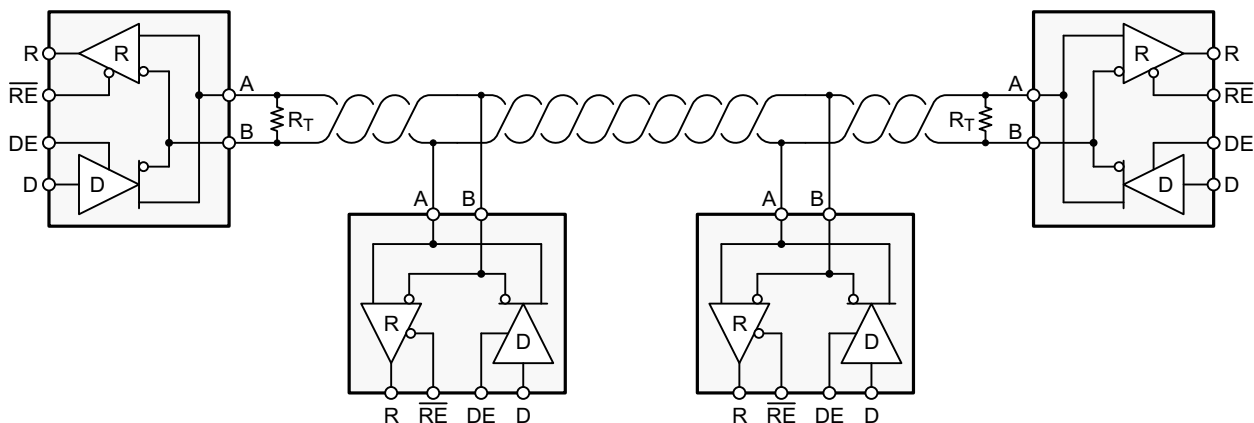
Using independent enable lines provides the most flexible control because it allows the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus and the data it sends; the node can also verify that the correct data has been transmitted.

### 9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor ( $R_T$ ) whose value matches the characteristic impedance ( $Z_0$ ) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

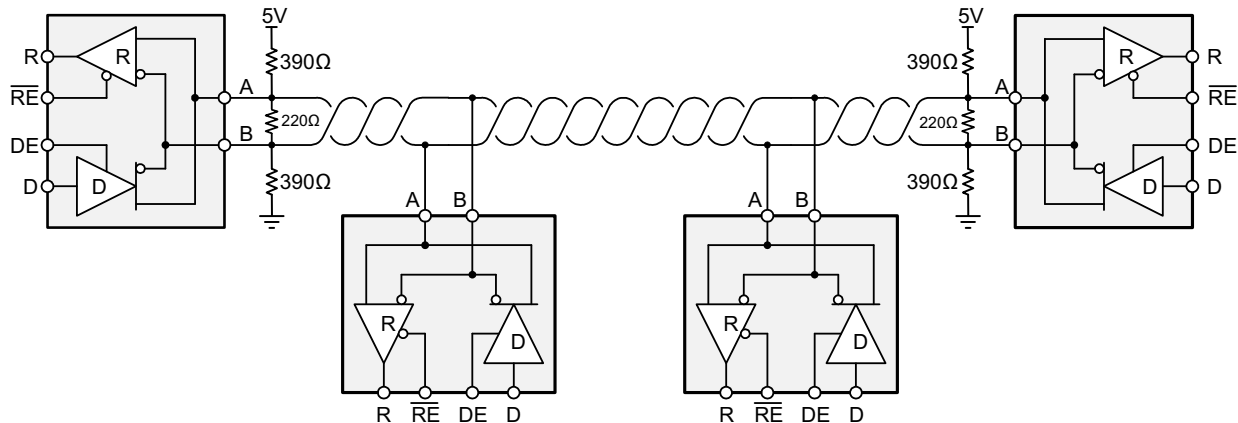


**Figure 24. Typical RS-485 Network With Half-Duplex Transceivers**

**Typical Application (continued)**

The PROFIBUS standard extends RS-485 by specifying the value of the termination resistor, the characteristic impedance of the bus cable, and the value of fail-safe termination at both ends of the bus.

PROFIBUS requires that 220-Ω termination resistors be placed at both ends of the bus, the bus cable impedance be between 135 Ω and 165 Ω, and that 390-Ω fail-safe resistors be placed on both the A and B lines at both ends of the bus.



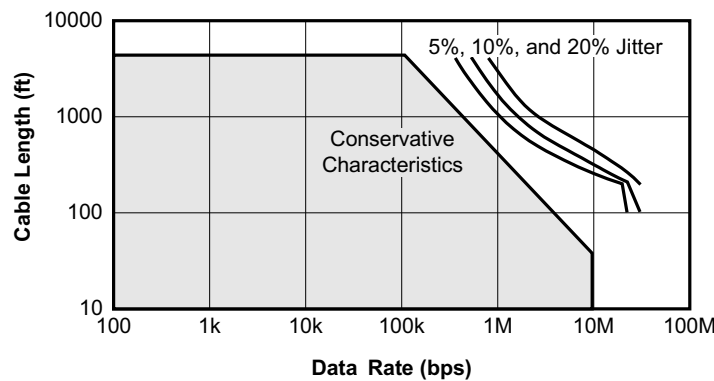
**Figure 25. Typical PROFIBUS network**

**9.2.1 Design Requirements**

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

**9.2.1.1 Data Rate and Bus Length**

There is an inverse relationship between data rate and bus length, that is, the higher the data rate, the shorter the cable length. Conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.



**Figure 26. Cable Length vs Data Rate Characteristic**

## Typical Application (continued)

### 9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in [Equation 1](#).

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

$t_r$  is the 10/90 rise time of the driver

$c$  is the speed of light ( $3 \times 10^8$  m/s)

$v$  is the signal velocity of the cable or trace as a factor of  $c$

Per [Equation 1](#), the maximum recommended stub length for the minimum driver output rise time of the SN65HVD1176 device for a signal velocity of 78% is 0.05 meters (0.16 feet).

### 9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k $\Omega$ . Because the SN65HVD1176 device is a 1/5 UL transceiver, it is possible to connect up to 160 receivers to the bus.

### 9.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD1176 device is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic-high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include zero volts differential.

To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input  $V_{ID}$  is more positive than +200 mV, and must output a low when  $V_{ID}$  is more negative than –200 mV. The receiver parameters that determine the fail-safe performance are  $V_{IT(+)}$  and  $V_{IT(-)}$ .

As shown in [Electrical Characteristics](#), differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than –20 mV will always cause a high receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum  $V_{IT(+)}$  threshold of –20 mV, and the receiver output will be high.

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

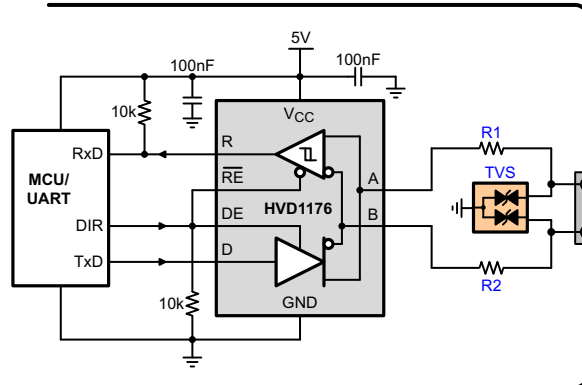


Figure 27. Transient Protection Against ESD, EFT, and Surge Transients

Figure 27 shows a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. Table 3 lists the associated Bill of Materials.

Table 3. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	5-V, 40-Mbps ProfiBus Transceiver	SN65HVD1176	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

### 9.2.3 Application Curve

Figure 28 demonstrates operation of the SN65HVD1179 at a signaling rate of 40 Mbps.

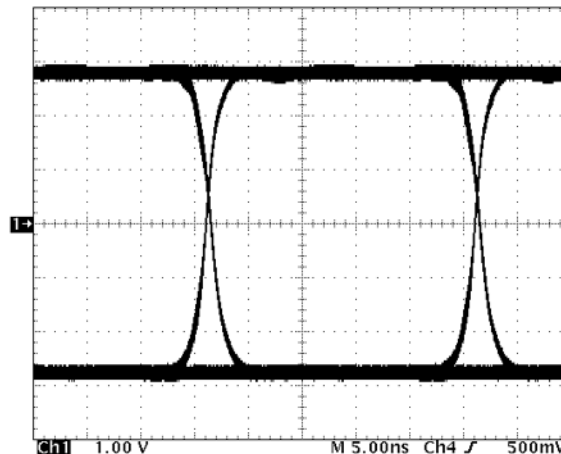


Figure 28. Differential Output of SN65HVD1176 Operation at 40 Mbps

## 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply.

## 11 Layout

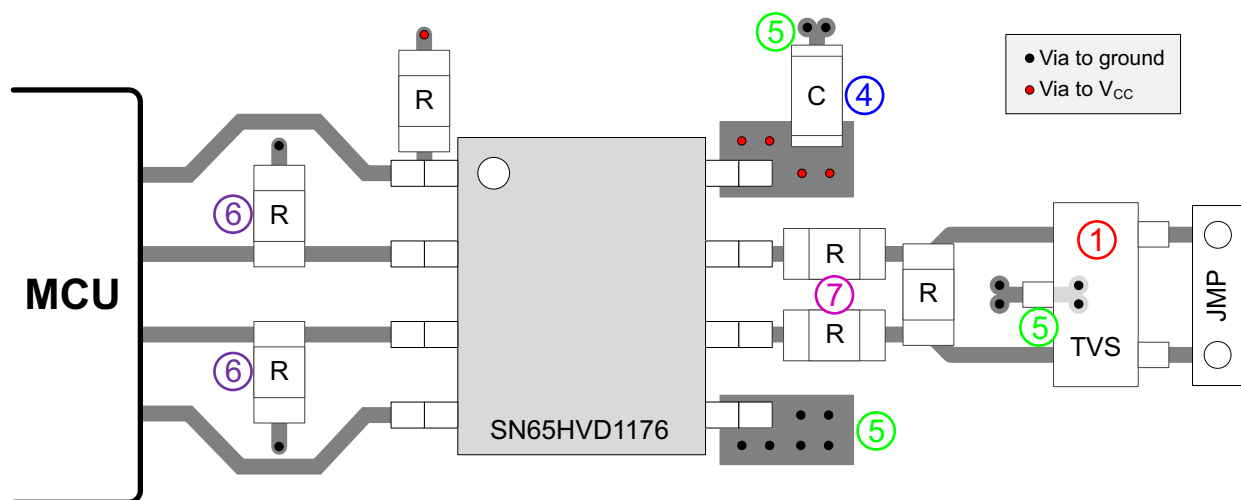
### 11.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus-node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, the UART, or the controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-k $\Omega$  to 10-k $\Omega$  pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) that reduce the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to less than 1 mA.

### 11.2 Layout Example



**Figure 29. SNx5HVD08 Layout Example**

## 12 Device and Documentation Support

### 12.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.2 Documentation Support

For related documentation see the following: *ISO1176 ISOLATED RS-485 PROFIBUS TRANSCEIVER (SLLS897)*

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD1176	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN75HVD1176	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.  
 PROFIBUS is a registered trademark of PROFIBUS Nutzerorganisation e.V..  
 All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1176D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	<a href="#">Samples</a>
SN65HVD1176DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	<a href="#">Samples</a>
SN65HVD1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	<a href="#">Samples</a>
SN65HVD1176DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176	<a href="#">Samples</a>
SN75HVD1176D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN1176	<a href="#">Samples</a>
SN75HVD1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN1176	<a href="#">Samples</a>
SN75HVD1176DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN1176	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

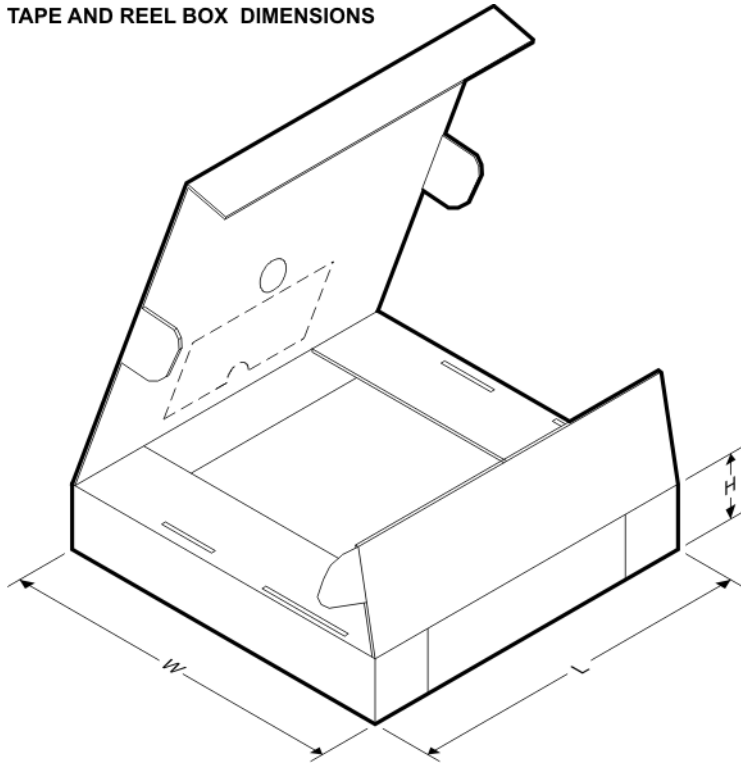
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1176DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75HVD1176DR	SOIC	D	8	2500	340.5	336.1	25.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65HVD1176D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD1176DG4	D	SOIC	8	75	507	8	3940	4.32
SN75HVD1176D	D	SOIC	8	75	507	8	3940	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated