

# 8-Stage Shift/Store Register with Three-State Outputs

## MC14094B

The MC14094B combines an 8-stage shift register with a data latch for each stage and a 3-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The  $Q_S$  output data is for use in high-speed cascaded systems. The  $Q_{\bar{S}}$  output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by 3-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

### Features

- 3-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

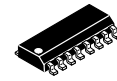
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

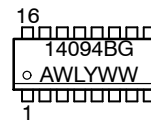


SOIC-16  
D SUFFIX  
CASE 751B

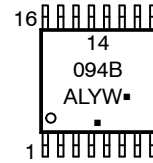


TSSOP-16  
DT SUFFIX  
CASE 948F

### MARKING DIAGRAMS



SOIC-16



TSSOP-16

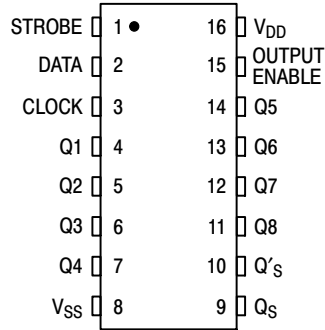
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14094B

## PIN ASSIGNMENT



## TRUTH TABLE

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q <sub>1</sub>	Q <sub>N</sub>	Q <sub>S</sub> *	Q' <sub>S</sub>
↗	0	X	X	Z	Z	Q <sub>7</sub>	No Chg.
↘	0	X	X	Z	Z	No Chg.	Q <sub>7</sub>
↗	1	0	X	No Chg.	No Chg.	Q <sub>7</sub>	No Chg.
↗	1	1	0	0	Q <sub>N-1</sub>	Q <sub>7</sub>	No Chg.
↗	1	1	1	1	Q <sub>N-1</sub>	Q <sub>7</sub>	No Chg.
↘	1	1	1	No Chg.	No Chg.	No Chg.	Q <sub>7</sub>

Z = High Impedance    X = Don't Care

\* At the positive clock edge, information in the 7th shift register stage is transferred to Q<sub>8</sub> and Q<sub>S</sub>.

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC14094BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14094BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14094BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14094BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14094BDTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
	"1" Level V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
		15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
		15	11	-	11	8.25	-	11	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	
15		4.2	-	3.4	8.8	-	2.4	-		
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μAdc
		10	-	10	-	0.010	10	-	300	
		15	-	20	-	0.015	20	-	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (4.1 μA/kHz) f + I <sub>DD</sub>							μAdc
		10	I <sub>T</sub> = (14 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (140 μA/kHz) f + I <sub>DD</sub>							
3-State Output Leakage Current	I <sub>TL</sub>	15	-	±0.1	-	±0.0001	±0.1	-	±3.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS (Note 5) (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t <sub>TLH</sub> , t <sub>THL</sub> = (1.35 ns/pF) C <sub>L</sub> + 33 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.6 ns/pF) C <sub>L</sub> + 20 ns t <sub>TLH</sub> , t <sub>THL</sub> = (0.4 ns/pF) C <sub>L</sub> + 20 ns	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 1) Clock to Serial out QS t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 305 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 107 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 82 ns  Clock to Serial out Q'S t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 350 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 149 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 62 ns  Clock to Parallel out t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 375 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.35 ns/pF) C <sub>L</sub> + 177 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 122 ns  Strobe to Parallel out t <sub>PLH</sub> , t <sub>PHL</sub> = (0.90 ns/pF) C <sub>L</sub> + 245 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.36 ns/pF) C <sub>L</sub> + 127 ns t <sub>PLH</sub> , t <sub>PHL</sub> = (0.26 ns/pF) C <sub>L</sub> + 87 ns  Output Enable to Output t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.90 ns/pF) C <sub>L</sub> + 95 ns t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.36 ns/pF) C <sub>L</sub> + 57 ns t <sub>PHZ</sub> , t <sub>PZL</sub> = (0.26 ns/pF) C <sub>L</sub> + 42 ns  t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.90 ns/pF) C <sub>L</sub> + 180 ns t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.36 ns/pF) C <sub>L</sub> + 77 ns t <sub>PLZ</sub> , t <sub>PZH</sub> = (0.26 ns/pF) C <sub>L</sub> + 57 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	350 125 95	600 250 190	ns
		5.0 10 15	- - -	230 110 75	460 220 150	
		5.0 10 15	- - -	420 195 135	840 390 270	
		5.0 10 15	- - -	290 145 100	580 290 200	
	t <sub>PHZ</sub> , t <sub>PZL</sub>	5.0 10 15	- - -	140 75 55	280 150 110	
	t <sub>PLZ</sub> , t <sub>PZH</sub>	5.0 10 15	- - -	225 95 70	450 190 140	
Setup Time Data in to Clock	t <sub>su</sub>	5.0 10 15	125 55 35	60 30 20	- - -	ns
Hold Time Clock to Data	t <sub>h</sub>	5.0 10 15	0 20 20	-40 -10 0	- - -	ns
Clock Pulse Width, High	t <sub>WH</sub>	5.0 10 15	200 100 83	100 50 40	- - -	ns
Clock Rise and Fall Time	t <sub>r(cl)</sub> t <sub>f(cl)</sub>	5 10 15	- - -	- - -	15 5.0 4.0	μs
Clock Pulse Frequency	f <sub>cl</sub>	5.0 10 15	- - -	2.5 5.0 6.0	1.25 2.5 3.0	MHz
Strobe Pulse Width	t <sub>WL</sub>	5.0 10 15	200 80 70	100 40 35	- - -	ns

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14094B

## 3-STATE TEST CIRCUIT

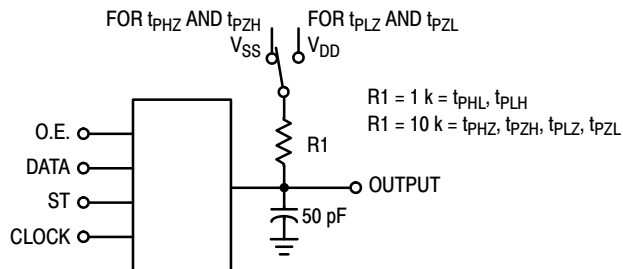
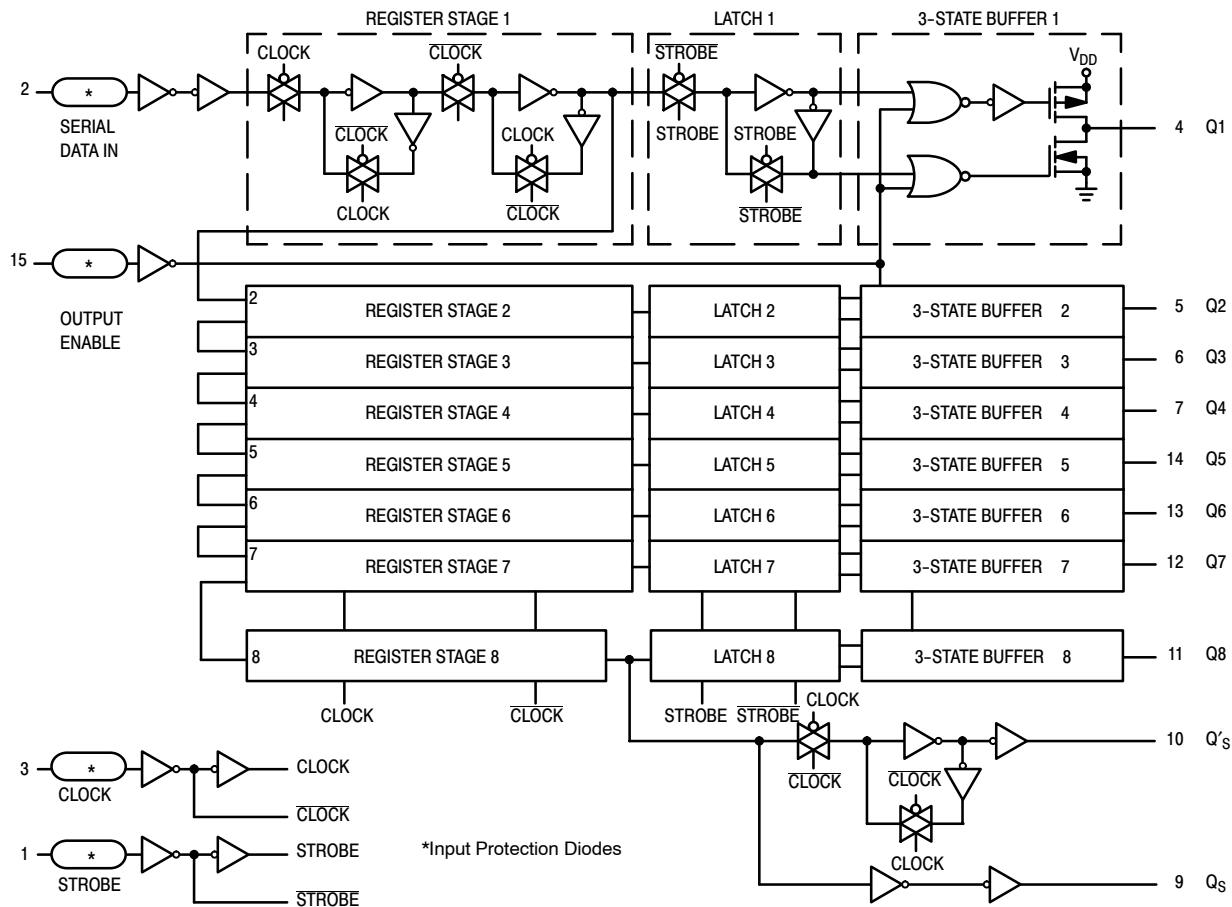


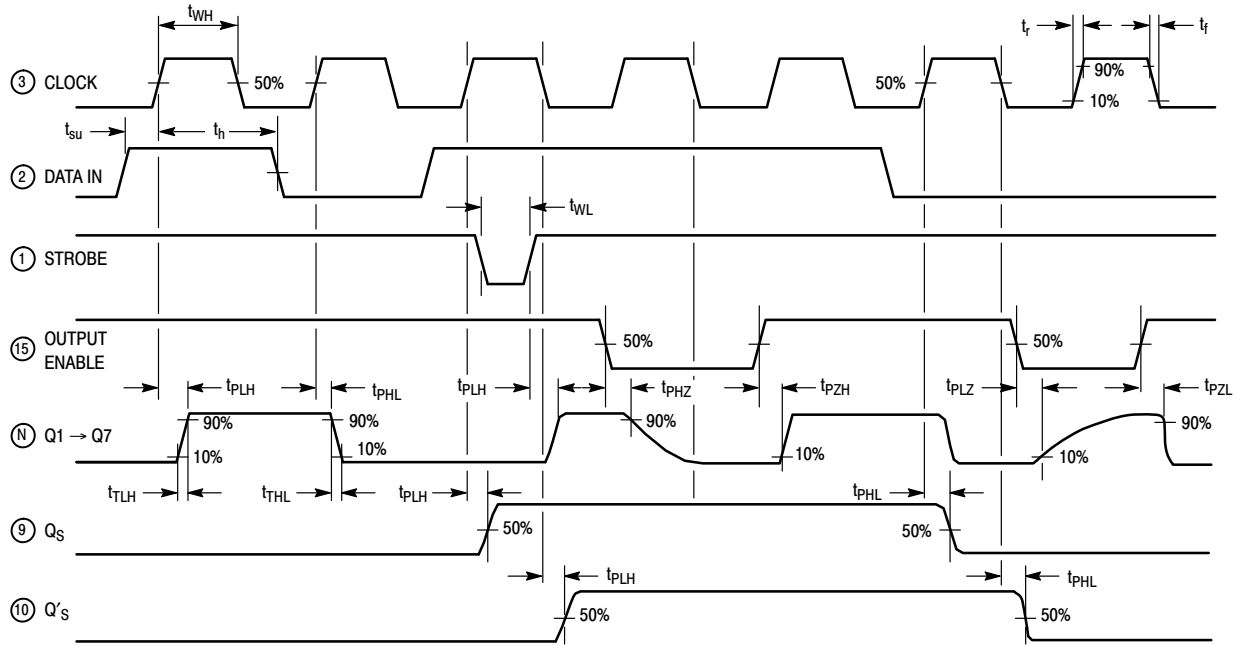
Figure 1.

## BLOCK DIAGRAM



# MC14094B

## DYNAMIC TIMING DIAGRAM



# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- |  |  |  |  |
|--|--|--|--|
| <p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR<br/>2. BASE<br/>3. EMITTER<br/>4. NO CONNECTION<br/>5. EMITTER<br/>6. BASE<br/>7. COLLECTOR<br/>8. COLLECTOR<br/>9. BASE<br/>10. EMITTER<br/>11. NO CONNECTION<br/>12. EMITTER<br/>13. BASE<br/>14. COLLECTOR<br/>15. EMITTER<br/>16. COLLECTOR</p>                           | <p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE<br/>2. ANODE<br/>3. NO CONNECTION<br/>4. CATHODE<br/>5. CATHODE<br/>6. NO CONNECTION<br/>7. ANODE<br/>8. CATHODE<br/>9. CATHODE<br/>10. ANODE<br/>11. NO CONNECTION<br/>12. CATHODE<br/>13. CATHODE<br/>14. NO CONNECTION<br/>15. ANODE<br/>16. CATHODE</p> | <p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/>2. BASE, #1<br/>3. EMITTER, #1<br/>4. COLLECTOR, #1<br/>5. COLLECTOR, #2<br/>6. BASE, #2<br/>7. EMITTER, #2<br/>8. COLLECTOR, #2<br/>9. COLLECTOR, #3<br/>10. BASE, #3<br/>11. EMITTER, #3<br/>12. COLLECTOR, #3<br/>13. COLLECTOR, #4<br/>14. BASE, #4<br/>15. EMITTER, #4<br/>16. COLLECTOR, #4</p>   | <p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1<br/>2. COLLECTOR, #1<br/>3. COLLECTOR, #2<br/>4. COLLECTOR, #2<br/>5. COLLECTOR, #3<br/>6. COLLECTOR, #3<br/>7. COLLECTOR, #4<br/>8. COLLECTOR, #4<br/>9. BASE, #4<br/>10. EMITTER, #4<br/>11. BASE, #3<br/>12. EMITTER, #3<br/>13. BASE, #2<br/>14. EMITTER, #2<br/>15. BASE, #1<br/>16. EMITTER, #1</p> |
| <p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1<br/>2. DRAIN, #1<br/>3. DRAIN, #2<br/>4. DRAIN, #2<br/>5. DRAIN, #3<br/>6. DRAIN, #3<br/>7. DRAIN, #4<br/>8. DRAIN, #4<br/>9. GATE, #4<br/>10. SOURCE, #4<br/>11. GATE, #3<br/>12. SOURCE, #3<br/>13. GATE, #2<br/>14. SOURCE, #2<br/>15. GATE, #1<br/>16. SOURCE, #1</p> | <p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE<br/>2. CATHODE<br/>3. CATHODE<br/>4. CATHODE<br/>5. CATHODE<br/>6. CATHODE<br/>7. CATHODE<br/>8. CATHODE<br/>9. ANODE<br/>10. ANODE<br/>11. ANODE<br/>12. ANODE<br/>13. ANODE<br/>14. ANODE<br/>15. ANODE<br/>16. ANODE</p>                                 | <p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH<br/>2. COMMON DRAIN (OUTPUT)<br/>3. COMMON DRAIN (OUTPUT)<br/>4. GATE P-CH<br/>5. COMMON DRAIN (OUTPUT)<br/>6. COMMON DRAIN (OUTPUT)<br/>7. COMMON DRAIN (OUTPUT)<br/>8. SOURCE P-CH<br/>9. SOURCE P-CH<br/>10. COMMON DRAIN (OUTPUT)<br/>11. COMMON DRAIN (OUTPUT)<br/>12. COMMON DRAIN (OUTPUT)<br/>13. GATE N-CH<br/>14. COMMON DRAIN (OUTPUT)<br/>15. COMMON DRAIN (OUTPUT)<br/>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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