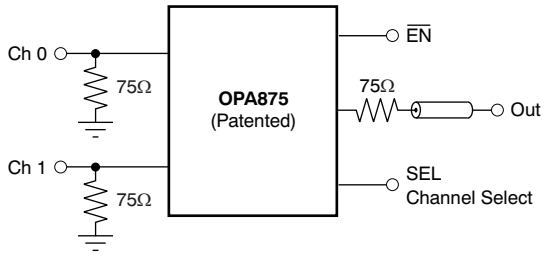
Single 2:1 High-Speed Video Multiplexer

FEATURES

- **700MHz SMALL-SIGNAL BANDWIDTH (A_V = +2)**
- **425MHz, 4V_{PP} BANDWIDTH**
- **0.1dB GAIN FLATNESS to 200MHz**
- **4ns CHANNEL SWITCHING TIME**
- **LOW SWITCHING GLITCH: 40mV_{PP}**
- **3100V/µs SLEW RATE**
- **0.025%/0.025° DIFFERENTIAL GAIN, PHASE**
- **HIGH GAIN ACCURACY: 2.0V/V ±0.4%**

APPLICATIONS

- **RGB SWITCHING**
- **LCD PROJECTOR INPUT SELECT**
- **WORKSTATION GRAPHICS**
- **ADC INPUT MUX**
- **DROP-IN UPGRADE TO LT1675-1**



2:1 Video Multiplexer

DESCRIPTION

The OPA875 offers a very wideband, single-channel 2:1 multiplexer in an SO-8 or a small MSOP-8 package. Using only 11mA, the OPA875 provides a gain of +2 video amplifier channel with greater than 425MHz large-signal bandwidth (4V_{PP}). Gain accuracy and switching glitch are improved over earlier solutions using a new input stage switching approach. This technique uses current steering as the input switch while maintaining an overall closed-loop design. With greater than 700MHz small-signal bandwidth at a gain of 2, the OPA875 gives a typical 0.1dB gain flatness to greater than 200MHz.

System power may be reduced using the chip enable feature for the OPA875. Taking the chip enable line high powers down the OPA875 to less than 300µA total supply current. Muxing multiple OPA875 outputs together, then using the chip enable to select which channels are active, increases the number of possible inputs.

Where three channels are required, consider using the OPA3875 for the same level of performance.

OPA875 RELATED PRODUCTS

	DESCRIPTION
OPA3875	Triple-Channel OPA875
OPA692	225MHz Video Buffer
OPA693	700MHz Video Buffer

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA875	SO-8	D	–40°C to +85°C	OPA875	OPA875ID	Rails, 75
					OPA875IDR	Tape and Reel, 2500
OPA875	MSOP-8	DGK	–40°C to +85°C	BPL	OPA875IDGKT	Tape and Reel, 250
					OPA875IDGKR	Tape and Reel, 2500

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range, unless otherwise noted.

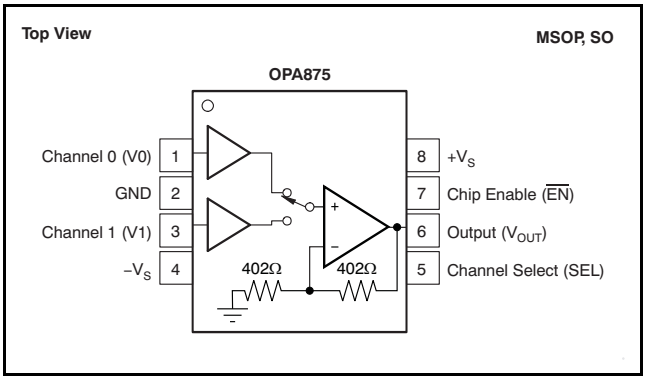
	OPA875	UNIT
Power Supply	±6.5	V
Internal Power Dissipation	See Thermal Analysis	
Input Voltage Range	$\pm V_S$	V
Storage Temperature Range	–65 to +125	°C
Lead Temperature (soldering, 10s)	+260	°C
Operating Junction Temperature	+150	°C
Continuous Operating Junction Temperature	+140	°C
ESD Rating:		
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	1500	V
Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

Table 1. TRUTH TABLE

OPA875		
SELECT	$\overline{\text{ENABLE}}$	V_{OUT}
1	0	R0
0	0	R1
X	1	Off

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: V_S = ±5V

At G = +2 and R_L = 150Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA875 TYP +25°C	OPA875 MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/MAX	TEST LEVEL[1]
AC PERFORMANCE	See Figure 1							
Small-Signal Bandwidth	V_O = 200mV$_{PP}$, R_L = 150Ω	700	525	515	505	MHz	min	B
Large-Signal Bandwidth	V_O = 4V$_{PP}$, R_L = 150Ω	425	390	380	370	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	V_O = 200mV$_{PP}$	200				MHz	typ	C
Maximum Small-Signal Gain	V_O = 200mV$_{PP}$, R_L = 150Ω, f = 5MHz	2.0	2.02	2.03	2.05	V/V	max	B
Minimum Small-Signal Gain	V_O = 200mV$_{PP}$, R_L = 150Ω, f = 5MHz	2.0	1.98	1.97	1.95	V/V	min	B
SFDR	10MHz, V_O = 2V$_{PP}$, R_L = 150Ω	–66	–64	–63	–62	dBc	max	B
Input Voltage Noise	f > 100kHz	6.7	7.0	7.2	7.4	nV/√Hz	max	B
Input Current Noise	f > 100kHz	3.8	4.2	4.6	4.9	pA/√Hz	max	B
NTSC Differential Gain	R_L = 150Ω	0.025				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.025				°	typ	C
Slew Rate	V_O = ±2V	3100	2800	2700	2600	V/µs	min	B
Rise Time and Fall Time	V_O = 0.5V Step	460				ps	typ	C
	V_O = 1.4V Step	600				ps	typ	C
CHANNEL-TO-CHANNEL PERFORMANCE								
Gain Match	R_L = 150Ω	±0.05	**±0.25**	±0.3	±0.35	%	max	A
Output Offset Voltage Mismatch		±3	**±9**	±10	±12	mV	max	A
Crosstalk	f < 50MHz, R_L = 150Ω	–65				dB	typ	C
CHANNEL AND CHIP-SELECT PERFORMANCE								
SEL (Channel Select) Switching Time	R_L = 150Ω	4				ns	typ	C
$\overline{EN}$ (Chip Select) Switching Time	Turn On	9				ns	typ	C
	Turn Off	60				ns	typ	C
SEL (Channel Select) Switching Glitch	Both Inputs to Ground, At Matched Load	40				mV$_{PP}$	typ	C
$\overline{EN}$ (Chip-Select) Switching Glitch	Both Inputs to Ground, At Matched Load	30				mV$_{PP}$	typ	C
Off Isolation	50MHz, Chip Disabled ($\overline{EN}$ = High)	–70				dB	typ	C
Maximum Logic 0	$\overline{EN}$, A0, A1		**0.8**	0.8	0.8	V	max	A
Minimum Logic 1	$\overline{EN}$, A0, A1		**2.0**	2.0	2.0	V	min	A
$\overline{EN}$ Logic Input Current	0V to 4.5V	25	**35**	45	50	µA	max	A
SEL Logic Input Current	0V to 4.5V	55	**70**	85	100	µA	max	A
DC PERFORMANCE								
Output Offset Voltage	R_{IN} = 0Ω, G = +2V/V	±2.5	**±14**	±15.8	±17	mV	max	A
Average Output Offset Voltage Drift				±50	±50	µV/°C	max	B
Input Bias Current		±5	**±18**	±19.5	±20.5	µA	max	A
Average Input Bias Current Drift				±40	±40	nA/°C	max	B
Gain Error (from 2V/V)	V_O = ±2V	0.4	**1.4**	1.5	1.6	%	max	A
INPUT								
Input Voltage Range		±2.8				V	min	C
Input Resistance		1.75				MΩ	typ	C
Input Capacitance	Channel Selected	0.9				pF	typ	C
	Channel Deselected	0.9				pF	typ	C
	Chip Disabled	0.9				pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +14°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

PARAMETER		CONDITIONS	OPA875 TYP +25°C	OPA875 MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OUTPUT									
Output Voltage Range			±3.5	**±3.4**	±3.35	±3.3	V	min	A
Output Current		V_O = 0V, Linear Operation	±70	**±50**	±45	±40	mA	min	A
Output Resistance		Chip enabled	0.3				Ω	typ	C
		Chip Disabled, Maximum	800	**912**	915	918	Ω	max	A
		Chip Disabled, Minimum	800	**688**	685	682	Ω	min	A
Output Capacitance		Chip Disabled	2				pF	typ	C
POWER SUPPLY									
Specified Operating Voltage			±5				V	typ	C
Minimum Operating Voltage				**±3.0**	±3.0	±3.0	V	min	B
Maximum Operating Voltage				**±6.0**	±6.0	±6.0	V	max	A
Maximum Quiescent Current		Chip Selected, V_S = ±5V	11	**11.5**	11.7	12	mA	max	A
Minimum Quiescent Current		Chip Selected, V_S = ±5V	11	**10**	9.5	9	mA	min	A
Maximum Quiescent Current		Chip Deselected	300	**500**	550	600	µA	max	A
Power-Supply Rejection Ratio	(+PSRR)	Input-Referred	56	**50**	48	47	dB	min	A
	(–PSRR)	Input-Referred	55	**51**	49	48	dB	min	A
THERMAL CHARACTERISTICS									
Specified Operating Range D Package			–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}		Junction-to-Ambient							
D	SO-8		+100				°C/W	typ	C
DGK	MSOP-8		+140				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At G = +2 and R_L = 150Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

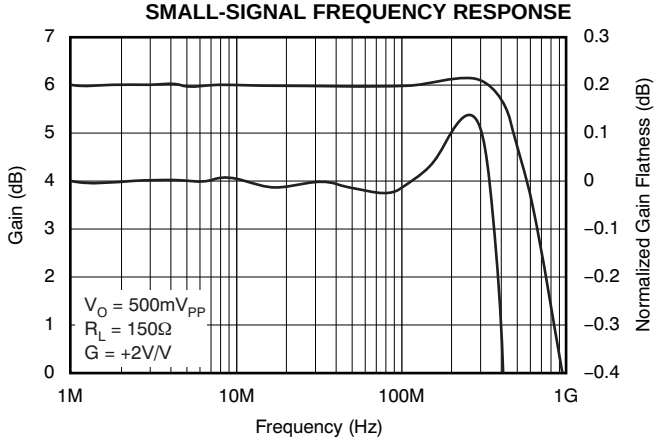


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

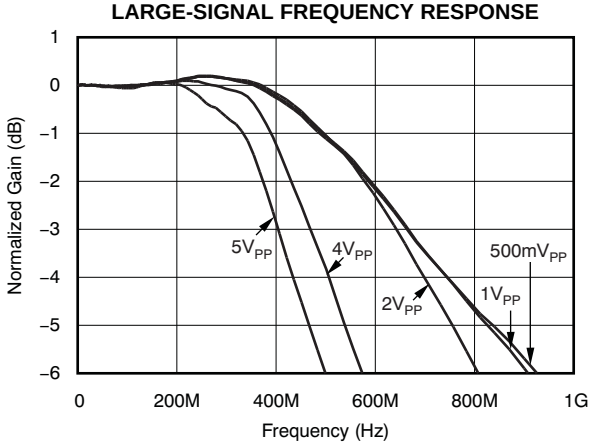


Figure 2.

NONINVERTING PULSE RESPONSE

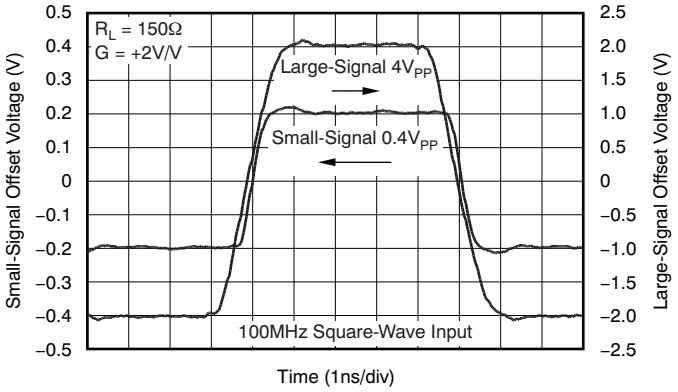


Figure 3.

DISABLE FEEDTHROUGH vs FREQUENCY

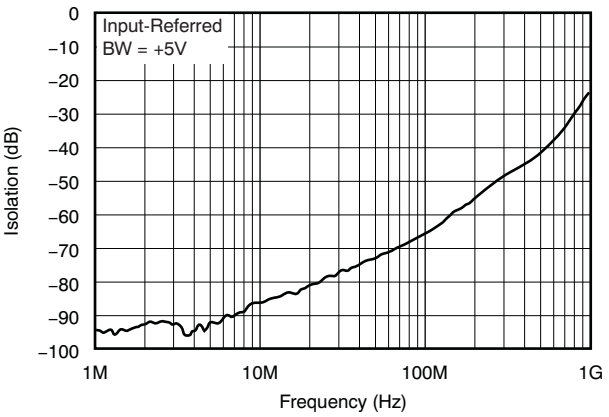


Figure 4.

RECOMMENDED R_S vs CAPACITIVE LOAD

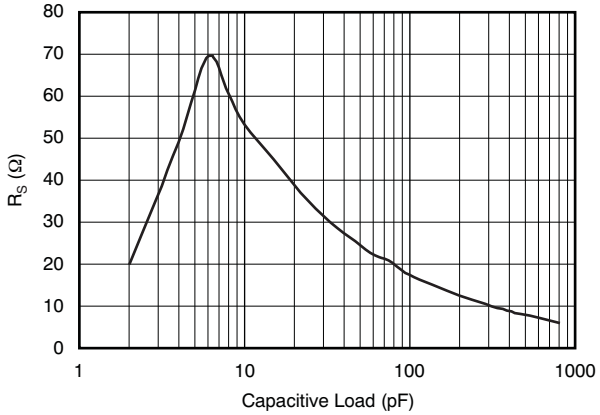


Figure 5.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

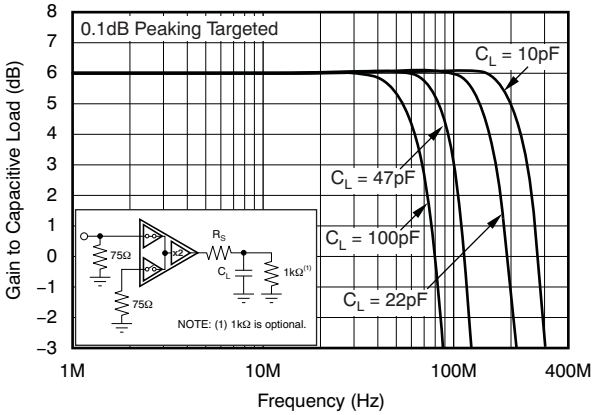


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

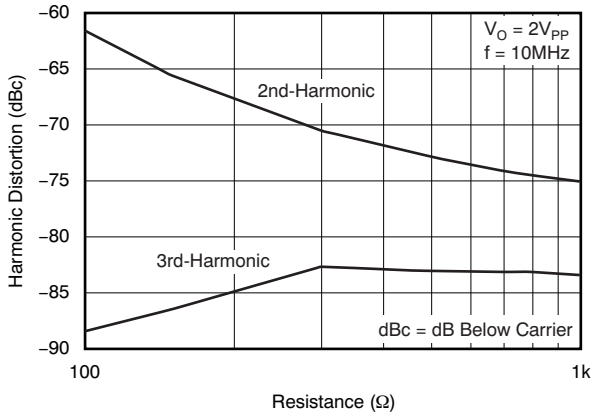


Figure 7.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

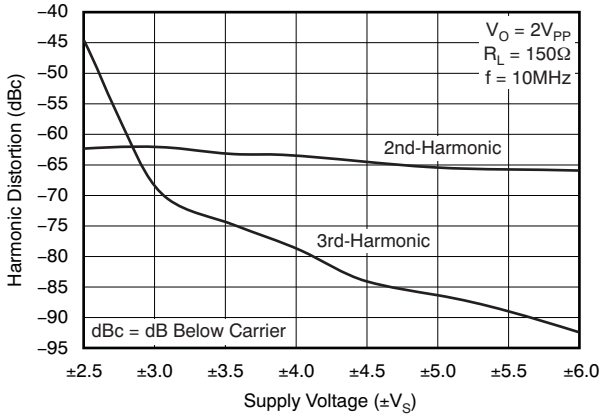


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

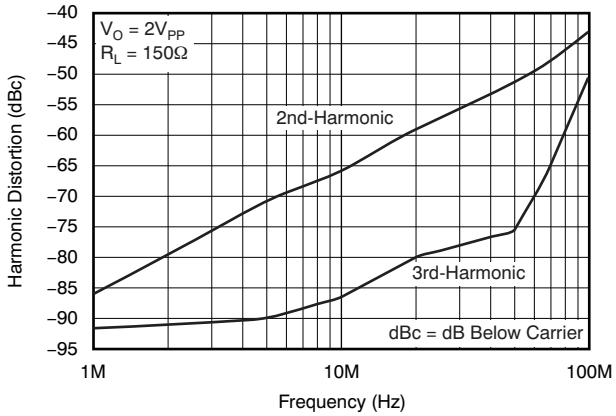


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

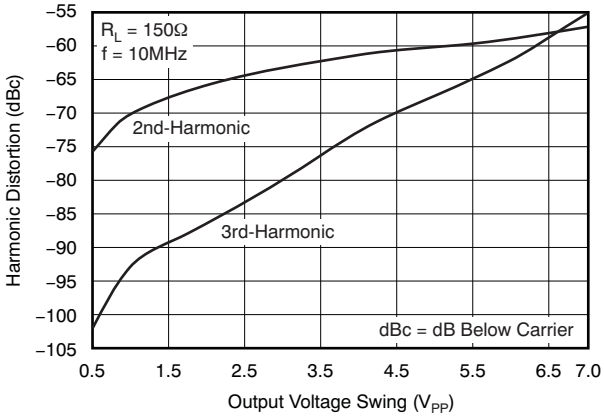


Figure 10.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

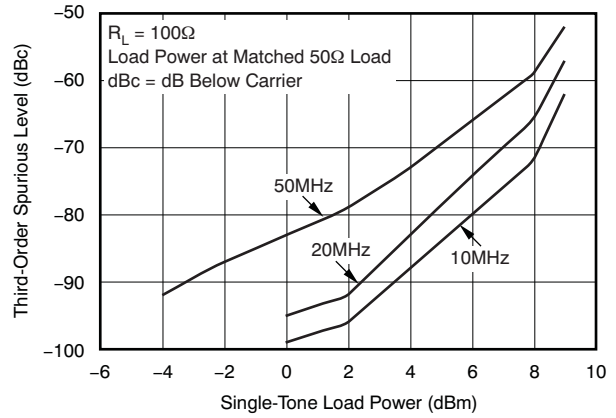


Figure 11.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

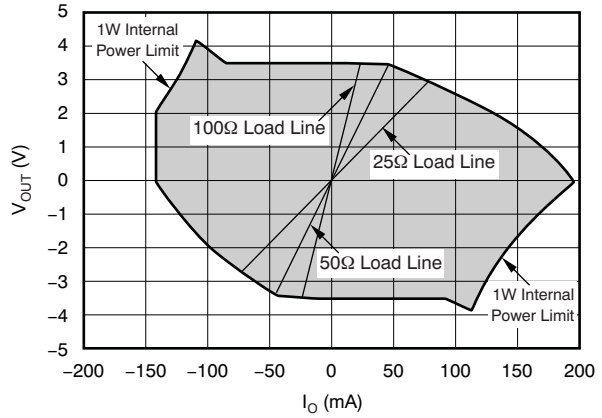


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

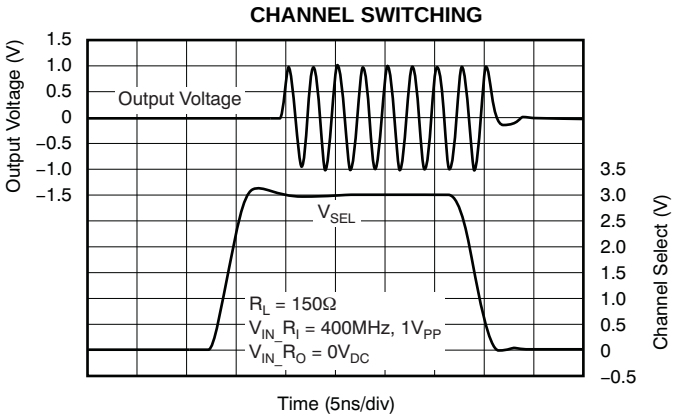


Figure 13.

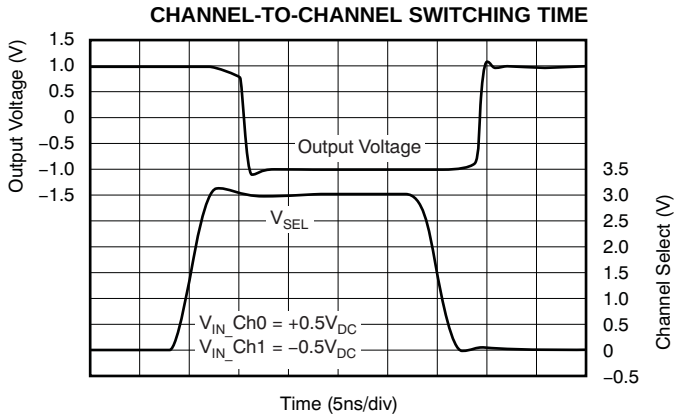


Figure 14.

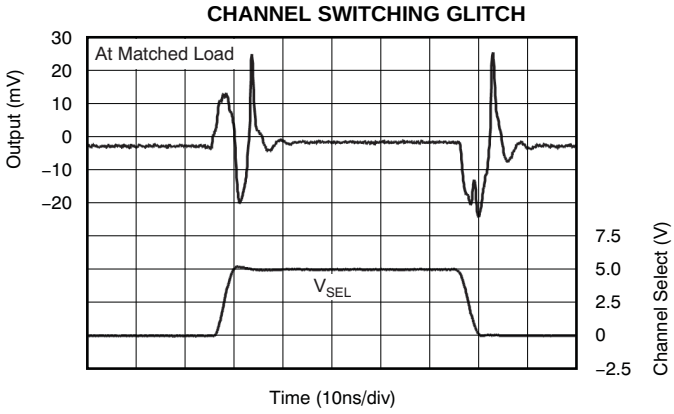


Figure 15.

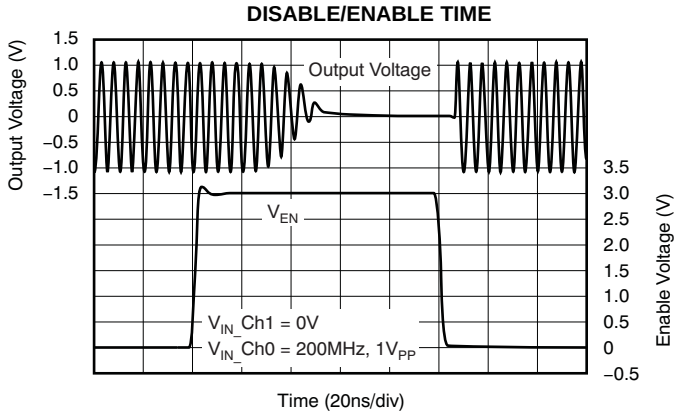


Figure 16.

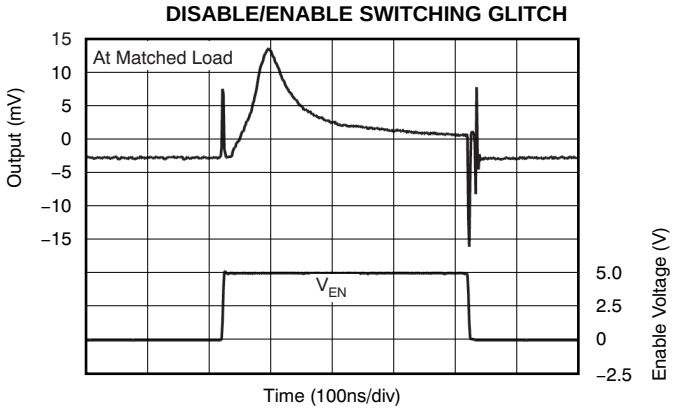


Figure 17.

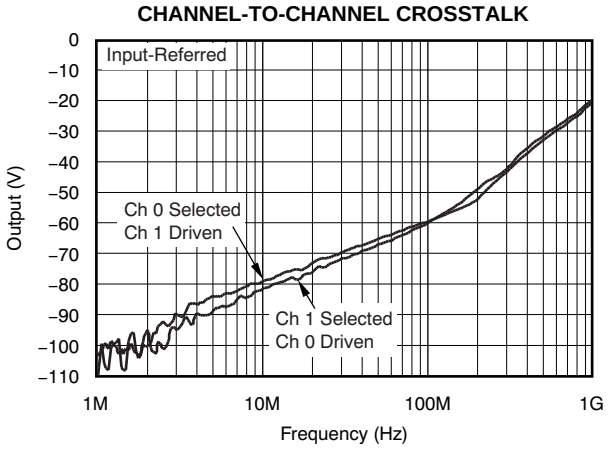


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At G = +2 and R_L = 150Ω, unless otherwise noted.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

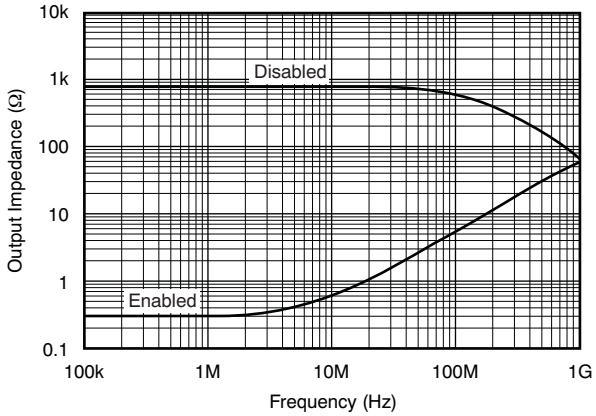


Figure 19.

INPUT IMPEDANCE vs FREQUENCY

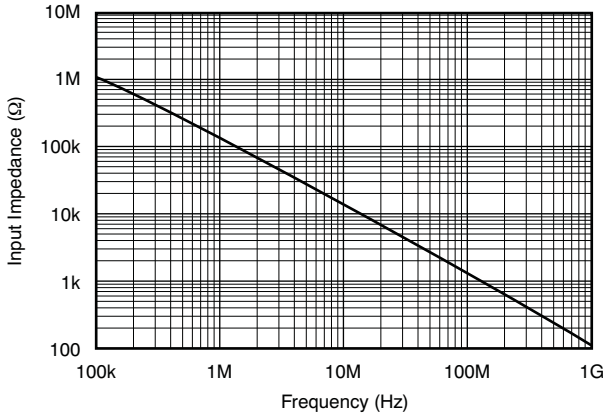


Figure 20.

PSRR vs FREQUENCY

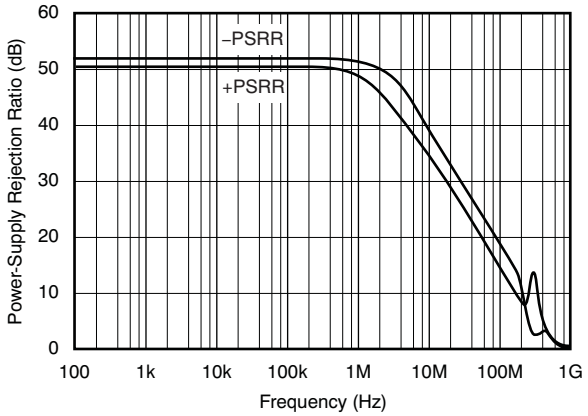


Figure 21.

SUPPLY CURRENT vs TEMPERATURE

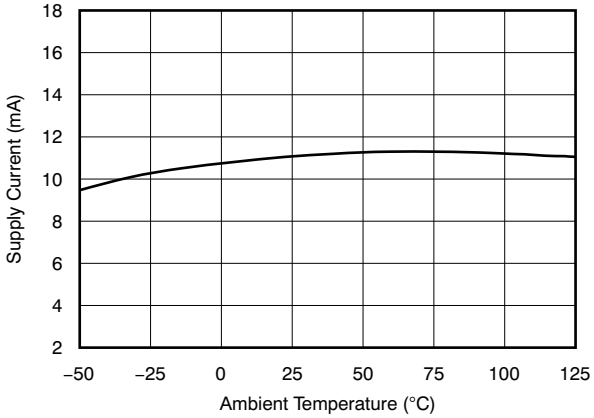


Figure 22.

TYPICAL DC DRIFT OVER TEMPERATURE

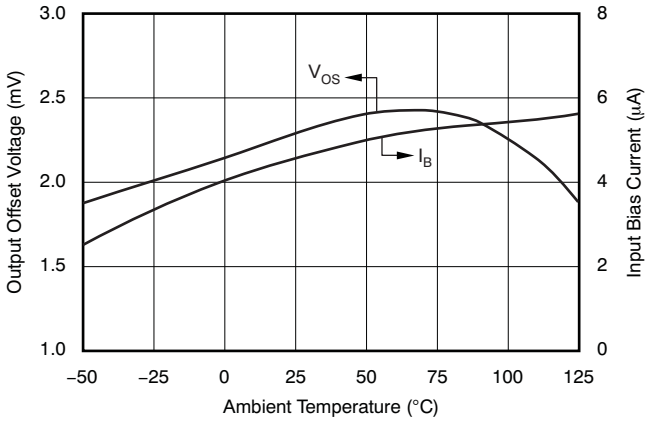


Figure 23.

INPUT VOLTAGE AND CURRENT NOISE

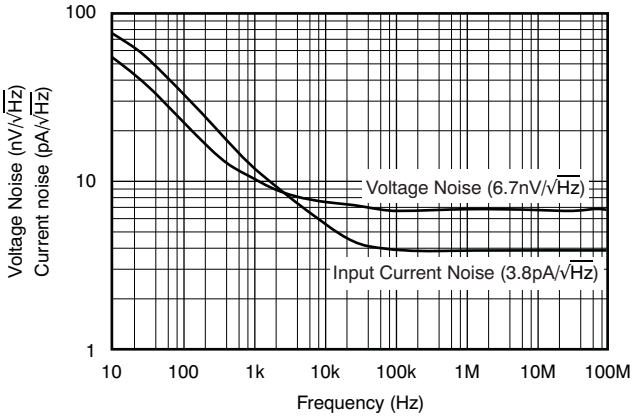


Figure 24.

APPLICATIONS INFORMATION

1-BIT HIGH-SPEED PGA

The OPA875 can be used as a 1-bit, high-speed programmable gain amplifier (PGA) when used in conjunction with another amplifier. Figure 25 shows the OPA695 used twice with one amplifier configured in a unity-gain structure, and the other amplifier configured in a gain of +8V/V.

When channel 0 is selected, the overall gain to the matched load of the OPA875 is 0dB. When channel 1 is selected, this circuit delivers an 18dB gain to the matched load.

TRANSMIT/RECEIVE SWITCH

The OPA875 can be used as a transmit/receive switch in which the receive channel is disconnected, when the OPA875 is switched from channel 0 to channel 1, to prevent the transmit pulse from going through the receive signal chain. This architecture is shown in Figure 26.

HIGH ISOLATION RGB VIDEO MUX

Three OPA875s can be used as a triple, 2:1 video MUX (see Figure 27). This configuration has the advantage of having higher R to G to B isolation than a comparable and more integrated solution does, such as the OPA3875, especially at higher frequencies. This comparison is shown in Figure 28.

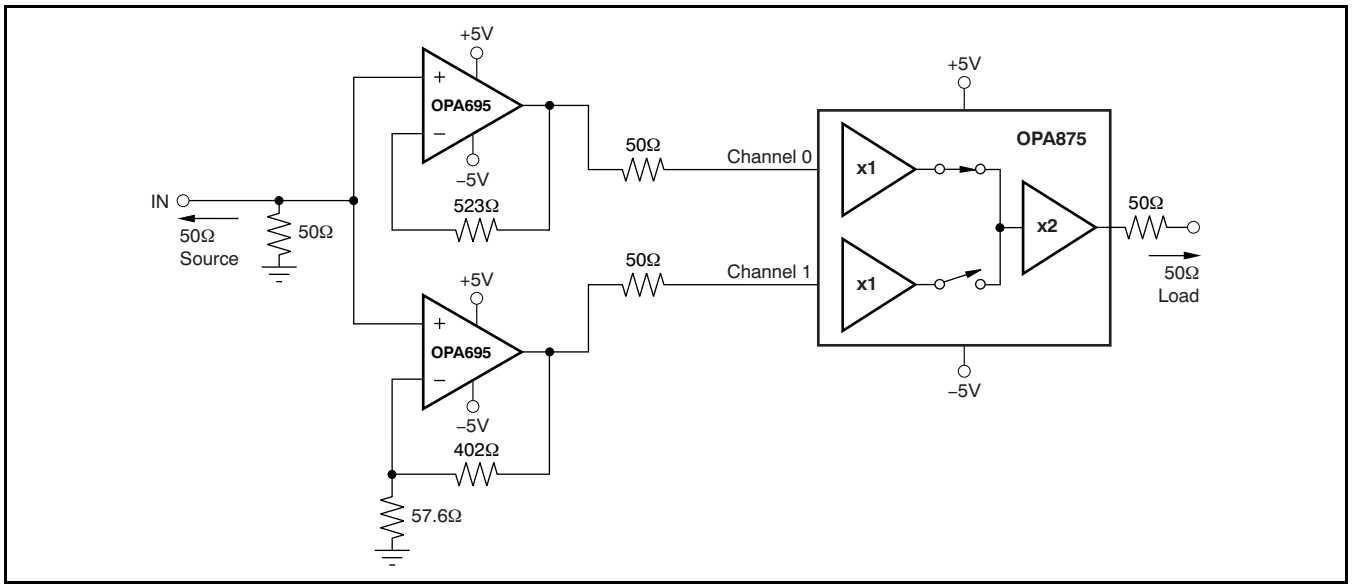


Figure 25. 1-Bit, High-Speed PGA

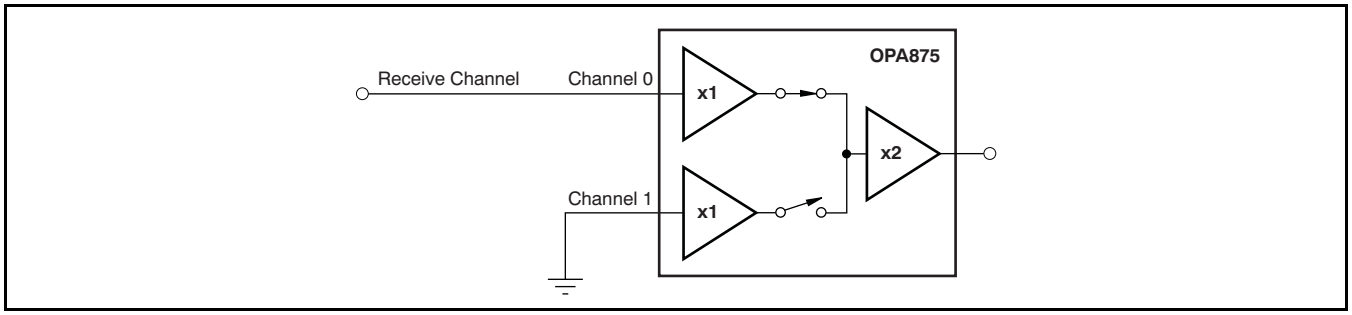


Figure 26. Transmit/Receive Switch

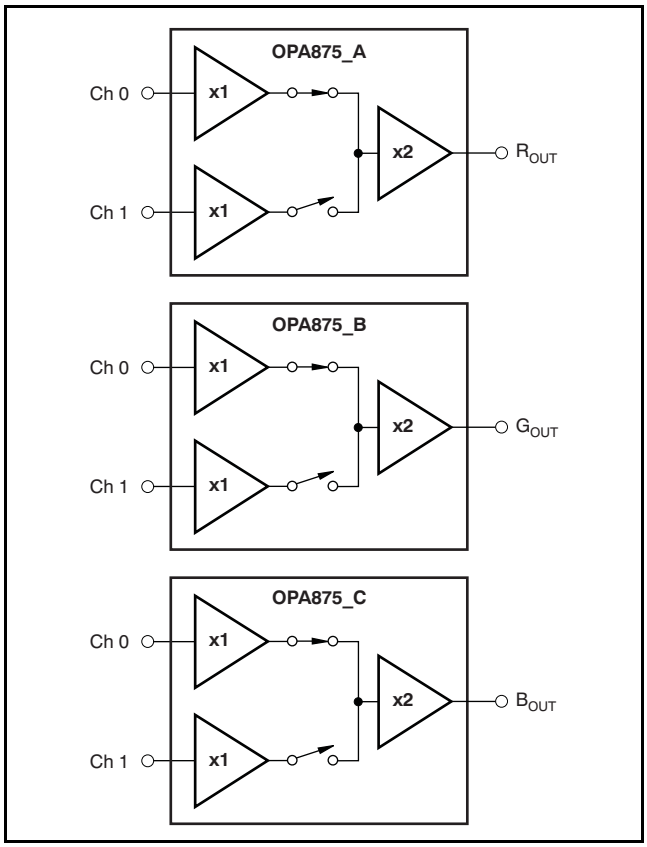


Figure 27. High Isolation RGB Video MUX

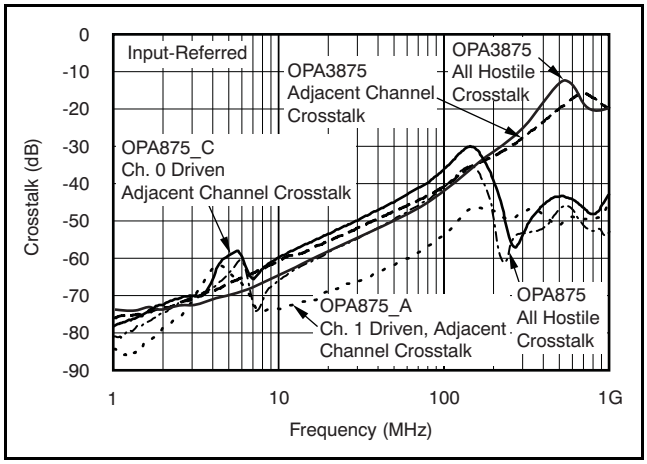


Figure 28. All Hostile and Adjacent Channel Crosstalk

The configuration of the three OPA875 devices used is shown in Figure 27. Note that for the test, the OPA875_B was measured when both the OPA875_A and OPA875_C were driven for all hostile crosstalk and only the OPA875_A or OPA875_C was driven for the adjacent channel crosstalk.

4-INPUT RGB ROUTER

Two OPA875s can be used together to form a four-input RGB router. The router for the red component is shown in Figure 29.

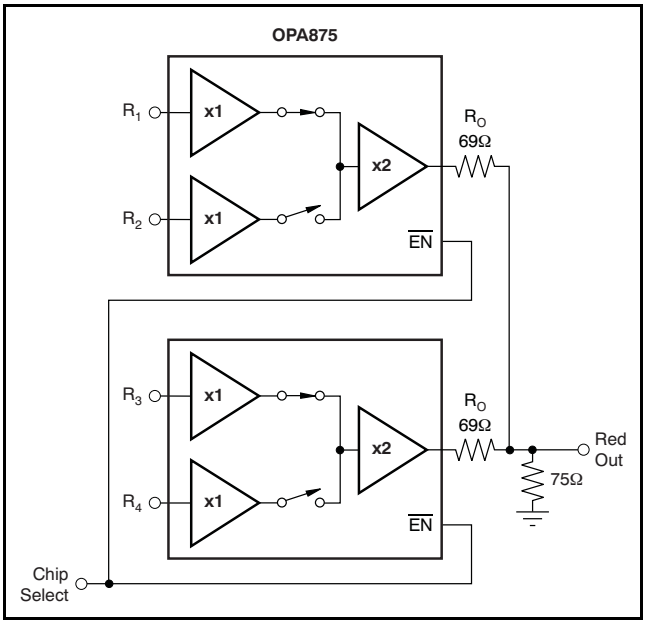


Figure 29. 4-Input RGB Router

When connecting OPA875 outputs together, maintain a gain of +1 at the load. The OPA875 operates at a gain of +6dB; thus, matching resistance must be selected to achieve –6dB attenuation.

The set of equations to solve are shown in Equation 1 and Equation 2. Here, the impedance of interest is $Z_O = 75\Omega$.

$$\begin{cases} R_O = Z_O \parallel (R + R_F + R_G) \\ 1 + \dfrac{R_F}{R_G} = 2 \end{cases} \quad (1)$$

$$\begin{cases} R_F + R_G = 804\Omega \\ R_F = R_G \end{cases} \quad (2)$$

Solving for R_O with *n* devices connected together, we get Equation 3:

$$R_O = \frac{75 \times (n-1) + 804}{2} \times \left(\sqrt{1 + \frac{241200}{[75 \times (n-1) + 804]^2}} - 1 \right) \quad (3)$$

Results for *n* varying from 2 to 6 are given in Table 2.

Table 2. Series Resistance versus Number of Parallel Outputs

NUMBER OF OPA875s	R_O (Ω)
2	69
3	63.94
4	59.49
5	55.59
6	52.15

The two major limitations of this circuit are the device requirements for each OPA875 and the acceptable return loss because of the mismatch between the load (75Ω) and the matching resistor.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA875. These fixtures are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 3.

Table 3. OPA875 Demonstration Fixtures

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA875IDGK	MSOP-8	DEM-OPA-MSOP-1B	SBOU044
OPA875ID	SO-8	DEM-OPA-SO-1D	SBOU049

The demonstration fixture can be requested at the Texas Instruments web site at (www.ti.com) through the OPA875 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA875 is available through the Texas Instruments web site at www.ti.com. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

DRIVING CAPACITIVE LOADS

One of the most demanding, yet very common load conditions is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed device such as the OPA875 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the device open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This isolation resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load; see Figure 5. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA875. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA875 output pin (see the Board Layout Guidelines section).

DC ACCURACY

The OPA875 offers excellent DC signal accuracy. Parameters that influence the output DC offset voltage are:

- Output offset voltage
- Input bias current
- Gain error
- Power-supply rejection ratio
- Temperature

Leaving both temperature and gain error parameters aside, the output offset voltage envelope can be described as shown in Equation 4:

$$V_{OSO\_envelope} = V_{OSO} + (R_S \bullet I_b) \times G \pm \left|5 - (V_{S+})\right| \times 10^{-\frac{PSRR+}{20}} \pm \left|-5 - (V_{S-})\right| \times 10^{-\frac{PSRR-}{20}} \quad (4)$$

With:

V_{OSO}: Output offset voltage

R_S: Input resistance seen by R0, R1, G0, G1, B0, or B1.

I_b: Input bias current

G: Gain

V_{S+}: Positive supply voltage

V_{S-}: Negative supply voltage

PSRR+: Positive supply PSRR

PSRR–: Negative supply PSRR

Evaluating the front-page schematic, using a worst-case, +25°C offset voltage, bias current and PSRR specifications and operating at ±6V, gives a worst-case output equal to Equation 5:

$$\pm 14mV + 75\Omega \times \pm 18\mu A \times 2 \pm \left|5 - 6\right| \times 10^{-\frac{50}{20}} \pm \left|-5 - (-6)\right| \times 10^{-\frac{51}{20}} = \pm 22.7mV \quad (5)$$

DISTORTION PERFORMANCE

The OPA875 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Also, providing an additional supply decoupling capacitor (0.01μF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2X rate while the 3rd-harmonic increases at a little less than the expected 3X rate. Where the test power doubles, the 2nd-harmonic increases only by less than the expected 6dB, whereas the 3rd-harmonic increases by less than the expected 12dB. This also shows up in the two-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 4dBm/tone into a matched 50Ω load (that is, $1V_{PP}$ for each tone at the load, which requires $4V_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show a 82dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels.

NOISE PERFORMANCE

The OPA875 offers an excellent balance between voltage and current noise terms to achieve low output noise. As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The device input voltage noise and the input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 30 shows this device noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

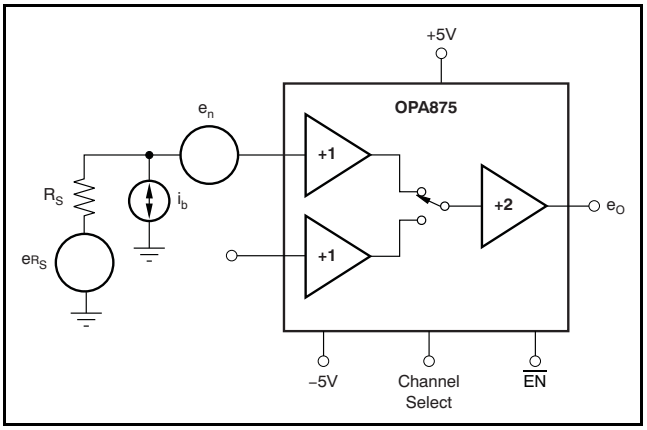


Figure 30. Noise Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 6 shows the general form for the output noise voltage using the terms shown in Figure 30.

$$e_o = 2\sqrt{e_n^2 + (i_b R_S)^2 + 4kTR_S} \quad (6)$$

Dividing this expression by the device gain (2V/V) gives the equivalent input-referred spot noise voltage at the noninverting input as shown in Equation 7.

$$e_n = \sqrt{e_n^2 + (i_b R_S)^2 + 4kTR_S} \quad (7)$$

Evaluating these two equations for the OPA875 circuit and component values shown in Figure 30 gives a total output spot noise voltage of 13.6nV/√Hz and a total equivalent input spot noise voltage of 6.8nV/√Hz. This total input-referred spot noise voltage is higher than the 6.7nV/√Hz specification for the mux voltage noise alone. This number reflects the noise added to the output by the bias current noise times the source resistor.

THERMAL ANALYSIS

Heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as discussed in this document. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA875IDGK in the circuit of Figure 30 operating at the maximum specified ambient temperature of +85°C with its outputs driving a grounded 100Ω load to +2.5V:

$$P_D = 10V \times 11mA + (5^2 [4 \times (100\Omega \parallel 804\Omega)]) = 180mW$$

$$\text{Maximum } T_J = +85°C + (0.18mW \times 140°C/W) = 110°C$$

This worst-case condition does not exceed the maximum junction temperature. Normally, this extreme case is not encountered. Careful attention to internal power dissipation is required.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier such as the OPA875 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 9, 11, 13, and 15) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA875. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them.

Estimate the total capacitive load and set R_S from the plot of Figure 5. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA875 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the Distortion versus Load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA875 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA875 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be seriesterminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in Figure 5. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA875 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA875 onto the board.

INPUT AND ESD PROTECTION

The OPA875 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 31.

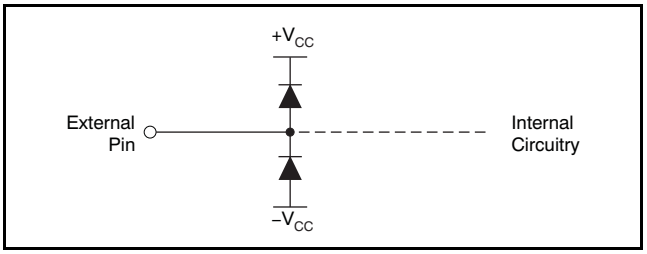


Figure 31. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA875), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

Revision History

Changes from Revision B (September 2007) to Revision C **Page**

- Changed storage temperature range rating in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C 2

Changes from Revision A (August 2007) to Revision B **Page**

- Changed ordering information column in Table 3. 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA875ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA875	Samples
OPA875IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA875	Samples
OPA875IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BPL	Samples
OPA875IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BPL	Samples
OPA875IDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	BPL	Samples
OPA875IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA875	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

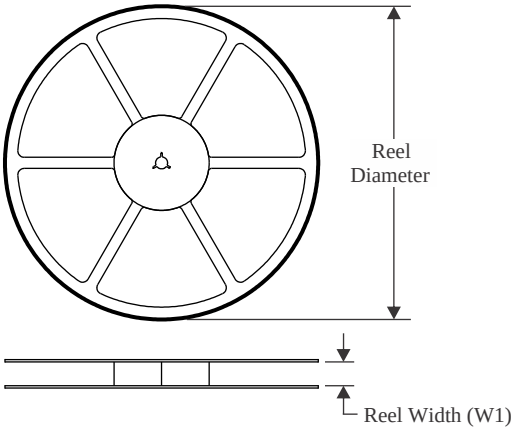
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

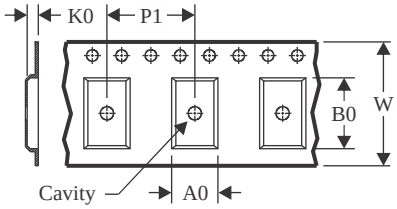
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

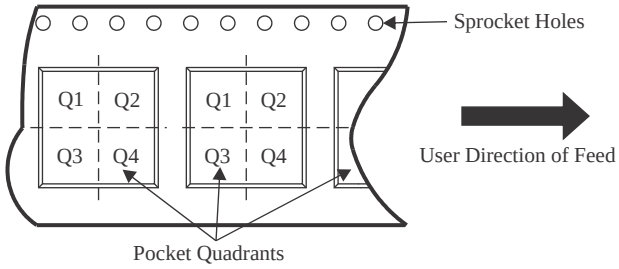


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

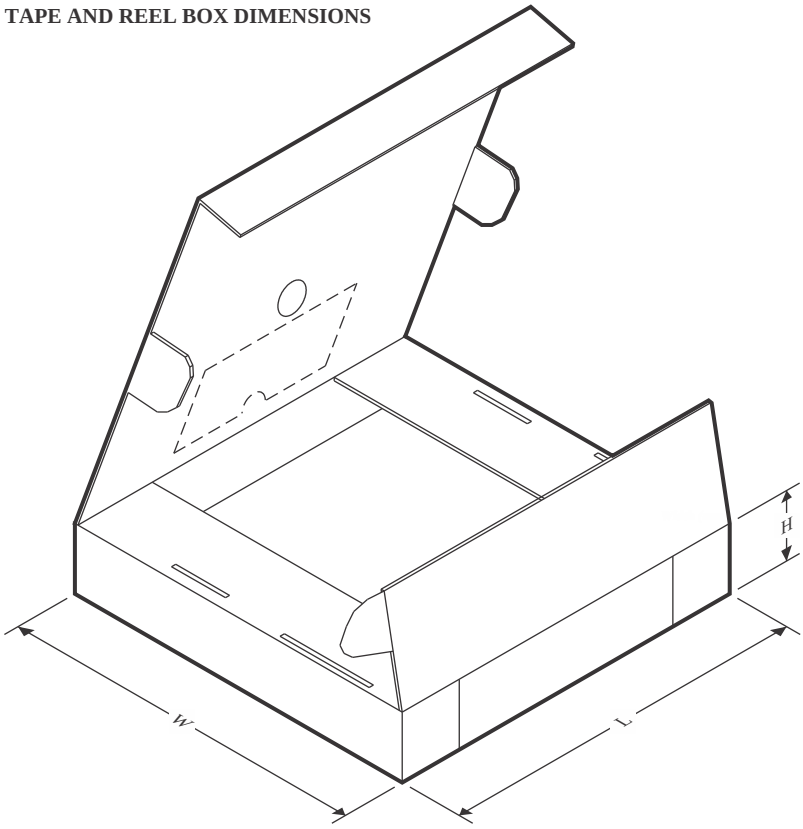
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA875IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA875IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

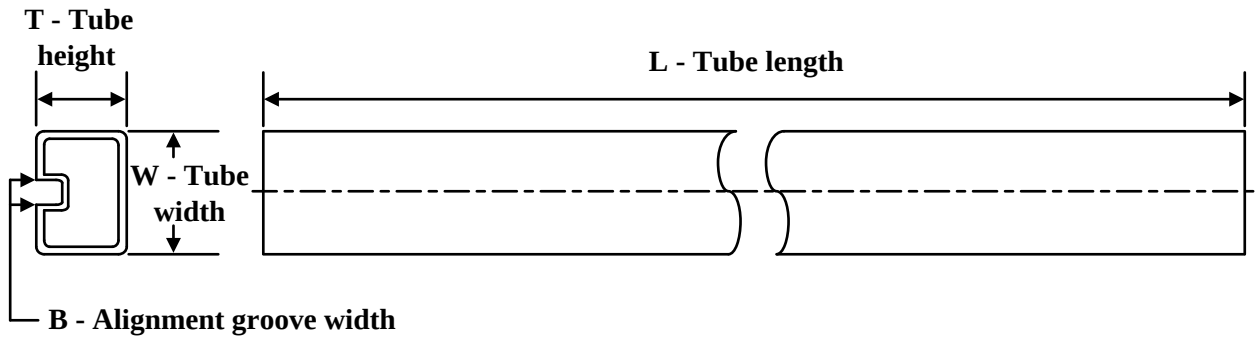
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

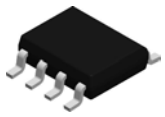
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA875IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA875IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA875ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA875IDG4	D	SOIC	8	75	506.6	8	3940	4.32

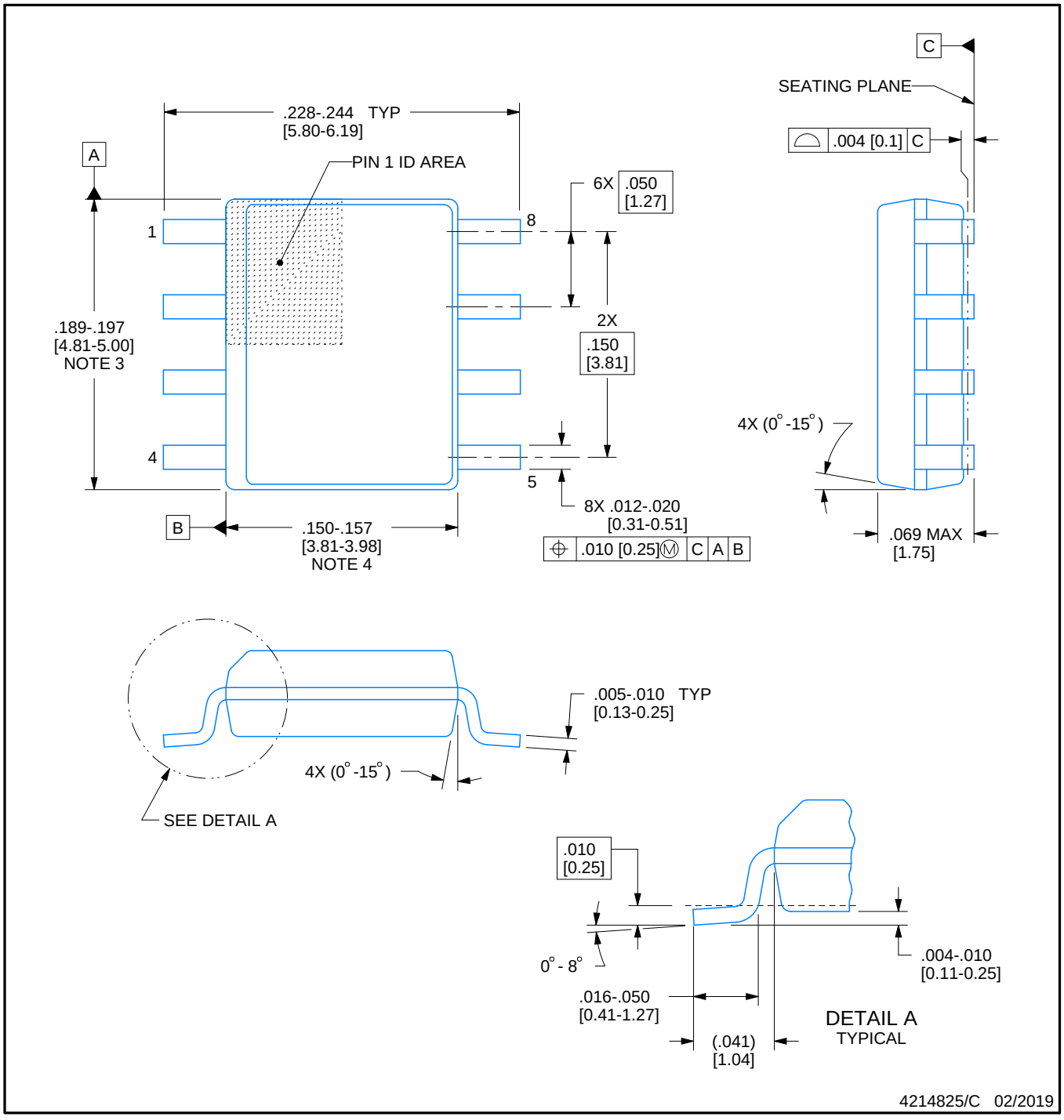


PACKAGE OUTLINE

D0008A

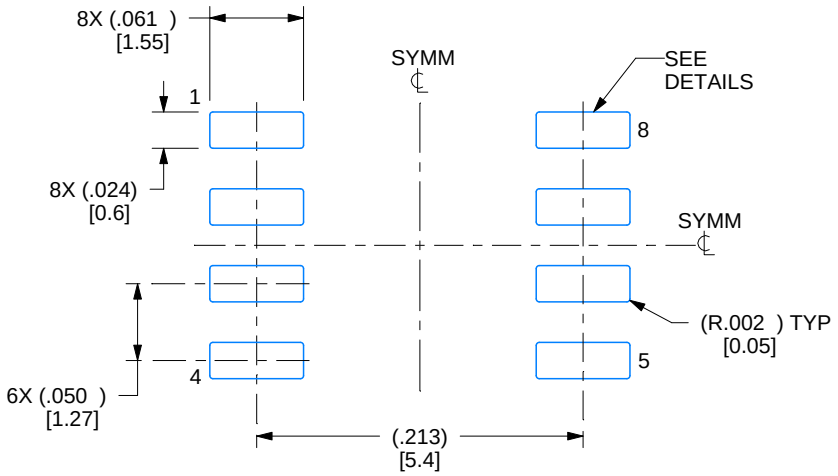
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

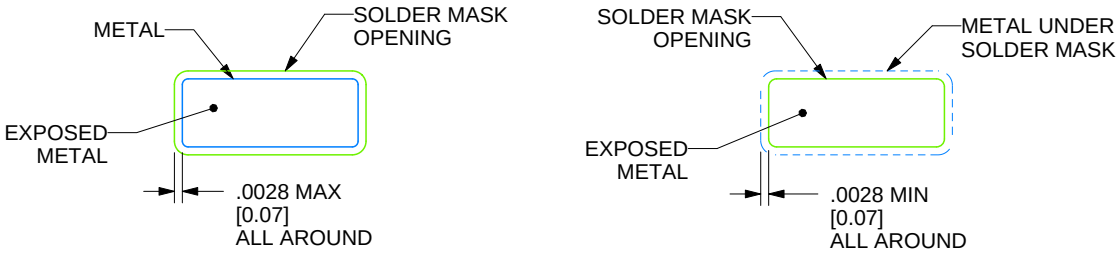


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

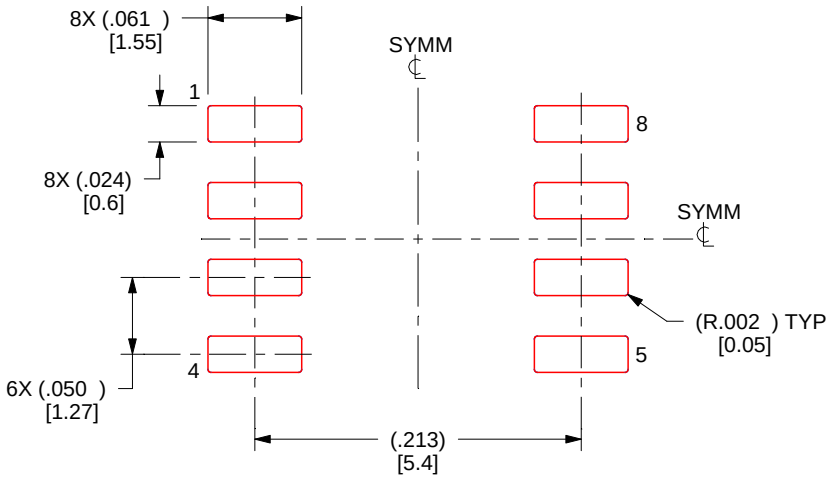
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



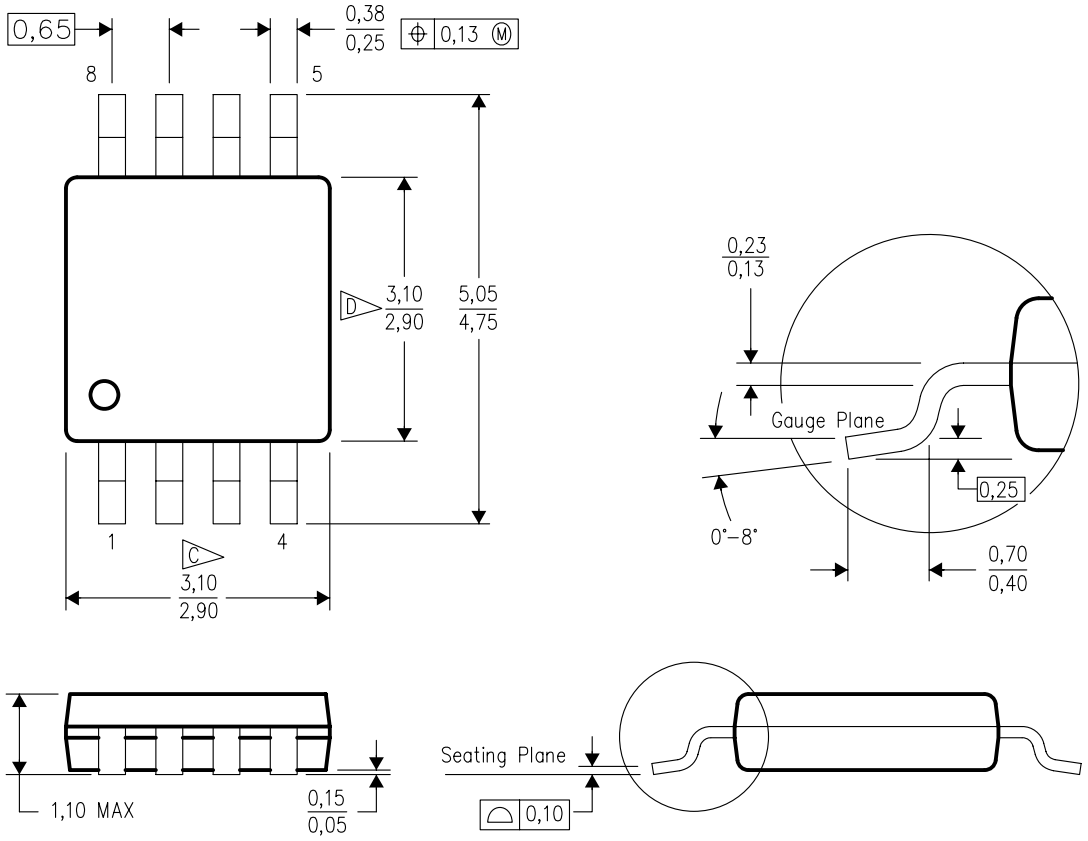
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

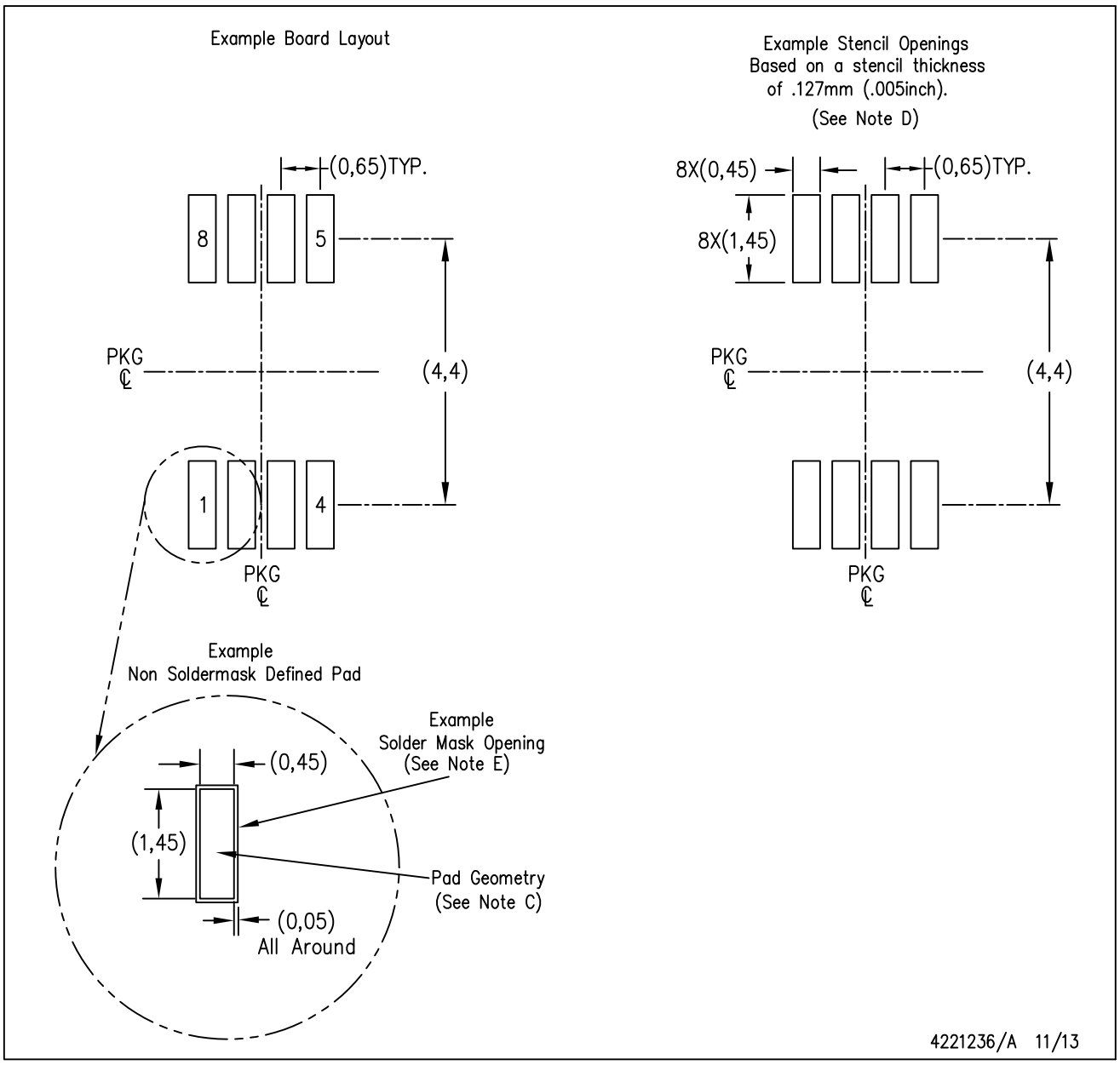
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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