FAIRCHILD SEMICONDUCTOR TM

April 1998

# FDS6680

## Single N-Channel Logic Level PWM Optimized PowerTrench™ MOSFET

### General Description

This N-Channel Logic Level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

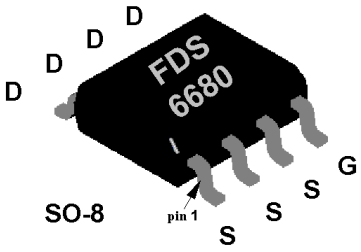
The MOSFET features faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

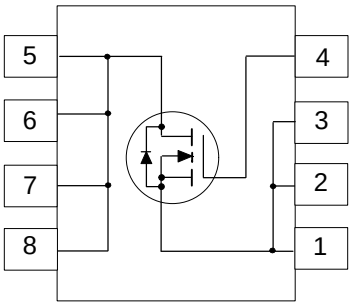
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 11.5 A, 30 V. $R_{DS(ON)}$ = 0.010 Ω @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 0.015 Ω @ $V_{GS}$ = 4.5 V.
- Optimized for use in switching DC/DC converters with PWM controllers.
- Very fast switching.
- Low gate charge (typical Qg = 19 nC).

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16




### Absolute Maximum Ratings $T_A$ = 25°C unless other wise noted

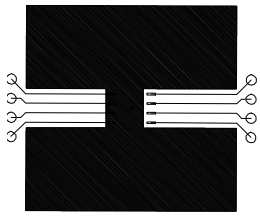
| Symbol | Parameter | | FDS6680 | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 11.5 | A |
| | - Pulsed | | 50 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

## Electrical Characteristics ($T_A$ = 25 °C unless otherwise noted )

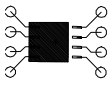
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 30 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | 23 | | mV/ °C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.7 | 3 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp.Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | -5 | | mV/°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 11.5 A | | 0.0085 | 0.01 | Ω |
| | | $T_J$ =125°C | | 0.014 | 0.017 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 9.5 A | | 0.0125 | 0.015 | |
| $I_{D(ON)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 50 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 11.5 A | | 40 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 2070 | | pF |
| $C_{oss}$ | Output Capacitance | | | 510 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 235 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DS}$= 15 V, $I_D$ = 1 A | | 13 | 21 | ns |
| $t_r$ | Turn - On Rise Time | $V_{GS}$ = 10 V , $R_{GEN}$ = 6 Ω | | 10 | 18 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 36 | 58 | ns |
| $t_f$ | Turn - Off Fall Time | | | 13 | 23 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15 V, $I_D$ = 11.5 A, | | 19 | 27 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = 5 V | | 7 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 6 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.1 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | | 1.2 | V |

Notes:

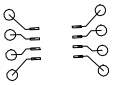
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W on a 1 in² pad of 2oz copper.



b. 105°C/W on a 0.04 in² pad of 2oz copper.



c. 125°C/W on a 0.006 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

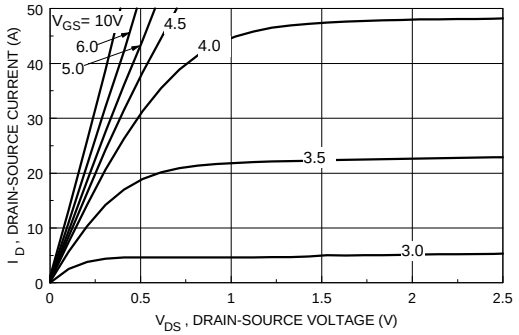



**Figure 1. On-Region Characteristics.**

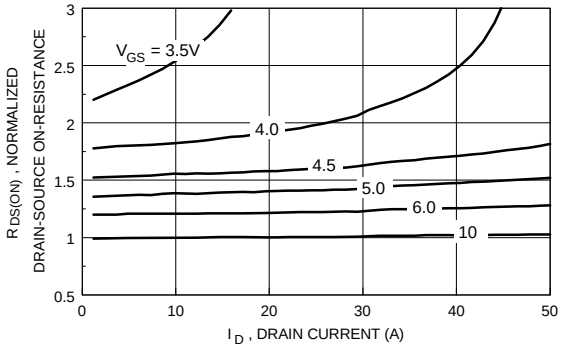



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

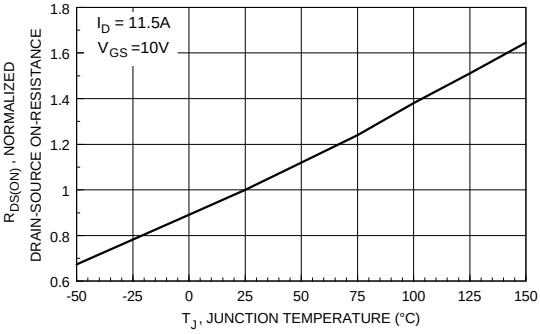



**Figure 3. On-Resistance Variation with Temperature.**

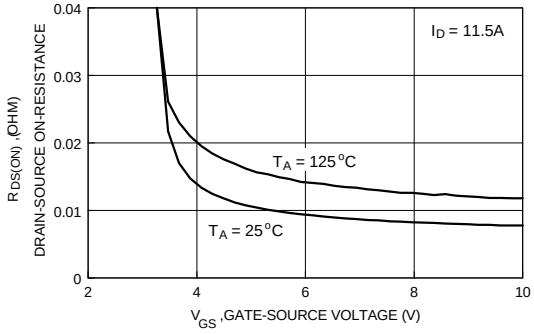



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

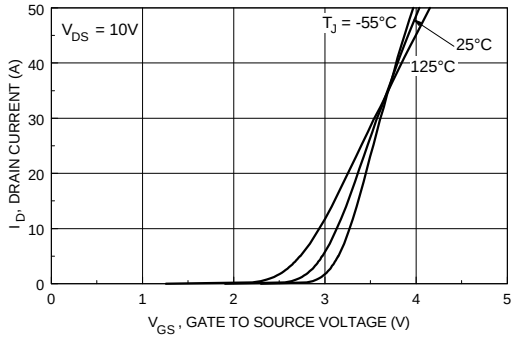



**Figure 5. Transfer Characteristics.**

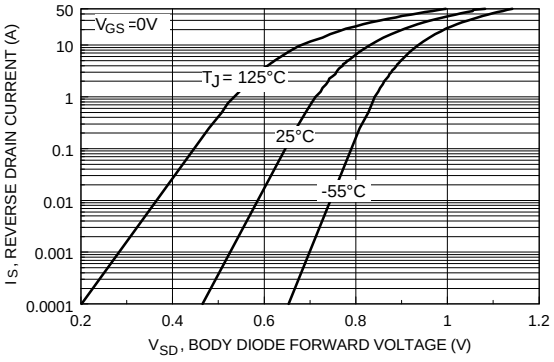



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical And Thermal Characteristics

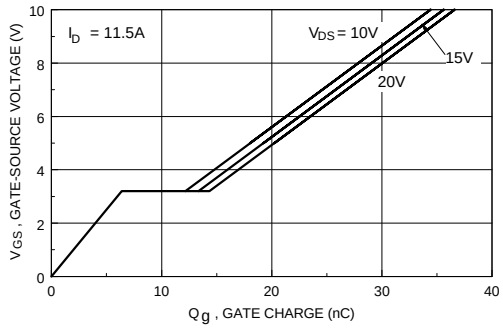



**Figure 7. Gate Charge Characteristics.**

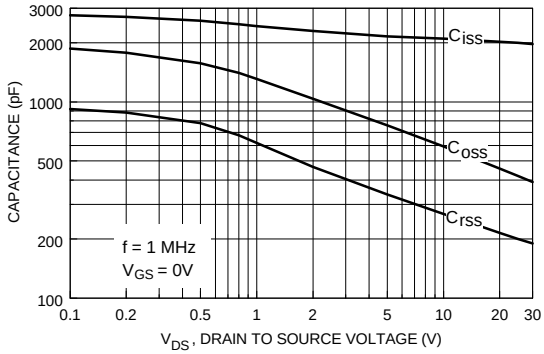



**Figure 8. Capacitance Characteristics.**

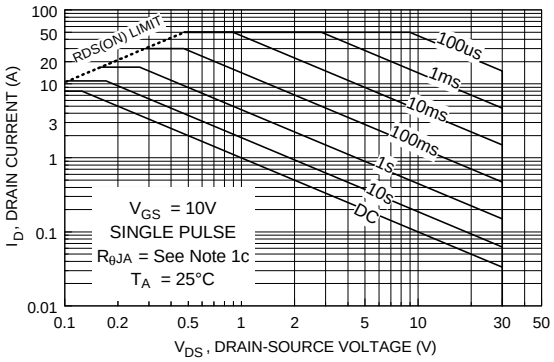



**Figure 9. Maximum Safe Operating Area.**

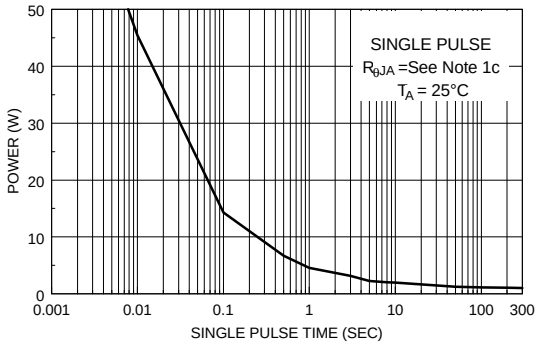



**Figure 10. Single Pulse Maximum Power Dissipation.**

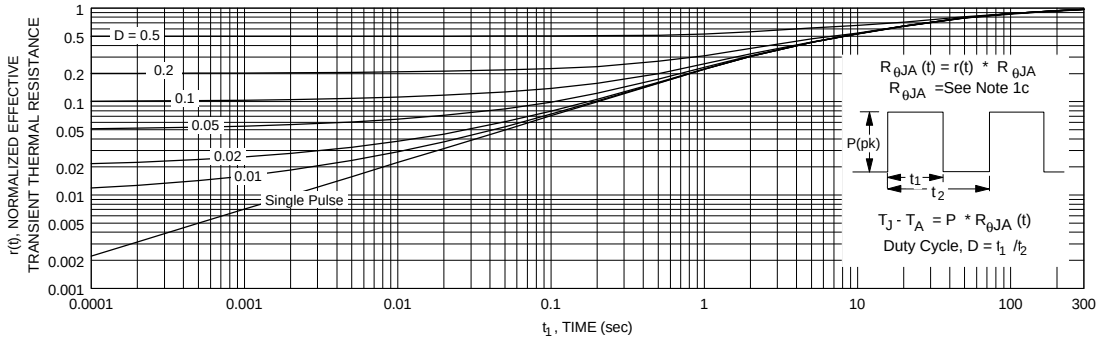



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.

Transient thermal response will change depending on the circuit board design.

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