

TLP701F

Industrial inverters
 Inverter for air conditioners
 IGBT/Power MOS FET gate drive

TLP701F consists of an infrared LED and an integrated photodetector.
 This unit is 6-lead SDIP package. The TLP701F is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The TLP701F is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP701 is capable of "direct" gate driving of low-power IGBTs.

- Peak output current : ± 0.6 A (max)
- Guaranteed performance over temperature : -40 to 100°C
- Supply current : 2 mA (max)
- Power supply voltage : 10 to 30 V
- Threshold input current : $I_{FLH} = 5$ mA (max)
- Switching time (t_{pLH} / t_{pHL}) : 700 ns (max)
- Common mode transient immunity : ± 10 kV/ μs (min)
- Isolation voltage : 5000 Vrms (min)
- Construction mechanical rating

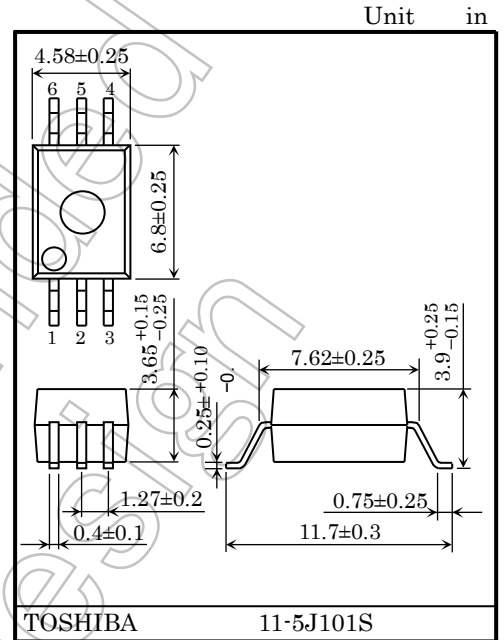
	10.16-mm pitch TLPXXXXF type
Creepage Distance	8.0 mm (min)
Clearance	8.0 mm (min)
Insulation Thickness	0.4 mm (min)

- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
File No.E67349
- VDE-approved: EN 60747-5-5, EN 62368-1 (Note 1)

Note 1 : When a VDE approved type is needed, please designate the **Option(D4)**.

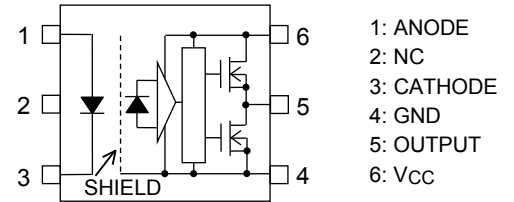
Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

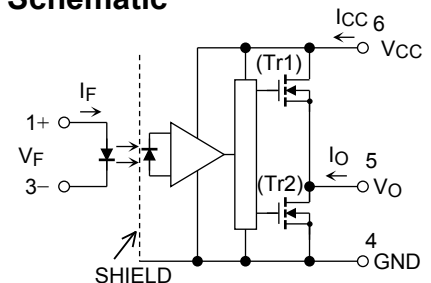


Weight : 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



A 0.1- μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
2004-04

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta ≥ 85°C)	ΔI _F /ΔTa	-0.54	mA/°C
	Pulse transient forward current (Note 1)	I _{FP}	1	A
	Reverse voltage	V _R	5	V
	Input power dissipation	P _D	40	mW
	Input power dissipation derating (Ta ≥ 85°C)	ΔP _D /ΔTa	-1.0	mW/°C
	Junction temperature	T _j	125	°C
Detector	"H" peak output current (Note 2)	I _{OPH}	-0.6	A
	"L" peak output current (Note 2)	I _{OPL}	0.6	A
	Output voltage	V _O	35	V
	Supply voltage	V _{CC}	35	V
	Output power dissipation	P _O	400	mW
	Output power dissipation derating (Ta ≥ 85°C)	ΔP _O /ΔTa	-1.0	mW/°C
	Junction temperature	T _j	125	°C
Operating frequency (Note 3)	f	25	kHz	
Operating temperature range	T _{opr}	-40 to 100	°C	
Storage temperature range	T _{stg}	-55 to 125	°C	
Lead soldering temperature (10 s) (Note 4)	T _{sol}	260	°C	
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 5)	BV _s	5000	V _{rms}	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 2 μs, f ≤ 15 kHz

Note 3: Exponential waveform I_{OPH} ≤ -0.3 A (≤ 2 μs), I_{OPL} ≤ +0.3 A (≤ 2 μs), Ta = 100 °C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 6)	I _F (ON)	7.5	—	10	mA
Input voltage, OFF	V _F (OFF)	0	—	0.8	V
Supply voltage	V _{CC}	10	—	30	V
Peak output current	I _{OPH} / I _{OPL}	—	—	± 0.2	A
Operating temperature	T _{opr}	-40	—	100	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 6: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.*	Max	Unit
Forward voltage		V _F	—	I _F = 5 mA, Ta = 25 °C		—	1.55	1.70	V
Temperature coefficient of forward voltage		ΔV _F /ΔTa	—	I _F = 5 mA		—	-2.0	—	mV/°C
Input reverse current		I _R	—	V _R = 5 V, Ta = 25 °C		—	—	10	μA
Input capacitance		C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Output current (Note 7)	"H" Level	I _{OPH1}	1	V _{CC} = 15 V I _F = 5 mA	V ₆₋₅ = 4 V	—	-0.38	-0.2	A
		I _{OPH2}			V ₆₋₅ = 10 V	—	-0.60	-0.4	
	"L" Level	I _{OPL1}	2	V _{CC} = 15 V I _F = 0 mA	V ₅₋₄ = 2 V	0.2	0.36	—	
		I _{OPL2}			V ₅₋₄ = 10 V	0.4	0.62	—	
Output voltage	"H" Level	V _{OH}	3	V _{CC} = 10 V	I _O = -100 mA, I _F = 5 mA	6.0	8.5	—	V
	"L" Level	V _{OL}			4	I _O = 100 mA, V _F = 0.8 V	—	0.4	
Supply current	"H" Level	I _{CCH}	5	V _{CC} = 10 to 30 V, V _O = Open	I _F = 10 mA	—	1.4	2.0	mA
	"L" Level	I _{CCL}			6	I _F = 0 mA	—	1.3	
Threshold input current	L → H	I _{FLH}	—	V _{CC} = 15 V, V _O > 1 V		—	2.5	5	mA
Threshold input voltage	H → L	V _{FHL}	—	V _{CC} = 15 V, V _O < 1 V		0.8	—	—	V
Supply voltage		V _{CC}	—	—		10	—	30	V

(*): All typical values are at Ta = 25°C

Note: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design. It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Note 7: Duration of IO time ≤ 50 μs, 1 pulse

Isolation Characteristics (Ta = 25 °C)

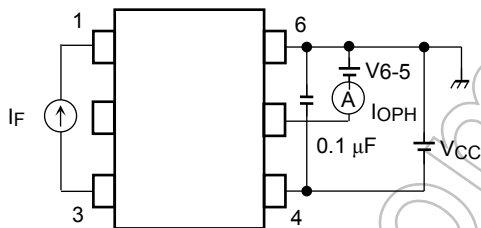
Characteristic	Symbol	Test Condition		Min	Typ.	Max	Unit
Capacitance input to output	C _S	V _S = 0 V, f = 1 MHz	(Note 5)	—	1.0	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V	(Note 5)	10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s	(Note 5)	5000	—	—	V _{rms}

Switching Characteristics (Ta = -40 to 100 °C, unless otherwise specified)

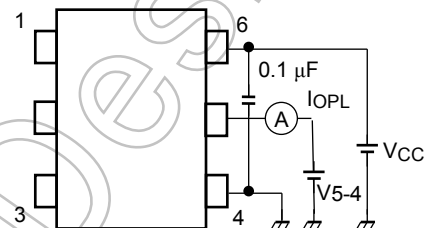
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	V _{CC} = 30 V R _g = 47 Ω C _g = 3 nF	I _F = 0 → 5 mA	100	—	700	ns
	H → L			t _{pHL}	I _F = 5 → 0 mA	100	—	
Output rise time (10–90 %)	t _r			I _F = 0 → 5 mA	—	50	—	
Output fall time (90–10 %)	t _f			I _F = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF	t _{pHL} - t _{pLH}			I _F = 0 ↔ 5 mA	—	—	500	
Common mode transient immunity at HIGH level output	CMH	8		V _{CM} = 1000 Vp-p V _{CC} = 30 V Ta = 25 °C	I _F = 5 mA V _O (min) = 26 V	-10000	—	—
Common mode transient immunity at LOW level output	CML		I _F = 0 mA V _O (max) = 1 V		10000	—	—	

(*): All typical values are at Ta = 25 °C.

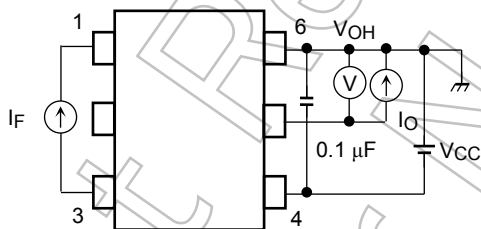
Test Circuit 1: I_{OPH}



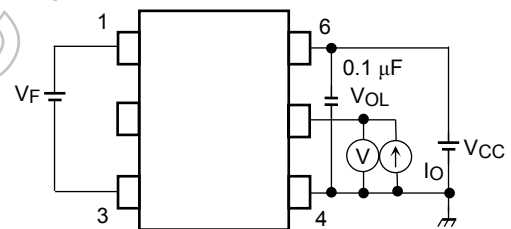
Test Circuit 2: I_{OPL}



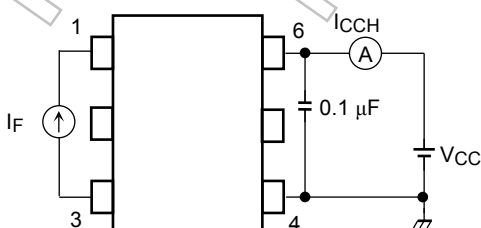
Test Circuit 3: V_{OH}



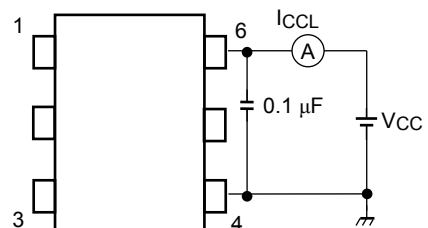
Test Circuit 4: V_{OL}



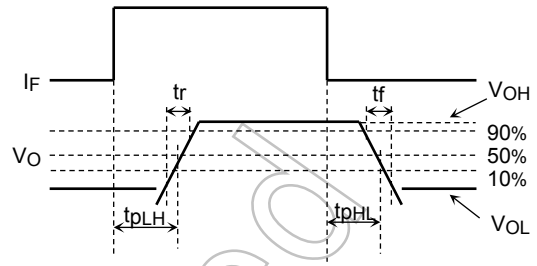
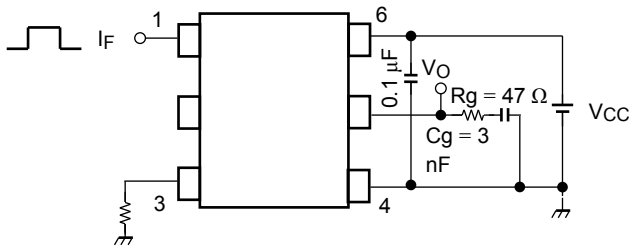
Test Circuit 5: I_{CCH}



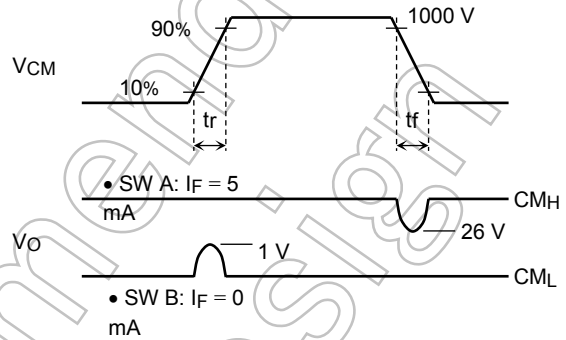
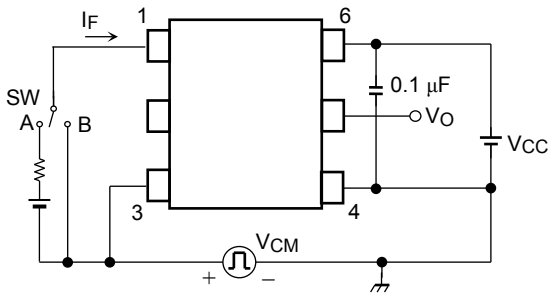
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , PDD



Test Circuit 8: CMH, CML



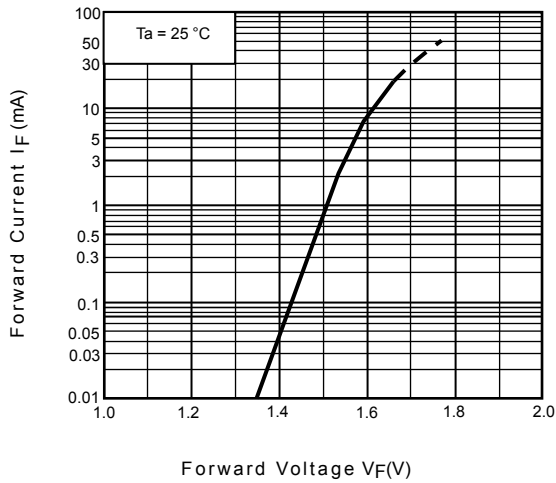
$$C_{ML} = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

$$C_{MH} = -\frac{800 \text{ V}}{t_f (\mu\text{s})}$$

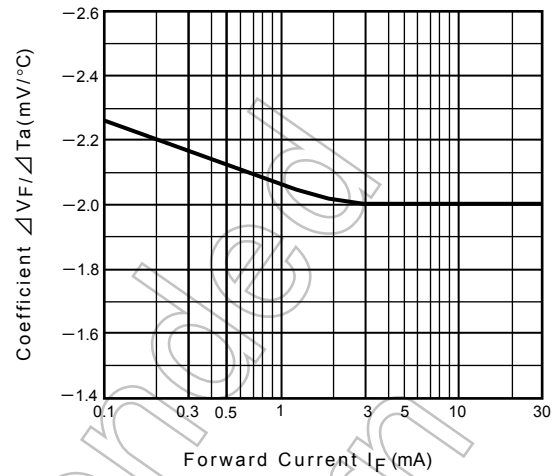
CML (CMH) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.

Not Recommended for New Design

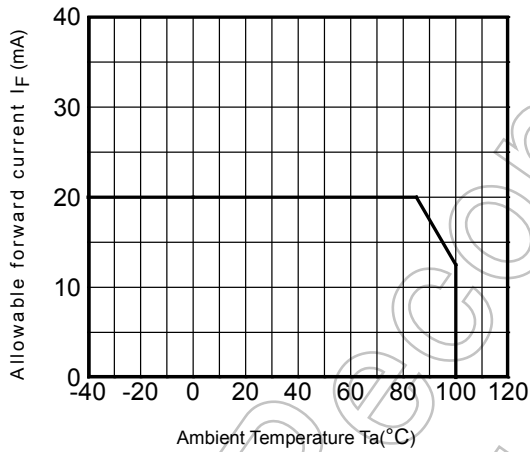
$I_F - V_F$



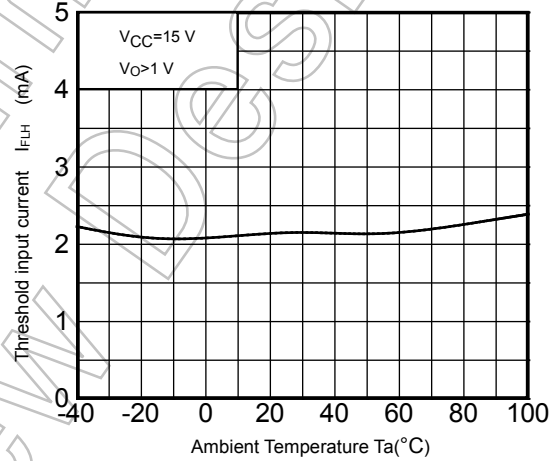
$\Delta V_F / \Delta T_a - I_F$



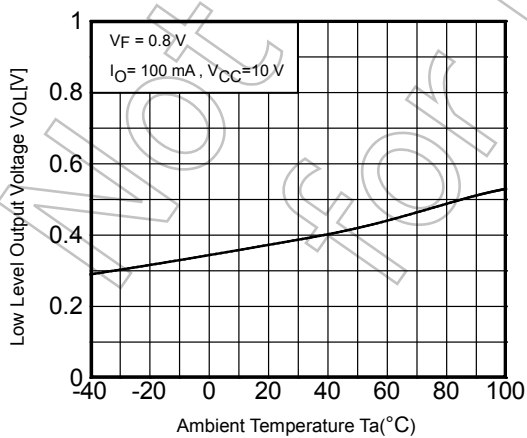
$I_F - T_a$



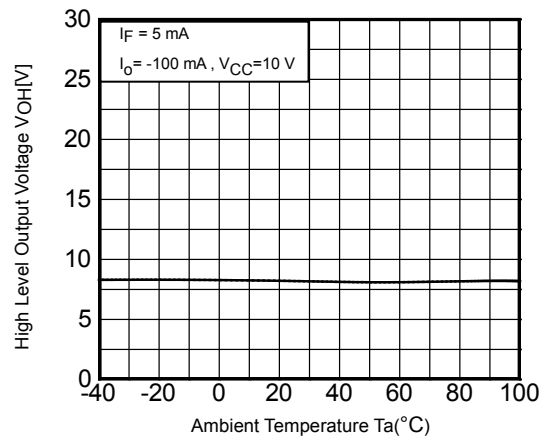
$I_{FLH} - T_a$



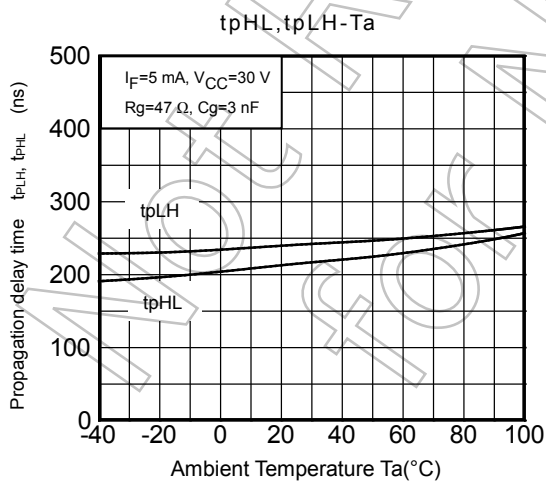
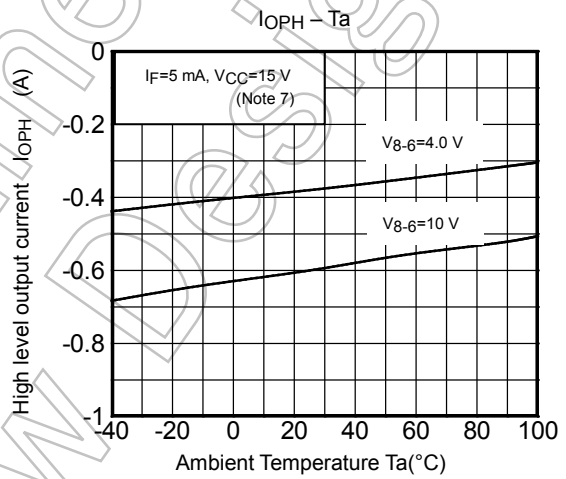
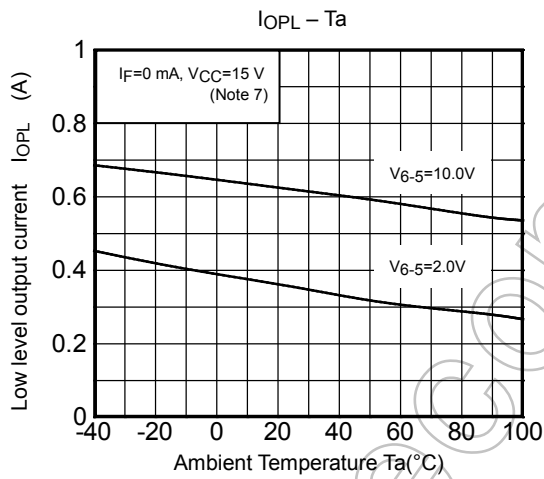
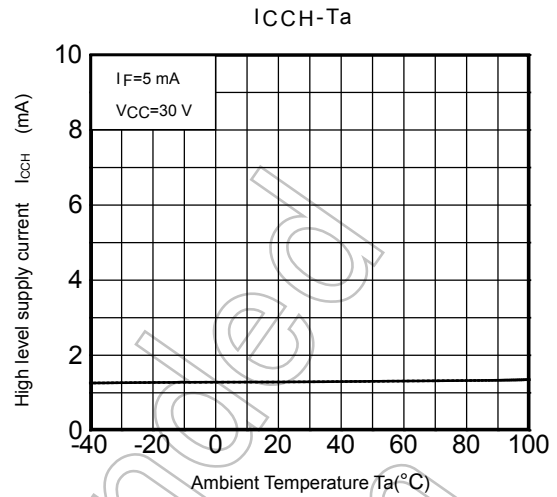
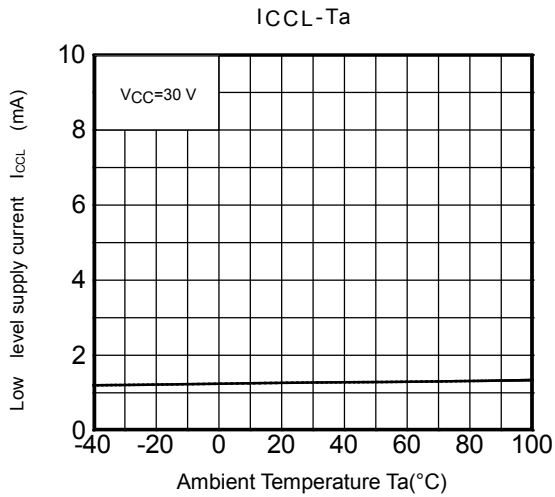
$V_{OL} - T_a$



$V_{OH} - T_a$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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