Product Update

UP006010-0508

Errata for Z8 Encore! XP® F64XX Series

Z8 Encore! XP® F64XX Series with Date Codes 0344 to 0519

The errata listed in Table 1 are found in Zilog's Z8 Encore! XP® F64XX Series devices with date codes 0344 to 0519, where the date code is YYWW (year and week of assembly). Date codes 0442 to 0519 are mixed; the errata will apply to some units, but not others. These errata are NOT APPLICABLE to date codes 0520 and later. When reviewing the following errata, it is recommended that you also download the most recent version of the Product Specification.

Table 1. Z8 Encore! XP F64XX Series Errata Date Code 0344 to 0519

Sl No.	Summary	Description
1	Read protect (RP) option bit may be bypassed.	The RP option bit does not prevent Flash access when bypassing the Flash controller. For more information, refer to *Third Party Flash Programming Support for Z8 Encore!® MCU Application Note (AN0117)*. User code cannot be read through the on-chip debugger when read protect is enabled. User code can only be read out when bypassing the Flash controller. **Workaround** None
2	START, STOP and NAK bits in the I^2C control register can be cleared by software writing a 0 to these bits.	The START, STOP, and NAK bits in the I^2C control register can be cleared by software writing a 0 to these bits. The Product Specification states that they cannot be cleared by writing a 0. **Workaround** None
3	Device may not complete Stop Mode Recovery initiated by a general-purpose input/output (GPIO) pin transition.	When Stop Mode Recovery is initiated by a GPIO pin transition, multiple pin transitions within 200 µs (approximate) of each other may cause the device to only partially wake up from STOP mode. Therefore, the device idles in a state between STOP mode and normal operation. The crystal oscillator is oscillating, but code does not execute. When stuck in this idle state, assertion of the external $\overline{\text{RESET}}$ pin does not initiate a system reset. **Workaround** The workarounds are listed below: • Add external filtering to the Stop Mode Recovery pin input signal to prevent multiple transitions in less than 200 µs. • Enable the Watchdog Timer (WDT) in STOP mode to allow a WDT to complete the Stop Mode Recovery in the event the device does not successfully complete the Stop Mode Recovery initiated by the GPIO pin transition.

Z8 Encore! XP® F64XX Series with Date Codes Prior to 0344

The errata listed in Table 2 are found in the production Z8 Encore! XP® F64XX Series devices with date codes prior to 0344, where the date code is YYWW (year and week of assembly). When reviewing the following errata, it is recommended that you also download the most recent version of the Product Specification.

Table 2. Z8 Encore! XP F64XX Series Errata Date Coded Prior to 0334

SI No.	Summary	Description
1	When the CPU exits from HALT mode, it fails to reset the master Interrupt Request Enable (IRQE) bit.	When the CPU exits from HALT mode, it fails to reset the master Interrupt Request Enable (IRQE) bit (bit 7 of the Interrupt Control Register). WDT interrupts cause the program counter (PC) and Flags to be pushed twice on the stack. The first push is the PC and Flags from where the interrupt occurred. The second push is the starting address and Flags of the Interrupt service routine (ISR). This problem also affects exits from HALT mode caused by other interrupt sources if more than one interrupt is pending. If only a single interrupt is pending then, the routine is executed normally except that interrupts are not disabled **Workaround** To mimic standard interrupt operation, the ISR should execute a disable interrupts (DI) instruction to reset the master Interrupt Request enable (IRQE) bit to 0. Further, on WDT interrupts before exiting, the ISR should add three to the stack pointer (SP). On normal interrupts, the ISR should check the program counter on the stack. If the PC on the stack contains the starting address of the ISR, then the ISR should add three to the stack pointer. This problem only affects exits from HALT mode.
2	System reset latency may exceed specification limits.	When exiting STOP mode and after a Power-On Reset (POR)/Voltage Brown-out (VBO) reset, the system reset Latency is 514 WDT cycles plus 16 system clock cycles rather than the 66 WDT cycles plus 16 system clock cycles as specified. **Workaround** None. This error is unlikely to affect system operation.
3	UART NEWFRM status bit does not function.	The NEWFRM status bit (bit 2 of the UART Status 1 register) does not indicate the start of a new frame. **Workaround** None

Table 2. Z8 Encore! XP F64XX Series Errata Date Coded Prior to 0334 (Continued)

Sl No.	Summary	Description
4	UART address compare function does not work.	Setting bit 7 (MPMD[1]) of the UART control 1 register to 1 does not produce the desired effect of enabling the UART address compare and associated interrupt functionality. **Workaround** Leave MPMD[1] in its reset state of 0.
5	UART baud rate generator cannot be used as simple timer.	Setting BRGCTL (bit 2 of the UART Control 1 register) to 1 when the UART receiver is disabled does not enable UART baud rate generator interrupt. Thus, the UART baud rate generator cannot be used as a simple timer. **Workaround** Use one of the four standard timers or the baud rate generators in the SPI or I^2C blocks to perform the desired timing operations.
6	Unlocking the Flash controller allows program and erase operations on all Flash pages.	During the Flash controller unlock sequence, the specification indicates that a second write to the Flash Page Select register is required (step 5 of the sequence) to unlock the Flash controller for the selected Flash page. The Flash controller unlocks for all Flash pages once the step 1 to step 4 of the unlock sequence are complete. **Workaround** None
7	Setting bits in the Flash sector protect register to 1 does not lock sectors.	Writing bits in the Flash sector protect register to 1 fails to prevent program and erase operations on the selected Flash memory sector. **Workaround** None
8	Watchdog Timer cannot be disabled in STOP mode.	The Watchdog Timer and its associated internal RC oscillator cannot be disabled in STOP mode. **Workaround** None
9	Watchdog Timer oscillator frequency is out of specification.	The typical Watchdog Timer internal oscillator frequency is 50 kHz rather than the currently specified 10 kHz. This frequency can result in WDT time-out values that are less than expected. **Workaround** Increase the WDT reload value by a factor of 5 to compensate for the frequency error.
10	Operating currents.	Operating currents in the various mode (NORMAL, HALT, and STOP) may be higher than typical values. **Workaround** None

Table 2. Z8 Encore! XP F64XX Series Errata Date Coded Prior to 0334 (Continued)

Sl No.	Summary	Description
11	$\overline{\text{RESET}}$ pin is not filtered.	The $\overline{\text{RESET}}$ pin does not properly filter the input signal. The device may enter Reset when the $\overline{\text{RESET}}$ pin is asserted for less than the specified four system clock cycles (from NORMAL mode). **Workaround** Add external filtering to the printed-circuit board.
12	Timers cannot be cascaded.	Setting the CSC bit (bit 4) of the Timer Control 0 Registers does not cascade the timers as indicated in the specification. **Workaround** Timers can be cascaded using the Timer-Out and Timer-In functions through the general-purpose I/O pins.
13	ADC generates extra interrupts.	The ADC continues to generate interrupts in CONTINUOUS mode after the first interrupt before the results of the next conversion is complete. **Workaround** Do not use CONTINUOUS mode. Use SINGLE-SHOT mode instead.

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