TPS65133 ±5-V, 250-mA Dual-Output Power Supply

1 Features

- 2.9-V to 5.0-V Input Voltage Range
- Fixed 5.0-V Positive Output Voltage (V_{POS})
- Fixed –5.0-V Negative Output Voltage (V_{NEG})
- ±1% Output Voltage Accuracy
- High Efficiency
- 250-mA Output Current Capability
- Independent Converter Operation Allows 100% Output Current Mismatch
- Excellent Line and Load Transient Response
- Operates in CCM to Minimize Output Noise
- Boost Converter able to Operate with Input Supply Voltages close to 5.0 V
- Short-Circuit Protection
- Thermal Shutdown

2 Applications

- LCD Bias
- AMOLED Supplies
- Operational Amplifier Supplies
- Headphone Amplifier Supplies
- Sensor Front-End Supplies
- Data Acquisition Supplies
- General ±5-V Power Supplies

3 Description

The TPS65133 is designed to supply any system requiring ±5.0-V supply rails. Each output can supply up to 250 mA of output current. The input supply voltage range is suitable for use with lithium ion batteries or from a fixed 3.3-V supply.

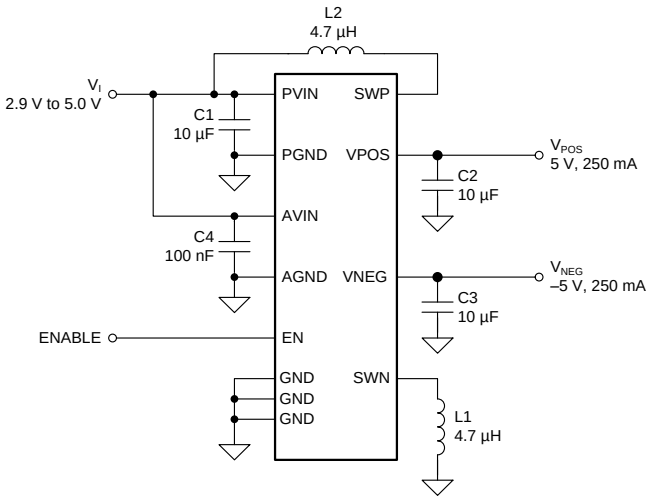
Efficiency is typically over 90% for most applications (operating from a lithium ion battery, output currents in the range 50 mA to 200 mA). The two converters in the TPS65133 device operate independently, allowing 100% mismatch between positive and negative output currents.

Device Information[1]

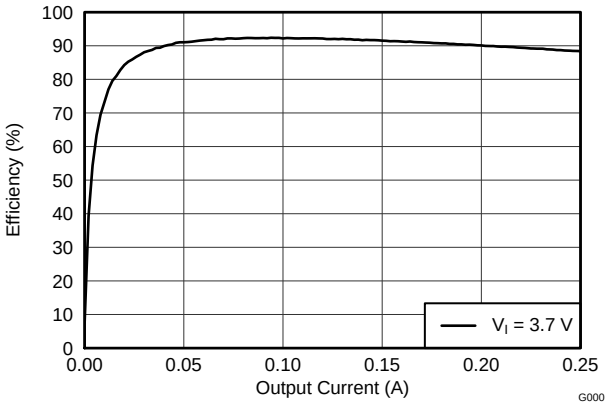
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65133	WSON (12)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application



Efficiency



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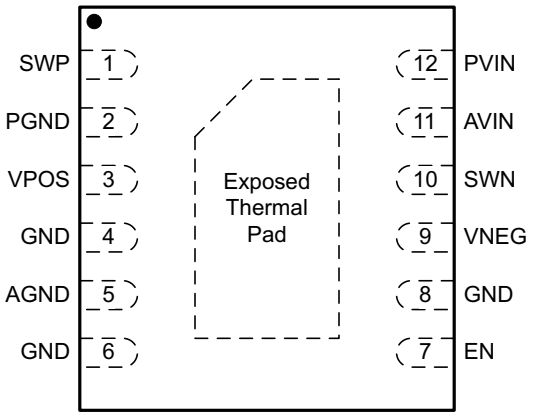
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2013) to Revision A	Page
• Added Device Information table, ESD Ratings table, Switching Characteristics table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
• Changed Layout Example	17

6 Pin Configuration and Functions

DPD Package
12-Pin WSON
(Top View)



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	5	Analog ground
AVIN	11	Internal logic supply pin
EN	7	Enable of boost and buck-boost converter
GND	4, 6, 8	Ground
SWP	1	Switch pin of the boost converter
PGND	2	Power ground of the boost converter
PVIN	12	Supply pin for the negative buck-boost converter. Place a capacitor close to this pin.
SWN	10	Switch pin of the negative buck-boost converter
VNEG	9	Output of the negative buck-boost converter (V_{NEG}), place a capacitor close to this pin.
VPOS	3	Output of the boost converter (V_{POS}), place a capacitor close to this pin.
Exposed thermal pad		Exposed thermal pad. Connect this pad to all GND pins.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage(2)	PVIN, AVIN, EN, SWP, VPOS	–0.3	6	V
	VNEG	–6.5	0.3	V
	SWN	–6.5	5.5	V
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to GND pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.9	3.7	5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Refer to the *Application Information* section for additional information.

7.4 Thermal Information

THERMAL METRIC(1)		TPS65133 DPD (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	25	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	25.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_I = 3.7 V, EN = V_I, V_{POS} = 5.0 V, V_{NEG} = –5.0 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT AND THERMAL PROTECTION						
V_I	Input voltage		2.9		5	V
	Shut down supply current	EN = GND $I_{(IN)} = I_{(AVIN)} + I_{(PVIN)} + I_{(SWP)}$		0.1	15	µA
	Undervoltage lockout threshold	V_I falling			2.1	V
	Undervoltage lockout threshold	V_I rising			2.5	V
	Thermal shutdown temperature			135		°C
LOGIC SIGNALS (EN)						
	High-level input voltage		1.2			V
	Low-level input voltage				0.4	V
BOOST CONVERTER (V_{POS})						
V_{POS}	Output voltage		4.95	5	5.05	V
	Low-side MOSFET on-state resistance	$I_{(SWP)}$ = 200 mA		250		mΩ
	High-side MOSFET on-state resistance	$I_{(SWP)}$ = –200 mA		350		
	High-side MOSFET current limit	Inductor valley current	0.8	1.1		A
$V_{(SCP)(P)}$	Short-circuit threshold in operation	V_{POS} falling		4.1		V
	Active discharge resistance	EN = GND; $I_{(VPOS)}$ = 1 mA	15	30	60	Ω
	Line regulation	I_{POS} = 100 mA		0.02		%/V
	Load regulation			0.24		%/A
BUCK-BOOST CONVERTER (V_{NEG})						
V_{NEG}	Negative output voltage default		–5.05	–5	–4.95	V
	High-side MOSFET on-state resistance	$I_{(SWN)}$ = –200 mA		250		mΩ
	Low-side MOSFET on-state resistance	$I_{(SWN)}$ = 200 mA		350		
	Low-side MOSFET current limit	Inductor valley current	1.5	2.2		A
$V_{(SCP)(N)}$	Short-circuit threshold in operation			–4.5		V
	Active discharge resistance	EN = GND; $I_{(VNEG)}$ = –1 mA	100	150	200	Ω
	Line regulation	I_{NEG} = –100 mA		0.01		%/V
	Load regulation			0.16		%/A

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER (V_{POS})						
	Switching frequency	I_{POS} = 200 mA	1.2	1.7	2.2	MHz
	Short-circuit detection time	The delay from when $V_{POS} < V_{(SCP)(P)}$ to when the boost converter turns off	1	3	5	ms
BUCK-BOOST CONVERTER (V_{NEG})						
	Switching frequency	I_{NEG} = –200 mA	1	1.7	2.4	MHz
	Short-circuit detection time	The delay from when $V_{NEG} > V_{(SCP)(N)}$ to when the inverting buck-boost converter turns off	1	3	5	ms
	Start-up delay	The delay from when V_{POS} has reached its target value to when V_{NEG} starts ramping		2		ms

7.7 Typical Characteristics

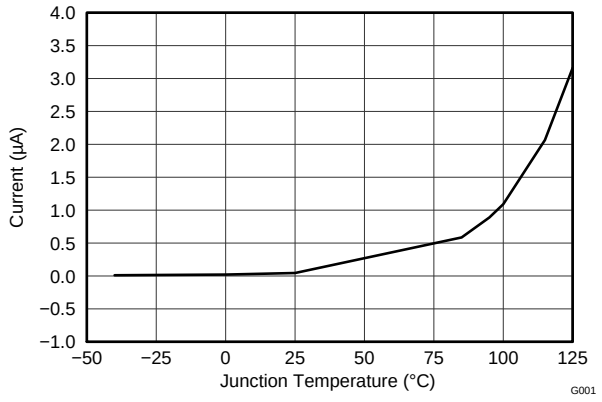


Figure 1. Shutdown Current into AVIN and PVIN

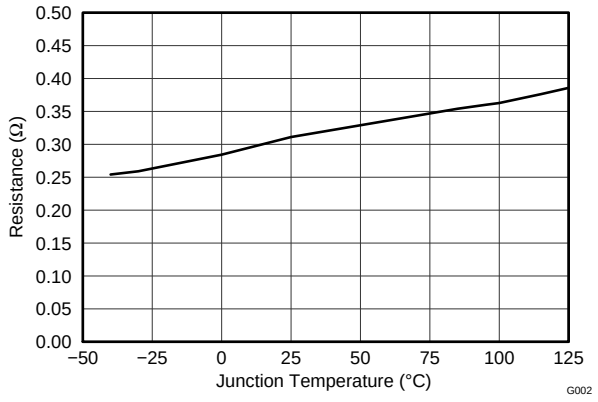


Figure 2. Boost Converter Switch $r_{DS(on)}$

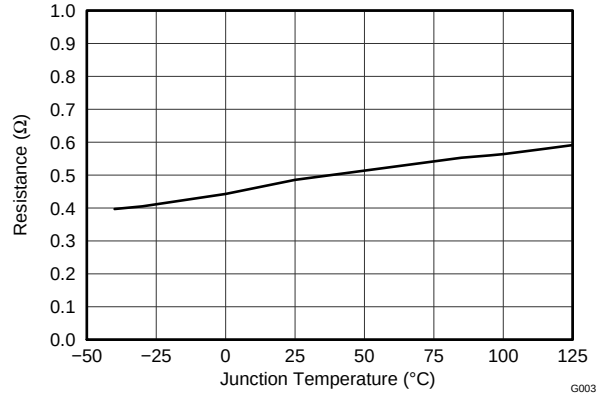


Figure 3. Boost Converter Rectifier $r_{DS(on)}$

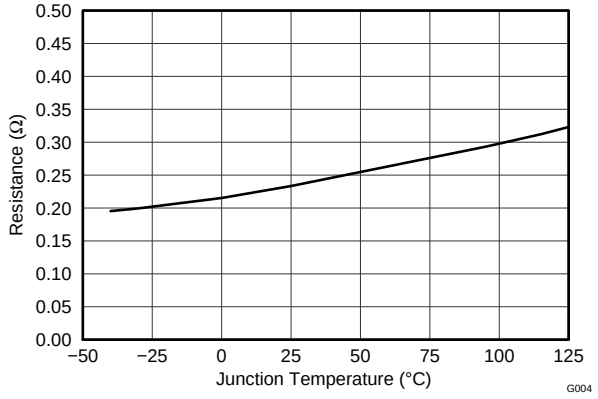


Figure 4. Inverting Buck-Boost Converter Switch $r_{DS(on)}$

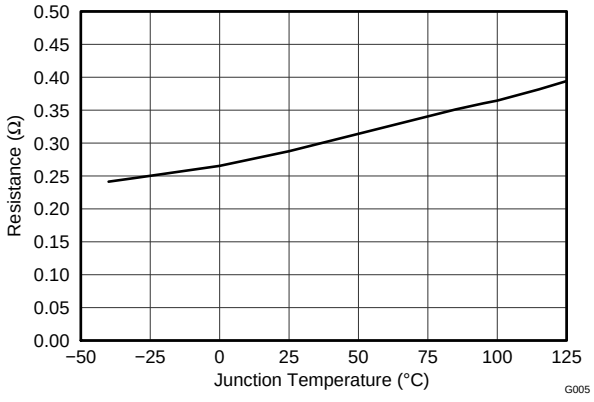


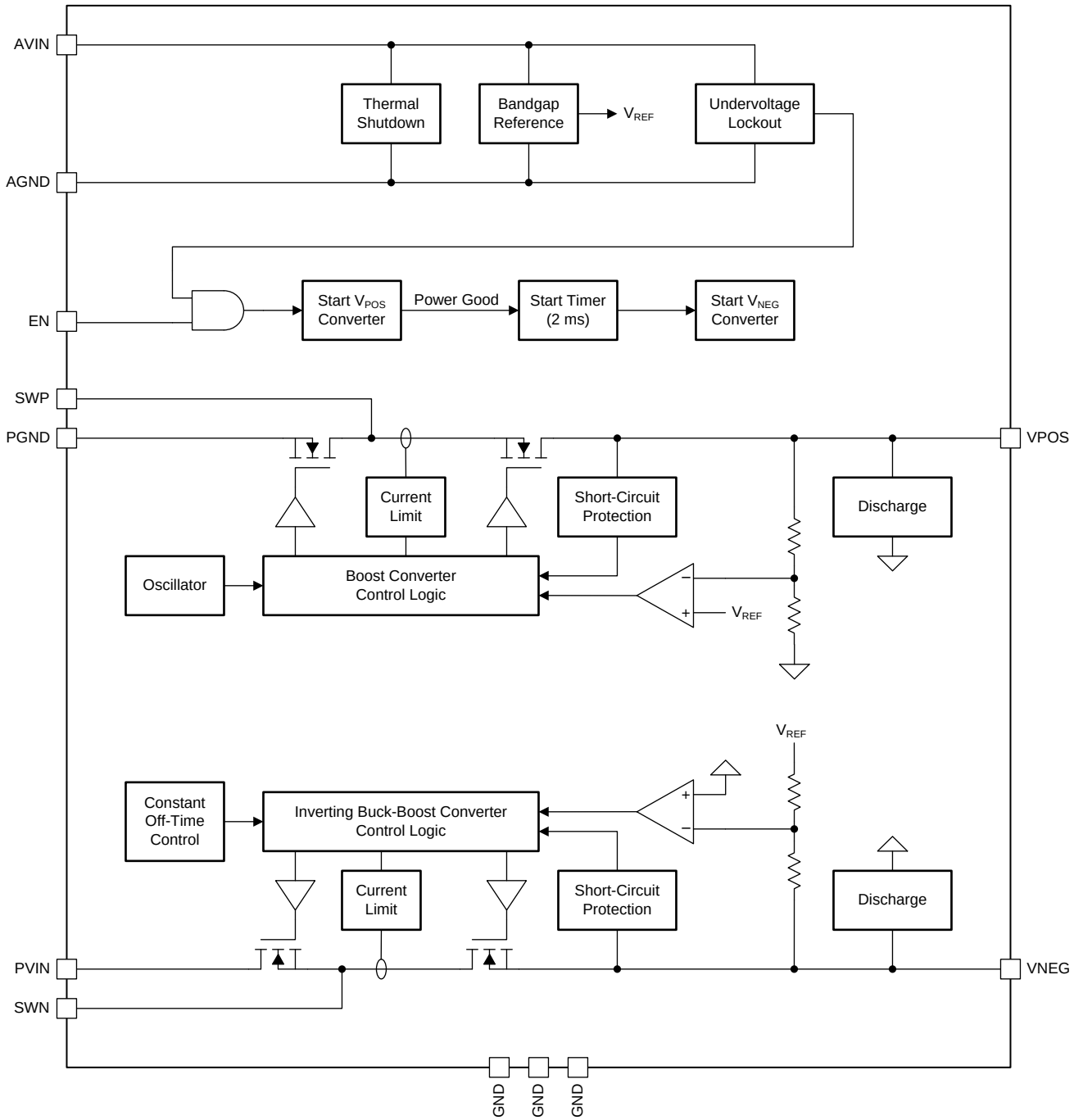
Figure 5. Inverting Buck-Boost Converter Rectifier $r_{DS(on)}$

8 Detailed Description

8.1 Overview

The TPS65133 device comprises a boost converter and an inverting buck-boost converter. The boost converter generates a positive output voltage of 5.0 V and the inverting buck-boost converter generates a negative output voltage of –5.0 V. Both converters have an output voltage accuracy of ±1%.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter (V_{POS})

The boost converter uses a current-mode topology with synchronous rectification (see Figure 6). The synchronous rectifier improves efficiency and provides input-output isolation when the converter is disabled. When the input supply voltage is close 5.0 V, preventing normal boost operation, the synchronous rectifier is disabled, allowing the output voltage regulation to be maintained (see *Operation with $V_I \approx V_{POS}$ (Diode Mode)*).

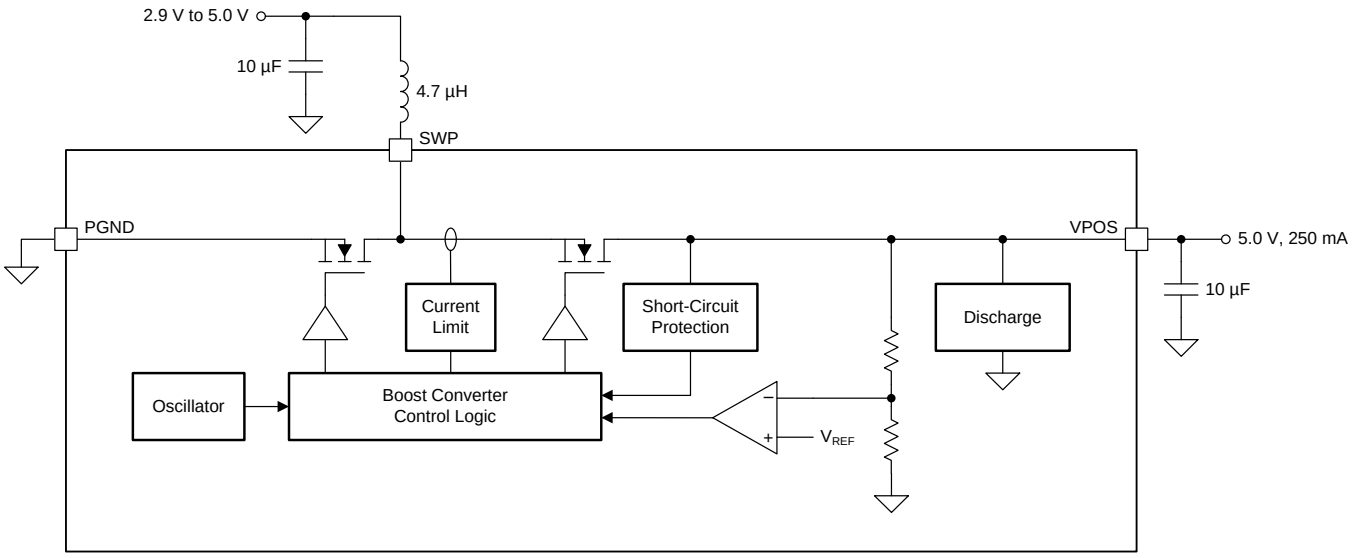


Figure 6. V_{POS} Boost Converter Internal Block Diagram

8.3.1.1 Switching Frequency (V_{POS})

The boost converter switching frequency may vary slightly as the operating conditions change, but is typically around 1.7 MHz for most operating conditions.

8.3.1.2 Output Voltage (V_{POS})

The boost converter's output voltage is factory-programmed to 5.0 V ±1.0% and cannot be changed by the user.

8.3.1.3 Startup (V_{POS})

The boost converter starts up as soon as EN=HIGH and the input supply voltage is above the UVLO threshold. The converter features an integrated soft-start function to control the ramp of its output voltage.

8.3.1.4 Shutdown (V_{POS})

The boost converter shuts down when EN=LOW or the input supply voltage falls below the UVLO threshold.

8.3.1.5 Active Discharge (V_{POS})

The boost converter output is actively discharged to ground when the converter is disabled (see Figure 8). During startup, active discharge begins as soon as the input supply voltage is above the UVLO threshold. During shutdown, active discharge persists until the input supply voltage is too low to support its operation ($V_I \approx 1.5$ V).

8.3.1.6 Short-Circuit Protection (V_{POS})

The boost converter is protected against short-circuits on its output. If a short-circuit condition is detected during start-up, the converter limits its output current until the short-circuit condition is removed. Note that if a boost converter short-circuit condition is detected during start-up, the inverting buck-boost converter will not start until the condition is removed (because the sequencing logic requires V_{POS} to be in regulation before the inverting buck-boost converter is started).

Feature Description (continued)

During normal operation the boost converter detects a short-circuit on its output if V_{POS} < 4.1 V for longer than 3 ms. When a short-circuit condition is detected both V_{POS} and V_{NEG} are disabled and the device shuts down. Normal operation is resumed by pulling EN low and then high again, or by cycling the input supply voltage.

8.3.2 Inverting Buck-Boost Converter (V_{NEG})

The inverting buck-boost converter uses a current-mode topology with synchronous rectification (see Figure 7).

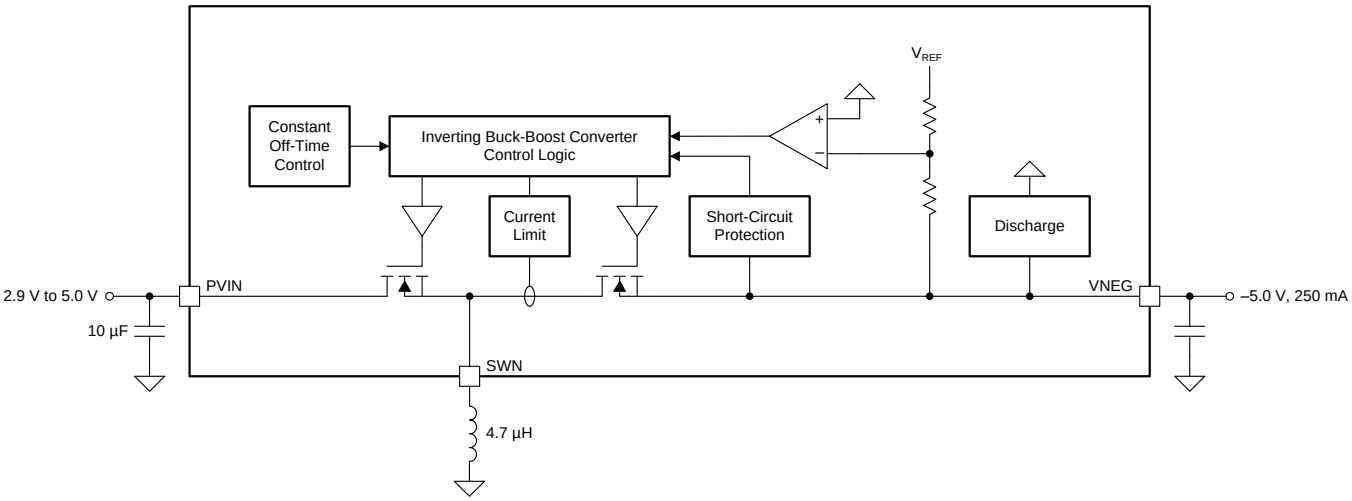


Figure 7. V_{NEG} Buck-Boost Converter Internal Block Diagram

8.3.2.1 Switching Frequency (V_{NEG})

The inverting buck-boost converter's switching frequency varies slightly with operating conditions, but is approximately 1.7 MHz for most operating conditions.

8.3.2.2 Output Voltage (V_{NEG})

The inverting buck-boost converter's output voltage is factory-programmed to –5.0 V ±1.0% and cannot be changed by the user.

8.3.2.3 Startup (V_{NEG})

The inverting buck-boost converter starts up approximately 2 ms after the boost converter output has reached 5.0 V. The converter's switch current is limited during startup and the output voltage ramps in a controlled manner.

8.3.2.4 Shutdown

The inverting buck-boost converter shuts down when EN=LOW or the input supply voltage falls below the UVLO threshold.

8.3.2.5 Active Discharge (V_{NEG})

The inverting buck-boost converter output is actively discharged to ground when the converter is disabled (see Figure 8). During startup, active discharge begins as soon as the input supply voltage is above the UVLO threshold. During shutdown, active discharge persists until the input supply voltage is too low to support its operation (V_I ≈ 1.5 V).

8.3.2.6 Short-Circuit Protection (V_{NEG})

The inverting buck-boost converter is protected against short-circuits on its output. If a short-circuit condition is detected during startup, the device converter limits its output current until the short-circuit condition is removed.

Feature Description (continued)

During normal operation the inverting buck-boost converter detects a short-circuit on its output if V_{NEG} > –4.5 V for longer than 3 ms. When a short-circuit condition is detected both V_{POS} and V_{NEG} are disabled and the device shuts down. Normal operation is resumed by pulling EN low and then high again, or by cycling the input supply voltage.

8.3.3 Startup and Shutdown Sequencing

Figure 8 illustrates the startup and shutdown sequencing of the TPS65133 device.

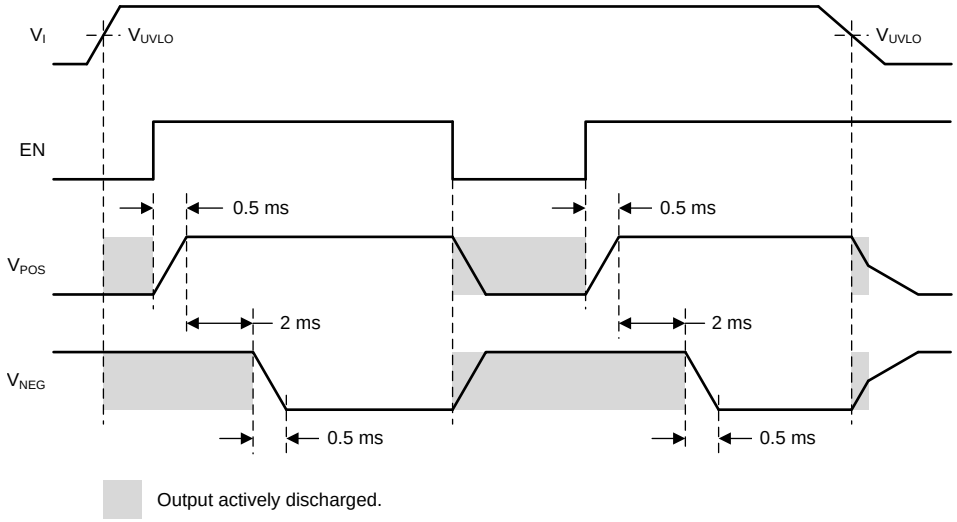


Figure 8. Startup and Shutdown Sequencing

8.3.4 Thermal Shutdown

The TPS65133 device features a thermal shutdown function to prevent damage because of excessive temperature. Once a junction temperature of 135°C (typical) is exceeded the device goes into shuts down. Normal operation is resumed (assuming that the device junction temperature has fallen below the thermal shut-down threshold) by pulling EN low and then high again, or by cycling the input supply voltage.

8.4 Device Functional Modes

8.4.1 Operation with V_I < 2.9 V

The recommended minimum input supply voltage is 2.9 V. The device continues to operate with input supply voltages below 2.9 V, however, full performance is not guaranteed. The device does not operate with input supply voltages below the UVLO threshold.

8.4.2 Operation with $V_I \approx V_{POS}$ (Diode Mode)

The TPS65133 device features a "diode" mode that enables it to regulate its positive output even when the input supply voltage is close to 5.0 V (i.e. too high for normal boost operation). When operating in diode mode the converter's synchronous rectifier stops switching and instead its body diode is used to rectify the output current. Boost converter efficiency is reduced in diode mode. At low output currents (≈2 mA and below), the boost converter automatically transitions from pulse-width modulation to pulse-skip operation. This ensures that the boost converter's output stays in regulation, but increases the voltage ripple on V_{POS}.

8.4.3 Operation with EN

When EN=LOW the TPS65133 device is disabled and switching is inhibited. When the input supply voltage is above the undervoltage lockout threshold and EN=HIGH the device is enabled and its start-up sequence begins.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65133 device can be used to generate ±5-V supply rails from input supply voltages in the range 2.9 V to 5 V, and has been optimized for use with regulated 3.3-V rails and single-cell Li-Ion batteries. Its output voltages are fixed at ±5 V and cannot be changed by the user. Both output voltages are controlled by the EN pin: a high logic level on the EN pin enables both outputs, and a low logic level disables them. Note that when the input supply voltage is above the UVLO threshold and the EN pin is low, both outputs are disabled and *actively discharged* to ground. When the input supply voltage is below the UVLO threshold, both outputs are disabled, but they are *not* actively discharged.

9.2 Typical Application

Figure 9 shows a typical application schematic suitable for supplying up to 250 mA at ±5 V from e.g. a single-cell Li-Ion battery.

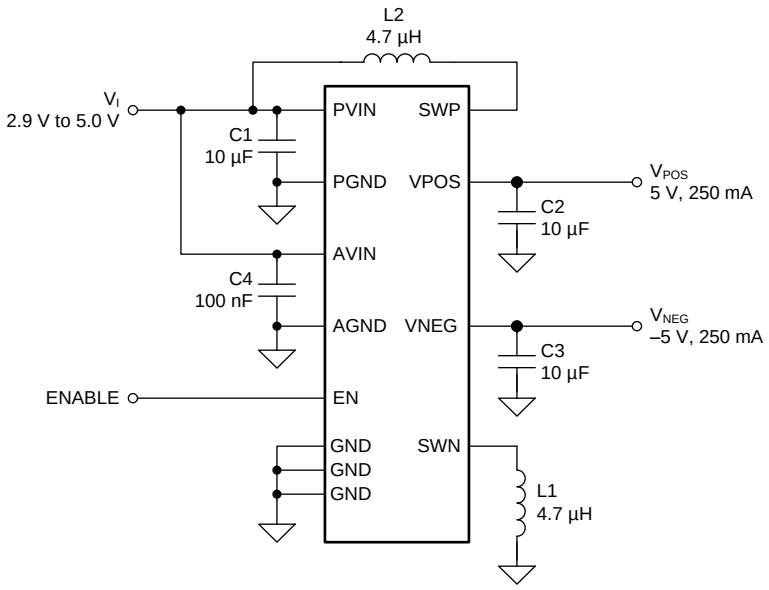


Figure 9. Typical Application Circuit

9.2.1 Design Requirements

The design parameters for the application circuit in Figure 9 are listed in Table 1.

Table 1. Design Parameters

PARAMETERS	EXAMPLE VALUES
Input voltage range	2.9 V to 5.0 V
Output voltage	±5.0 V
Switching frequency	1.7 MHz

9.2.2 Detailed Design Procedure

In order to maximize performance, the TPS65133 device has been optimized for use with a relatively narrow range of external components, and customers are recommended to use the application circuit shown in Figure 9 and the components listed in Table 2 and Table 3.

9.2.2.1 Inductor Selection

The two dc-dc converters in the TPS65133 device have been optimized for use with 4.7 µH inductors, and it is recommended to use this value in all applications. Customers using different values of inductors should characterize performance thoroughly before going to mass production.

Table 2. Inductor Selection

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
L1, L2	4.7 µH	Coilmaster	MMPP252012-4R7N
		Toko	1239AS-H-4R7M
		ABCO	LPP252012-4R7N
		Coilcraft	XFL4020-4R7ML

9.2.2.2 Capacitor Selection

The recommended capacitor values are shown in Table 3. Applications using less than the recommended capacitance (e.g. to save PCB area) may experience increased voltage ripple. In general, the lower the output power required by the application, the lower the capacitance needed for proper performance. C4 improves immunity to noise on the input supply voltage, but it is not necessary in many applications.

Table 3. Capacitor Selection

PARAMETER	VALUE	MANUFACTURER	PART NUMBER
C1, C2, C3	10 µF	Murata	GRM21BR71A106KE51
C4	100 nF		GRM21BR71E104KA01

9.2.3 Application Performance Graphs

The performance shown in the following graphs was obtained using the circuit shown in Figure 9 and the external components listed in Table 2 and Table 3. (1)

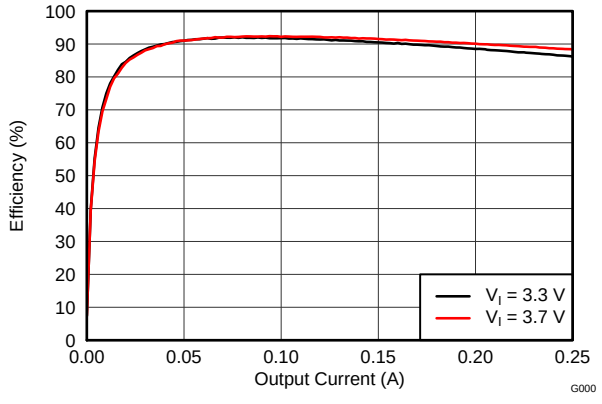


Figure 10. Efficiency vs Output Current

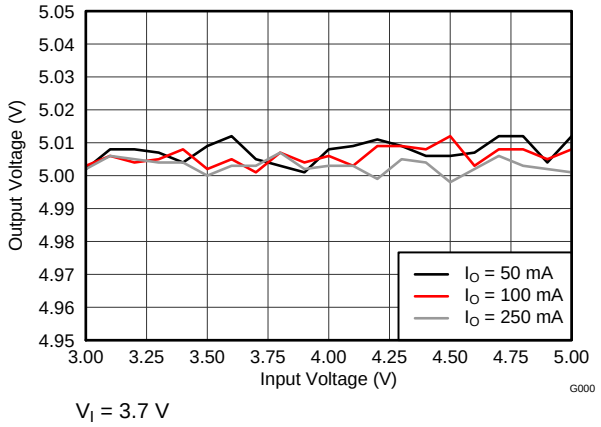
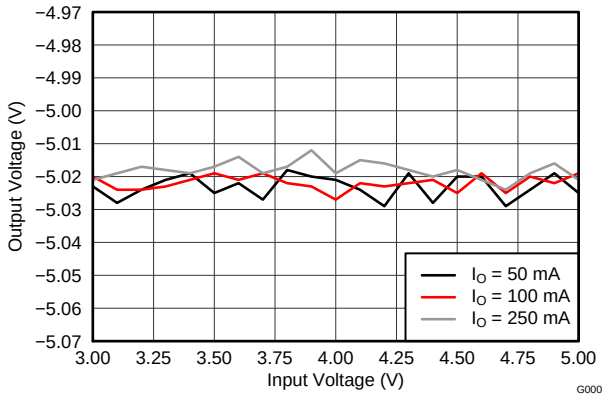


Figure 11. V_{POS} Line Regulation

(1) The Toko inductor was used to obtain the application graphs.



V_I = 3.7 V

Figure 12. V_{NEG} Line Regulation

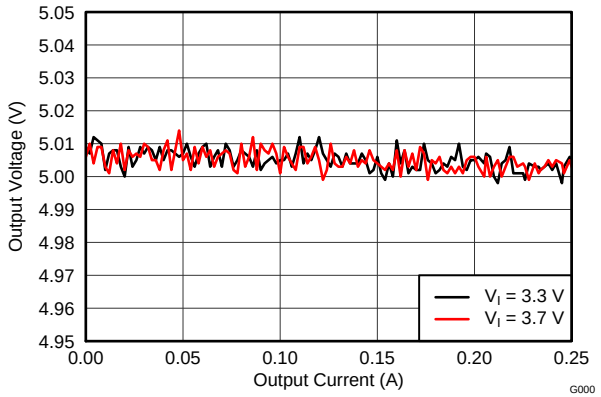


Figure 13. V_{POS} Load Regulation

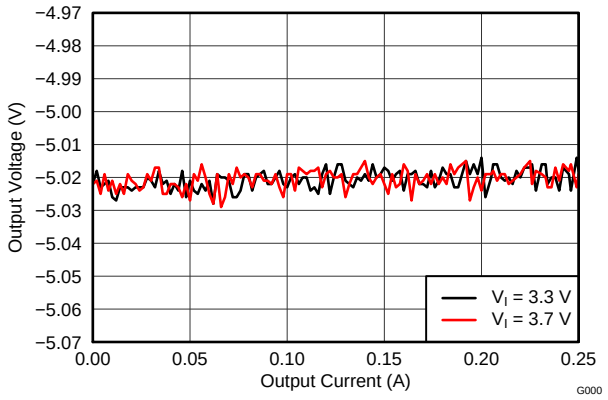
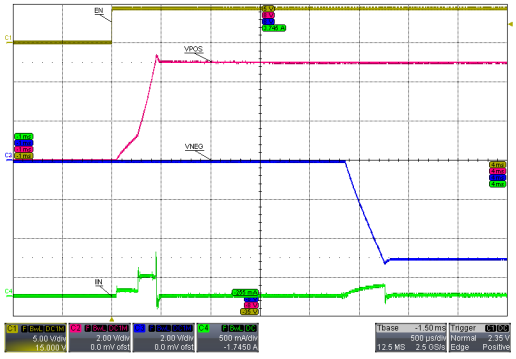
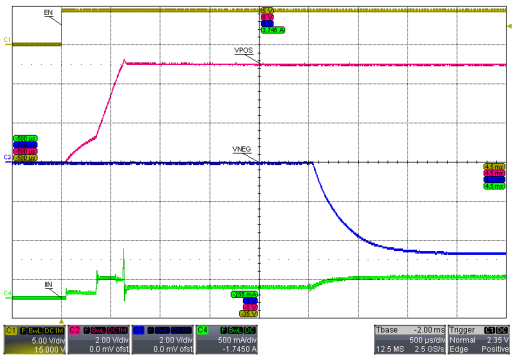


Figure 14. V_{NEG} Load Regulation



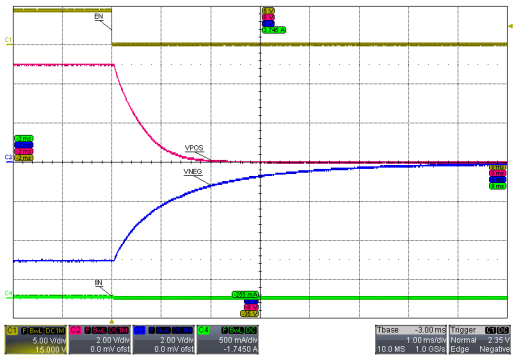
V_I = 3.7 V, I_{POS} = I_{NEG} = 0 mA

Figure 15. V_{POS} and V_{NEG} Startup Behavior (0 mA)



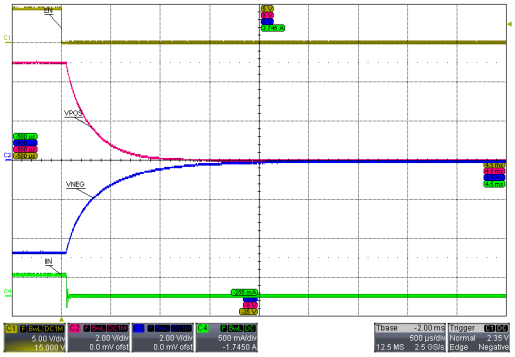
V_I = 3.7 V, I_{POS} = I_{NEG} = 100 mA

Figure 16. V_{POS} and V_{NEG} Startup Behavior (100 mA)



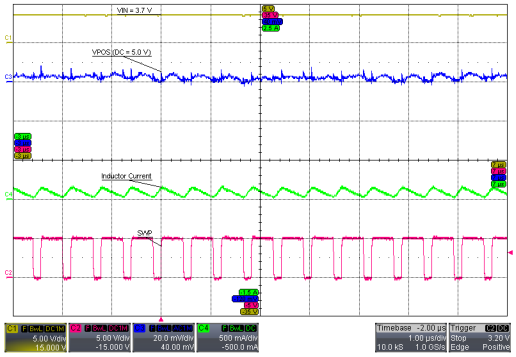
V_I = 3.7 V, I_{POS} = I_{NEG} = 0 mA

Figure 17. V_{POS} and V_{NEG} Shutdown Behavior (0 mA)



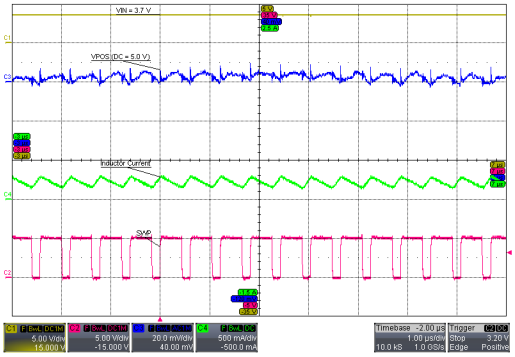
V_I = 3.7 V, I_{POS} = I_{NEG} = 100 mA

Figure 18. V_{POS} and V_{NEG} Shutdown Behavior (100 mA)



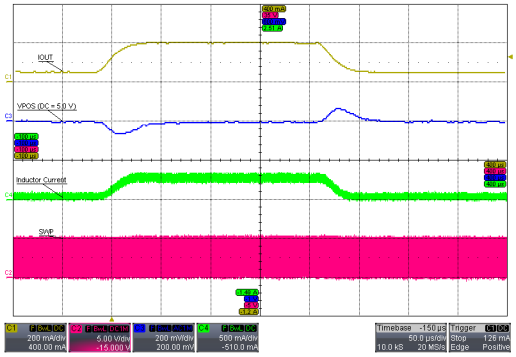
V_I = 3.7 V, I_{POS} = 10 mA

Figure 19. V_{POS} Switching Waveforms (10 mA)



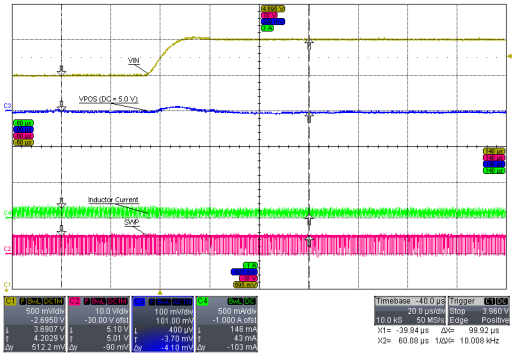
V_I = 3.7 V, I_{POS} = 100 mA

Figure 20. V_{POS} Switching Waveforms (100 mA)



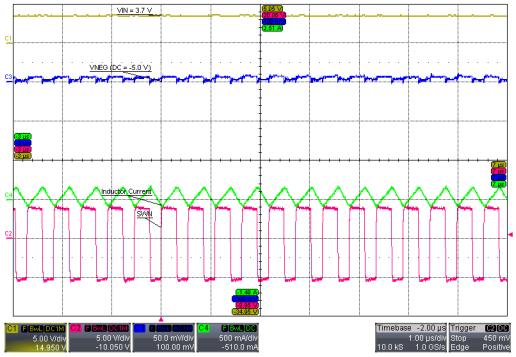
V_I = 3.7 V, I_{POS} = 50 mA to 200 mA

Figure 21. V_{POS} Load Transient



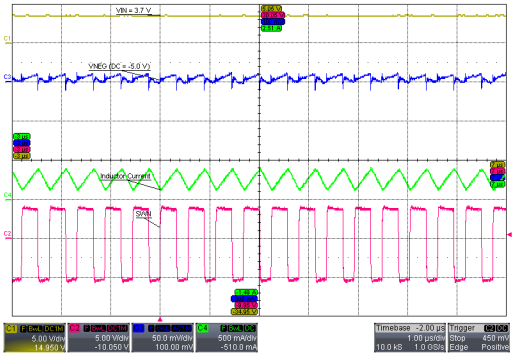
V_I = 3.7 V to 4.2 V, I_{POS} = 50 mA

Figure 22. V_{POS} Line Transient



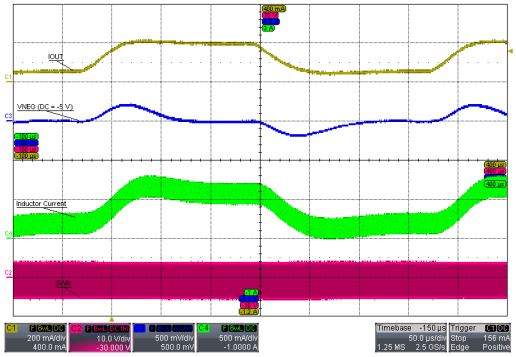
V_I = 3.7 V, I_{NEG} = 10 mA

Figure 23. V_{NEG} Switching Waveforms (10 mA)



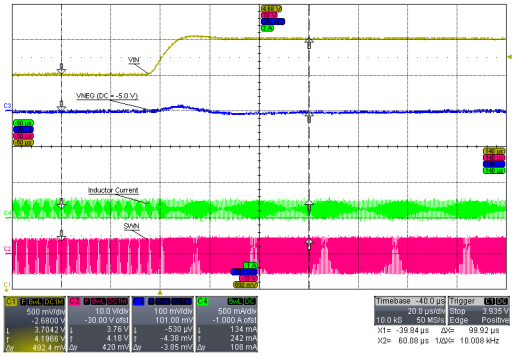
V_I = 3.7 V, I_{NEG} = 100 mA

Figure 24. V_{NEG} Switching Waveforms (100 mA)



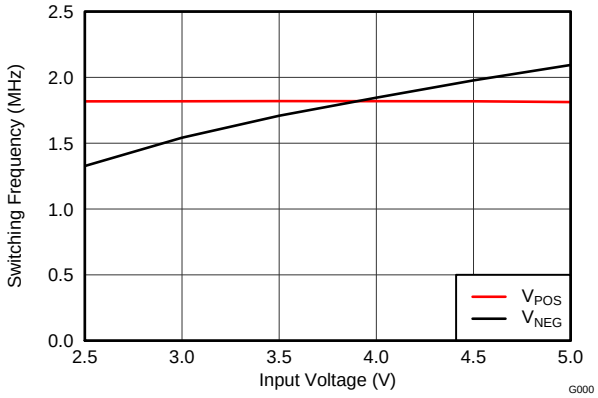
V_I = 3.7 V, I_{NEG} = 50 mA to 200 mA

Figure 25. V_{NEG} Load Transient



V_I = 3.7 V to 4.2 V, I_{NEG} = 50 mA

Figure 26. V_{NEG} Line Transient



I_{POS} = I_{NEG} = 100 mA

Figure 27. Switching Frequency

10 Power Supply Recommendations

The TPS65133 device is designed to operate from an input supply voltage in the range 2.9 V to 5.0 V. If the input supply is located more than a few centimeters from the device additional bulk capacitance may be required. The 10-µF shown in the schematics in this data sheet are typical for this function.

11 Layout

11.1 Layout Guidelines

No PCB layout is perfect, and compromises are always necessary. However, the basic principles listed below (in order of importance) go a long way to achieving the full performance of the TPS65133 device.

- Route discontinuous switching currents on the top layer using short, wide traces. Avoid routing these signals through vias, which have relatively high parasitic inductance and resistance.
- Place C1 as close as possible to pin 12.
- Place C2 as close as possible to pin 3. Place C3 as close as possible to pin 9.
- Use the exposed thermal pad to connect GND, AGND and PGND.
- Use a copper pour (preferably on layer 2) as a thermal spreader and connect it to the exposed thermal pad using a number of thermal vias.

Figure 28 illustrates how a PCB layout following the above principles may be realized in practice.

11.2 Layout Example

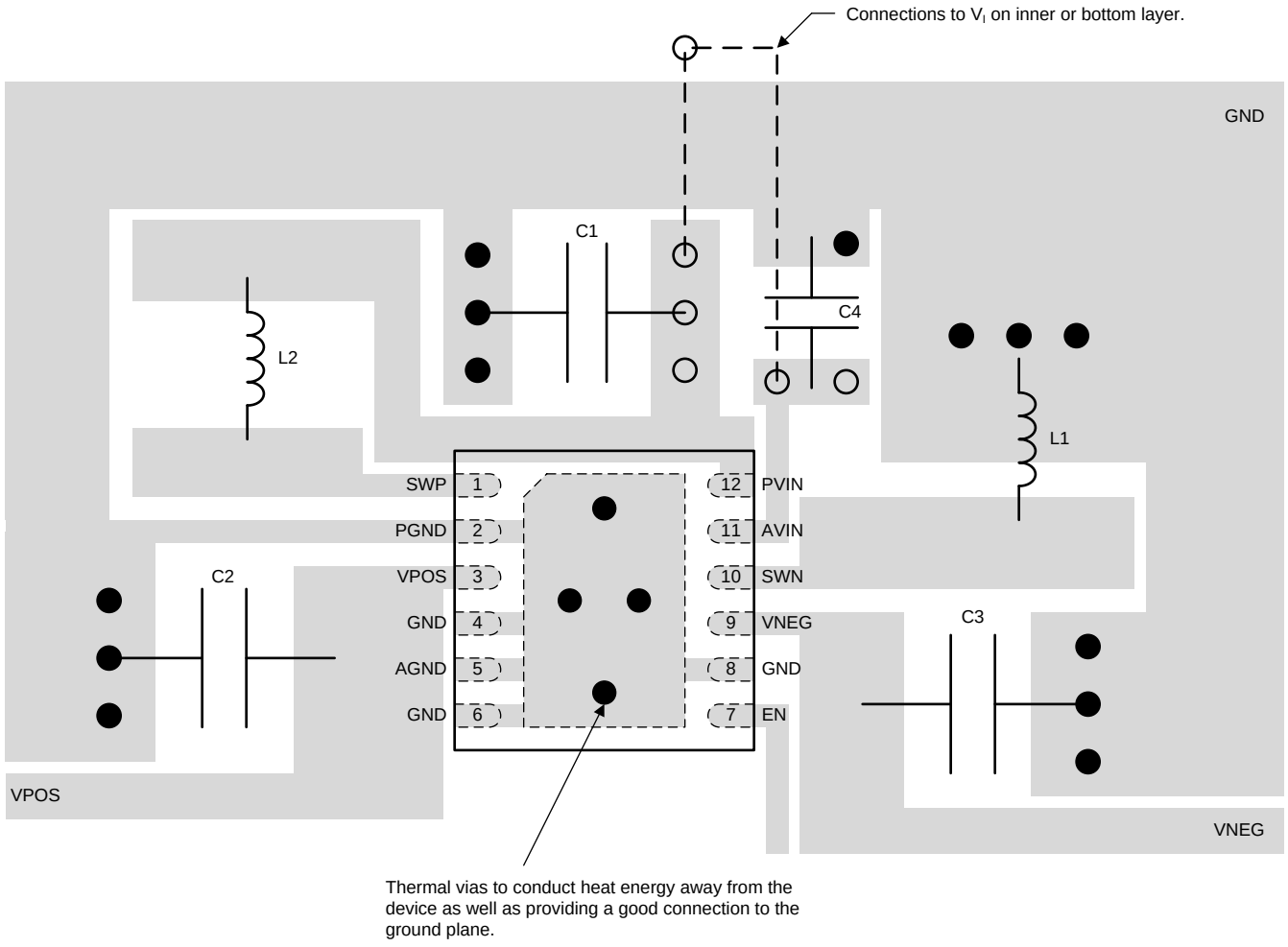


Figure 28. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided *AS IS* by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

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All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

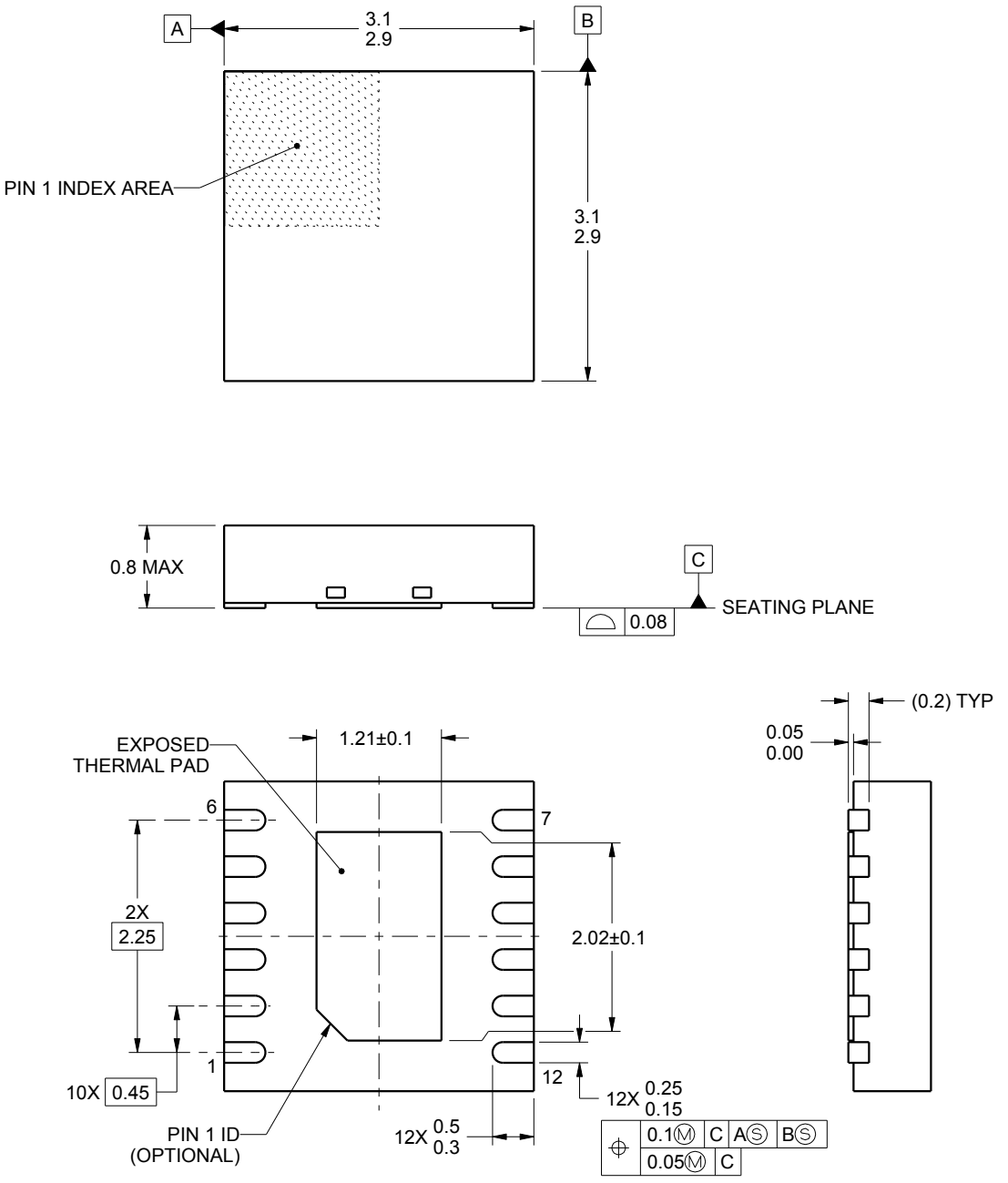
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DPD0012A

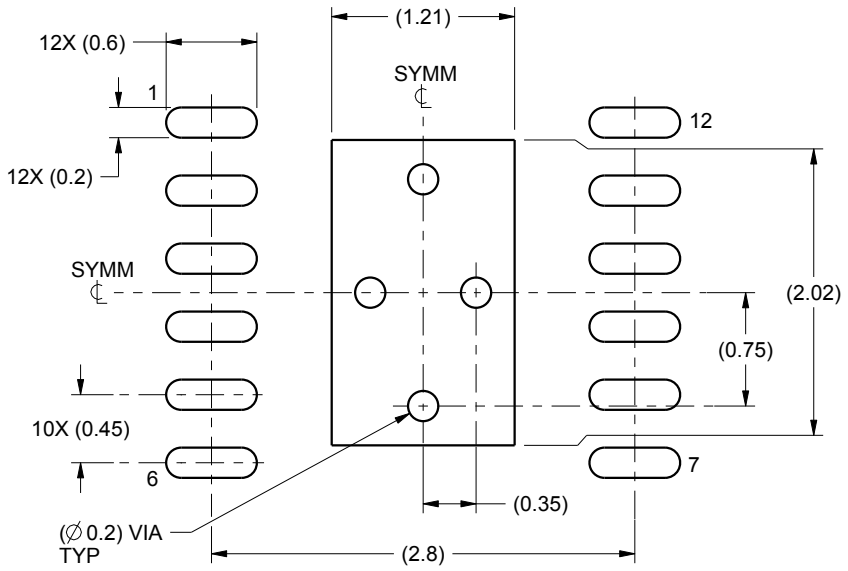
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

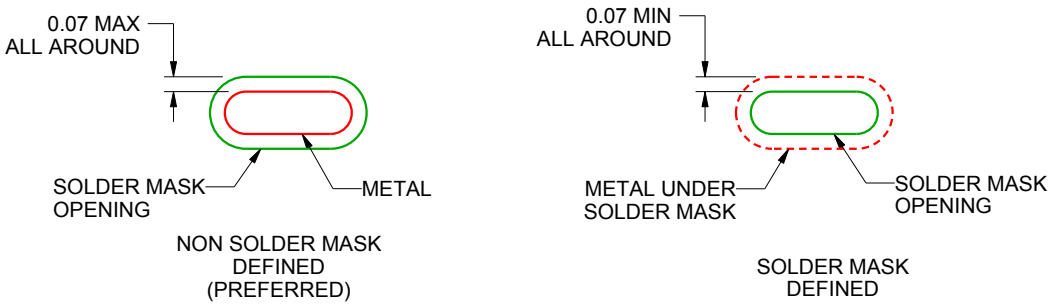


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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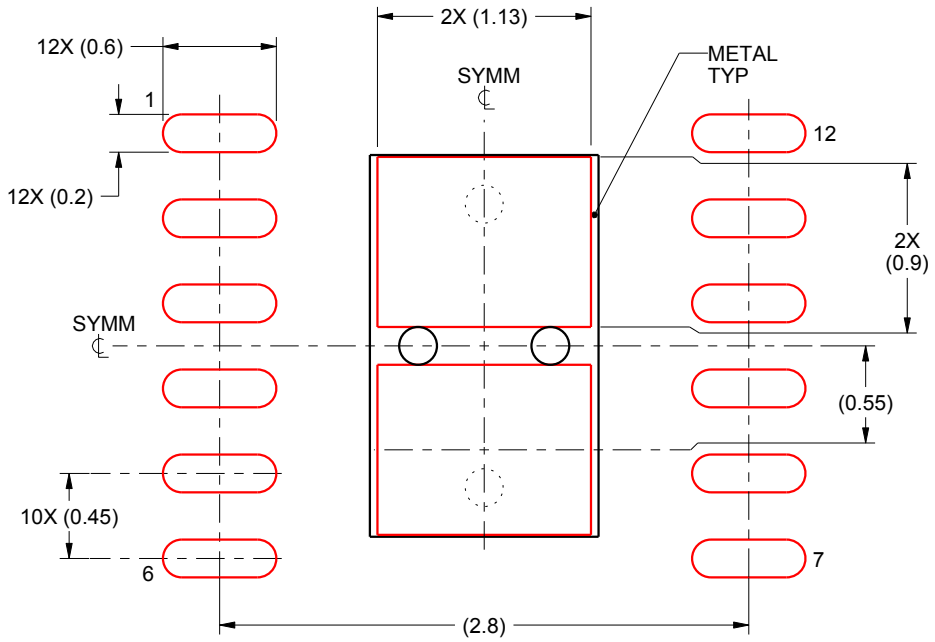
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65133DPDR	ACTIVE	WSON	DPD	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SHY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

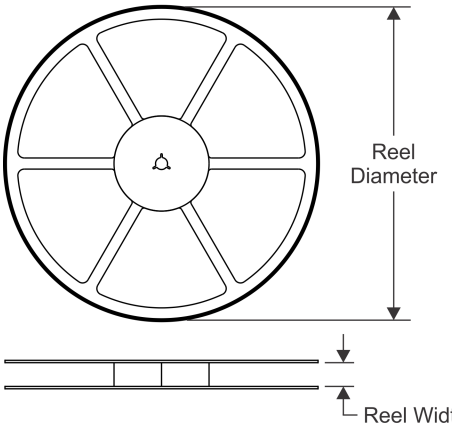
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

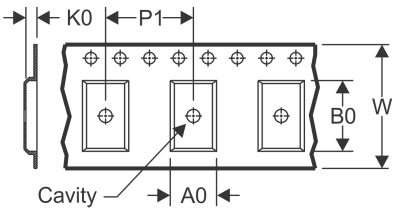
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

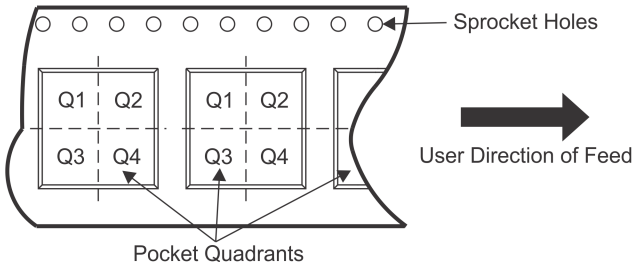


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

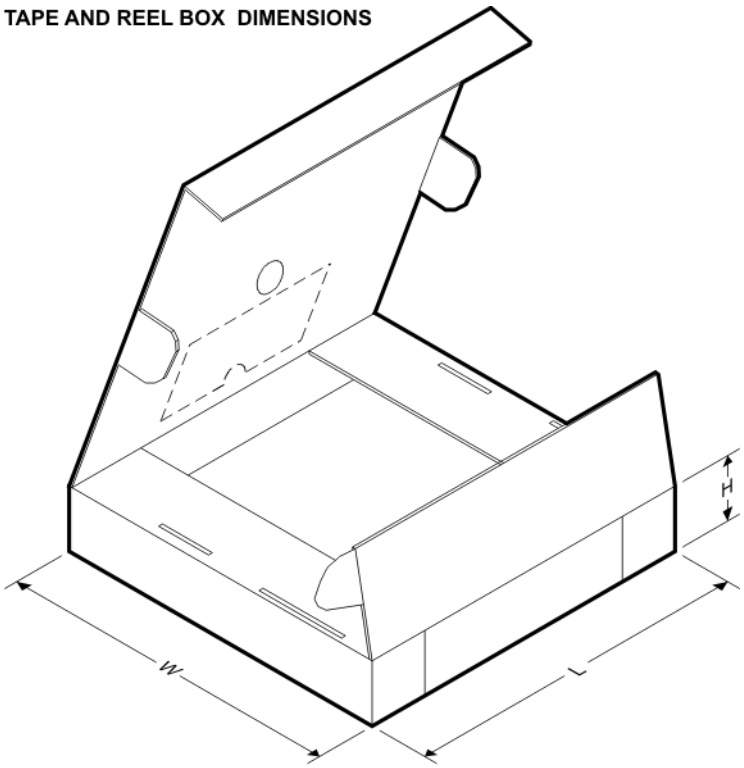
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65133DPDR	WSON	DPD	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

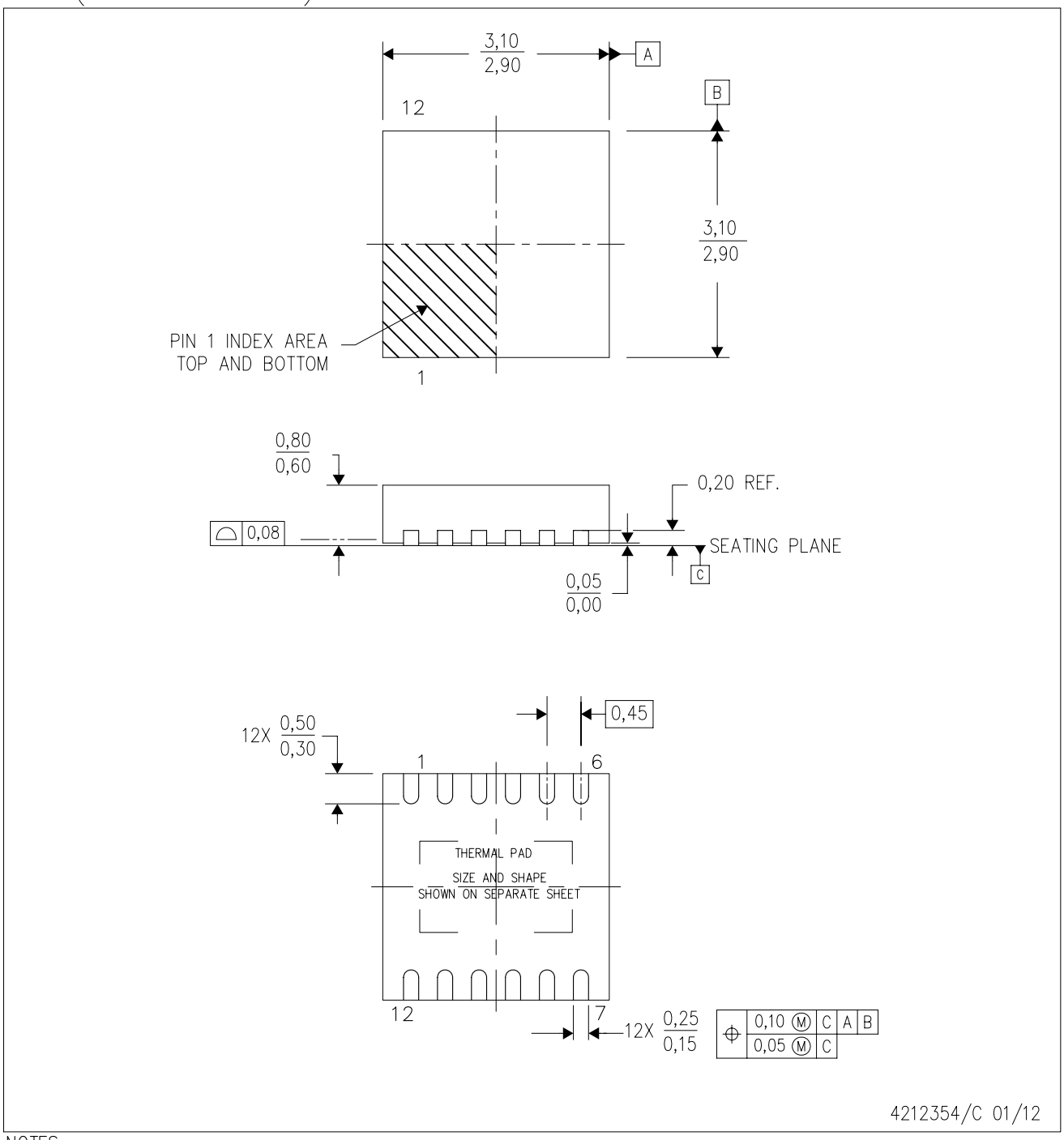
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65133DPDR	WSON	DPD	12	3000	367.0	367.0	35.0

DPD (S–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

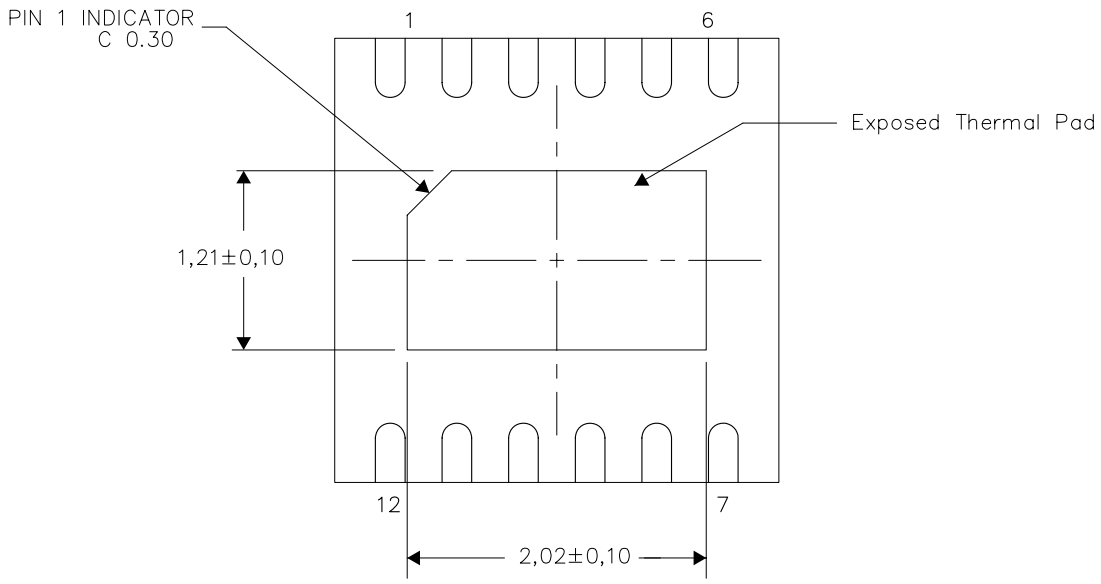
DPD (S–PUSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4212468/A 02/12

NOTE: All linear dimensions are in millimeters

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