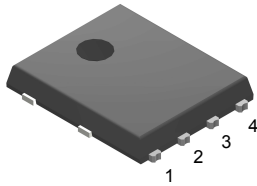
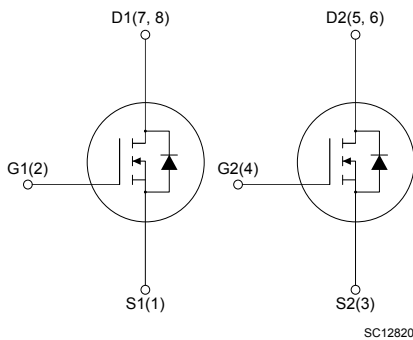


## Automotive-grade dual N-channel 60 V, 21 mΩ typ., 32 A STripFET F6 Power MOSFET in a PowerFLAT 5x6 DI package




**PowerFLAT 5x6  
double island**



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STL8DN6LF6AG	60 V	27 mΩ	32 A	55 W

- AEC-Q101 qualified 
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

### Applications

- Switching applications

### Description

This device is a dual N-channel Power MOSFET developed using the STripFET F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.



#### Product status link

[STL8DN6LF6AG](#)

#### Product summary

<b>Order code</b>	STL8DN6LF6AG
<b>Marking</b>	8DN6LF6
<b>Package</b>	PowerFLAT 5x6 double island
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	32	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	23	
$I_D^{(1)}$	Drain current (continuous) at $T_B = 25\text{ }^\circ\text{C}$	9.6	A
	Drain current (continuous) at $T_B = 100\text{ }^\circ\text{C}$	6.8	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	38	A
$I_{DM}^{(2)}$	Drain current (pulsed)	128	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (one channel active)	55	W
	Total power dissipation at $T_B = 25\text{ }^\circ\text{C}$ (one channel active)	4.8	
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .
2. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	2.7	$^\circ\text{C}/\text{W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	31.3	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, not repetitive	32	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = 38\text{ A}$ , $V_{DD} = 43.5\text{ V}$ )	120	mJ

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified.

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9.6\text{ A}$		21	27	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 9.6\text{ A}$		25	31	

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1340	-	pF
$C_{oss}$	Output capacitance		-	90	-	pF
$C_{rss}$	Reverse transfer capacitance		-	60	-	pF
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}$ , $I_D = 9.6\text{ A}$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	27	-	nC
$Q_{gs}$	Gate-source charge		-	4.6	-	nC
$Q_{gd}$	Gate-drain charge		-	4.3	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 12.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	9.6	-	ns
$t_r$	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	56	-	ns
$t_f$	Fall time		-	7	-	ns

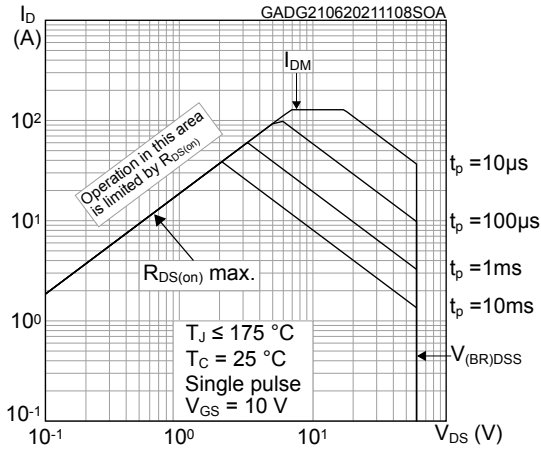
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9.6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		38	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 9.6\text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	22.5		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 48\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	22.2		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	2.0		A

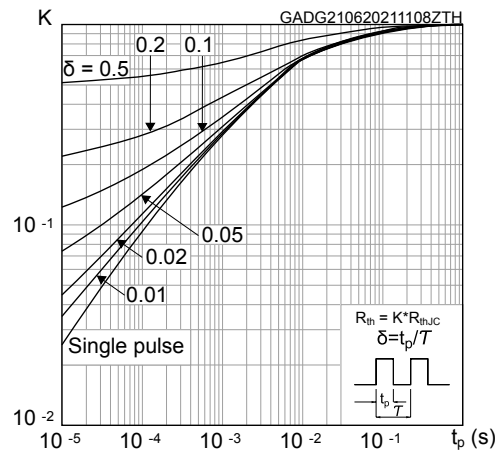
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

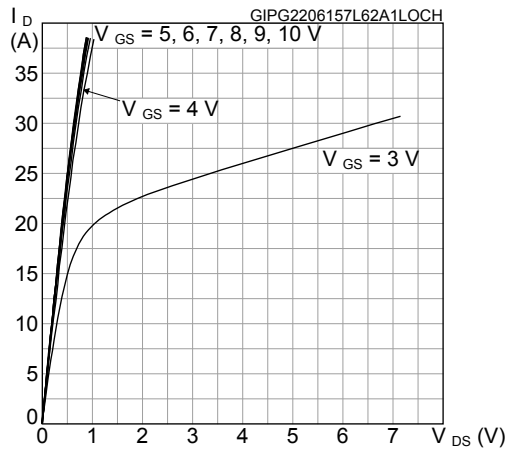
**Figure 1. Safe operating area**



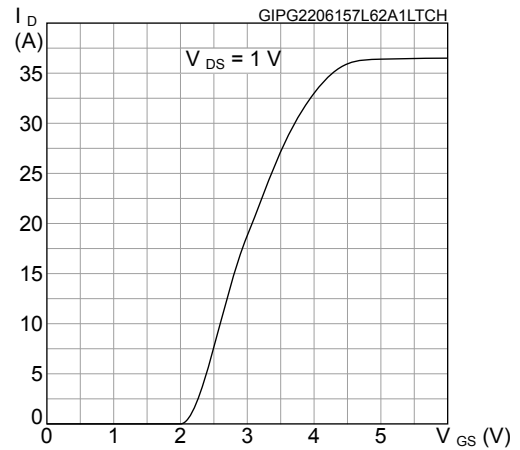
**Figure 2. Thermal impedance**



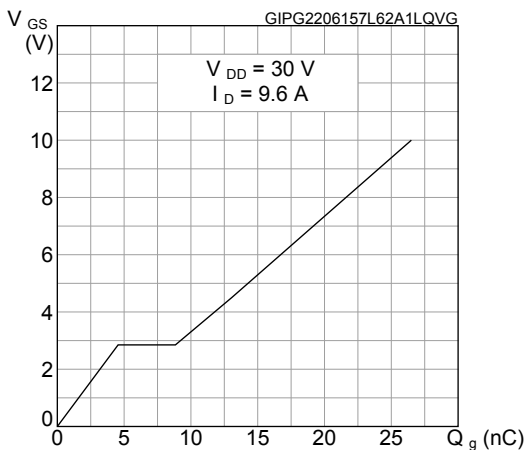
**Figure 3. Output characteristics**



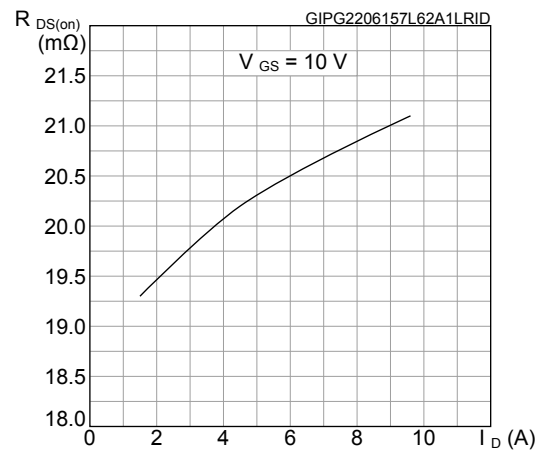
**Figure 4. Transfer characteristics**



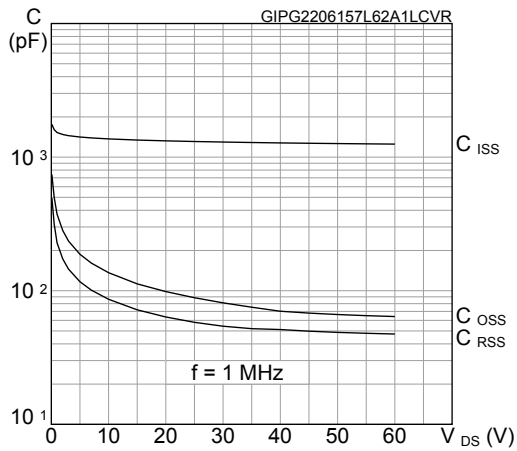
**Figure 5. Gate charge vs gate-source voltage**



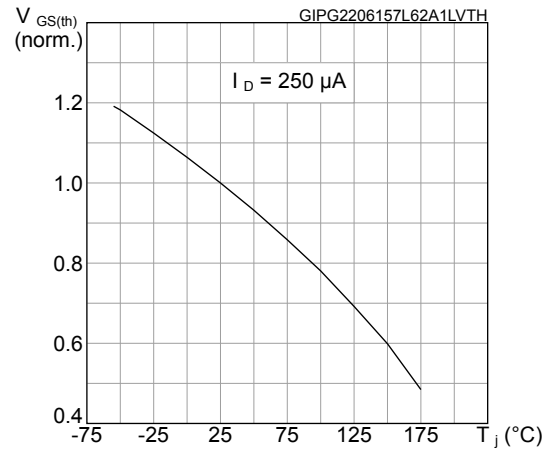
**Figure 6. Static drain-source on-resistance**



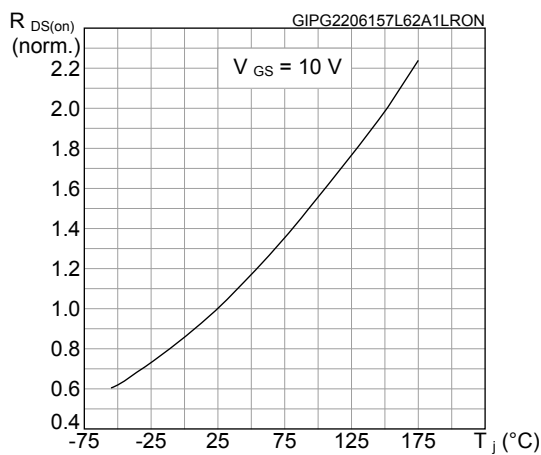
**Figure 7. Capacitance variations**



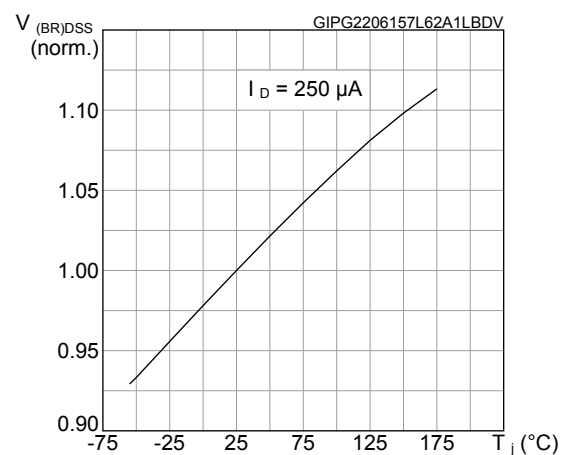
**Figure 8. Normalized gate threshold voltage vs temperature**



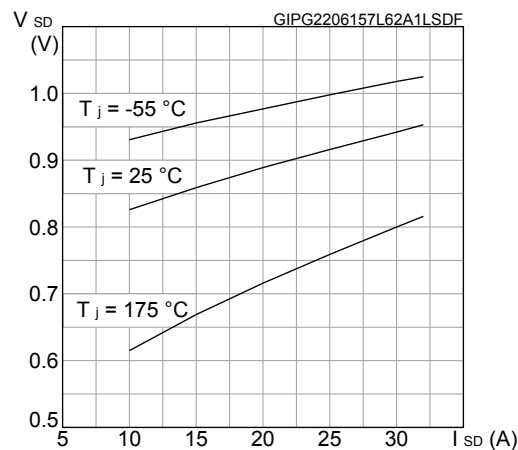
**Figure 9. Normalized on-resistance vs temperature**



**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**

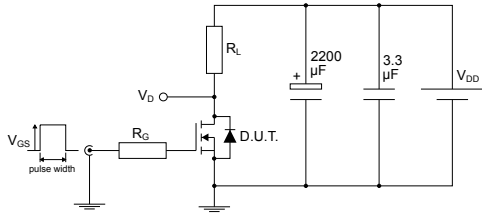


**Figure 11. Source-drain diode forward characteristics**



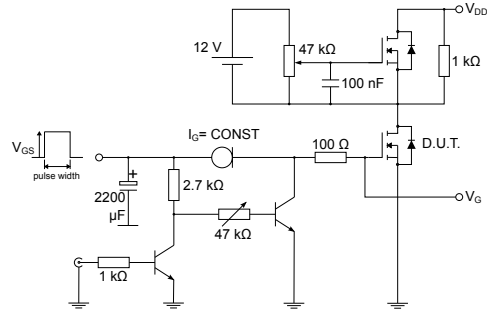
### 3 Test circuits

Figure 12. Test circuit for resistive load switching times



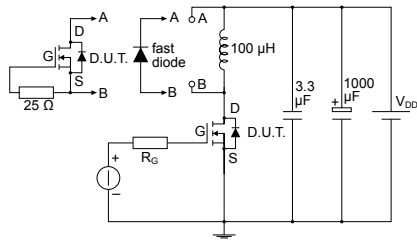
AM01468v1

Figure 13. Test circuit for gate charge behavior



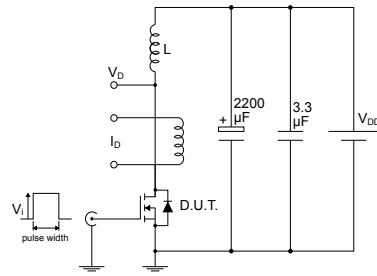
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times



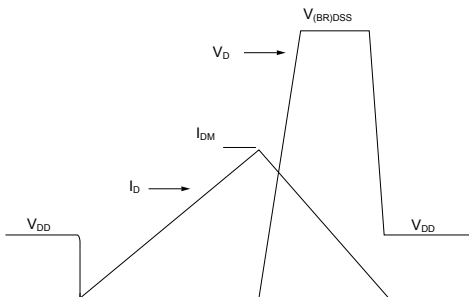
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Figure 15. Unclamped inductive load test circuit



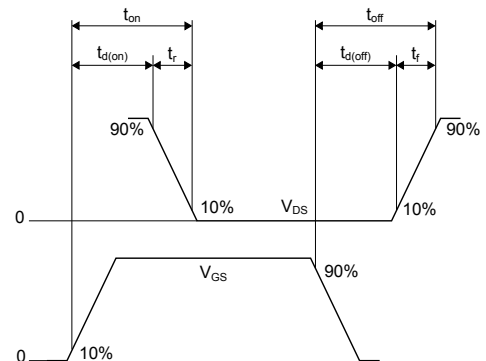
AM01471v1

Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



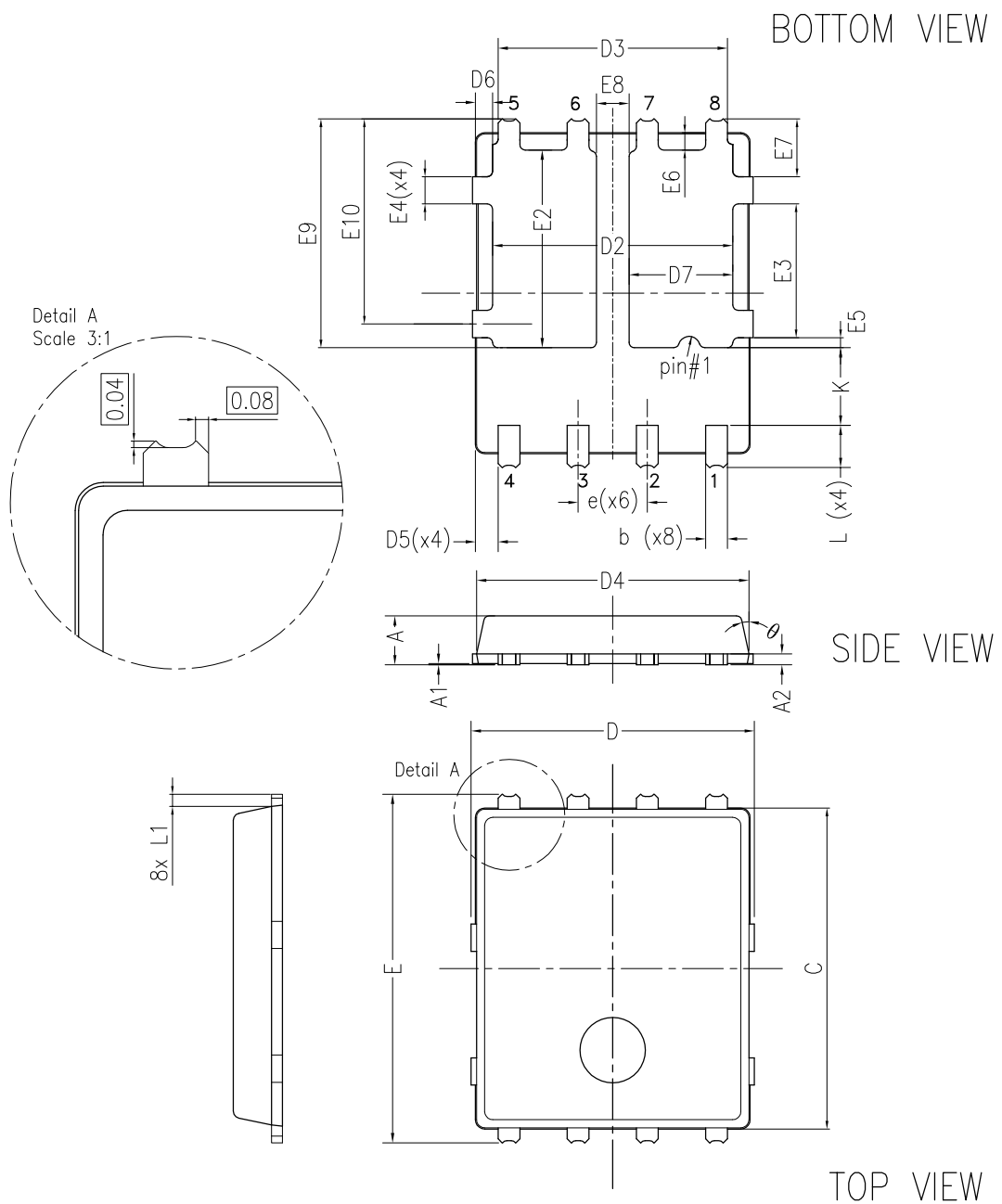
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 5x6 double island WF type R package information

**Figure 18. PowerFLAT 5x6 double island WF type R package outline**



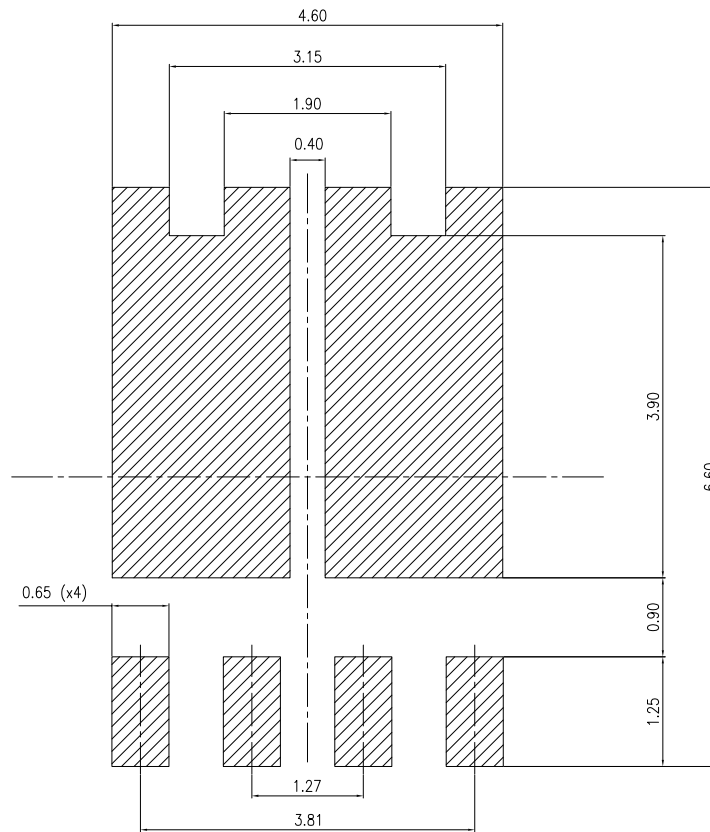
8256945\_typeR-WF\_R18



**Table 8. PowerFLAT 5x6 double island WF type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

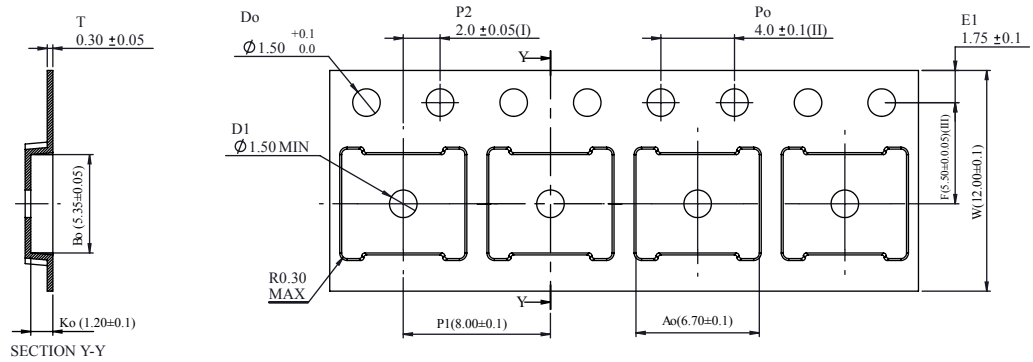
Figure 19. PowerFLAT 5x6 double island recommended footprint (dimensions are in mm)



8256945\_DI\_FP\_smp\_R18

## 4.2 PowerFLAT 5x6 WF packing information

**Figure 20. PowerFLAT 5x6 WF tape (dimensions are in mm)**

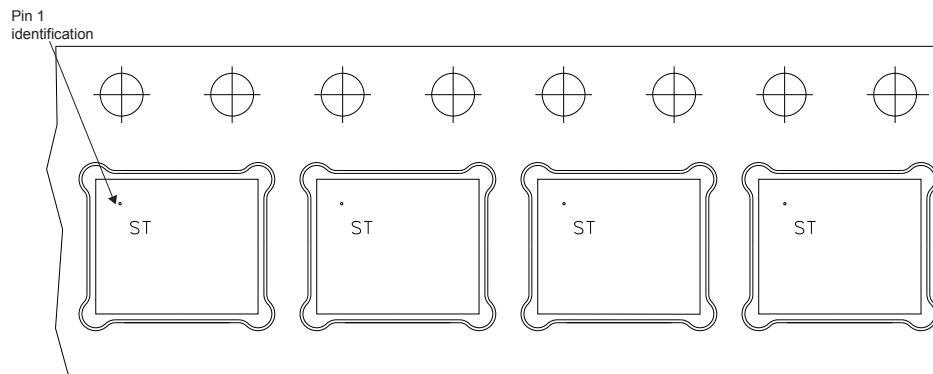


- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
- (III) Measured from centreline of sprocket hole to centreline of pocket.

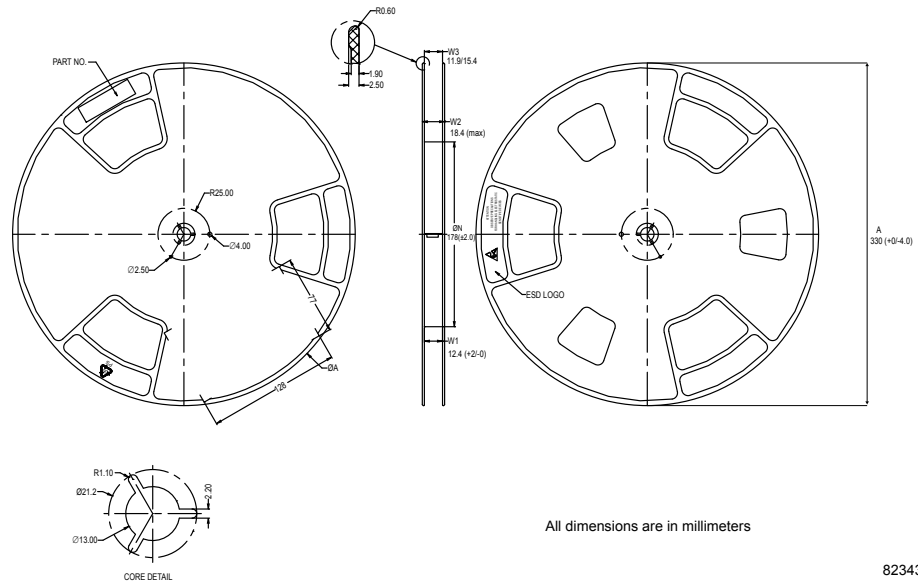
Base and bulk quantity 3000 pcs

8234350\_TapeWF\_rev\_C

**Figure 21. PowerFLAT 5x6 package orientation in carrier tape**



**Figure 22. PowerFLAT 5x6 reel (dimensions are in mm)**



## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Jun-2015	1	First release.
07-Jul-2015	2	Minor text edits throughout document.
19-Jan-2016	3	Updated title. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> and <i>Table 4: "Avalanche characteristics"</i> . Updated <i>Figure 2: "Safe operating area"</i> and <i>Figure 3: "Thermal impedance"</i> . Minor text changes.
21-Sep-2016	4	Updated <i>Table 2: "Absolute maximum ratings"</i> . Updated <i>Section 4.1: "PowerFLAT™ 5x6 double island WF type R package information"</i> . Minor text changes.
01-Jul-2021	5	Updated <a href="#">Internal schematic for dual N-channel</a> in cover page. Updated <i>Figure 1. Safe operating area</i> and <i>Figure 2. Thermal impedance</i> . Minor text changes.

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