Process Change Notification

PCN Number: PCN-2020-140 **PCN Notification Date:** 11/11/2020

Informational PCN

Data Sheet Update:
CS43L36 ver. F5 to F6

Dear Customer,

This notification is to advise you of the following change.

With immediate effect, the data sheet for CS43L36 is updated to reflect the following changes:

- Correcting a typing error for the default value of the “Reserved” and “SRC_SDIN_FS” register fields shown in the Power-up Sequence section. These corrected values will be consistent with what is defined in the Register Description section for the SRC Input Sample Rate register.
- Updating the QFN thermal characteristics which have been recalculated with an improved thermal simulation model. The model has been accepted in this industry and Cirrus have synchronized and aligned methodology for the calculation. This provide better guidance for customers’ system thermal design.

If you have any questions, please contact your Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

Process Change Notification

PCN Number: PCN-2020-140 **PCN Notification Date:** 11/11/2020

Products Affected:

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	Data Sheet Update: CS43L36						
Customer Contact:	Local Field Sales Representative		**Phone:** (512) 851-4000		**Dept:**	Corporate Quality	
Proposed 1st Ship Date:		NA	**Estimated Sample Availability Date:**			NA	
Change Type:							
	Assembly Site		Assembly Process		Assembly Materials		
	Wafer Fab Site		Wafer Fab Process		Wafer Fab Materials		
	Wafer Bump Site		Wafer Bump Process		Wafer Bump Material		
	Test Site		Test Process		Design		
X	Electrical Specification		Mechanical Specification		Part Number		
	Packing/Shipping/Labeling	X	Other				
Comments:	Data Sheet Update						

PCN Details

Description of Change:

The data sheet for CS43L36 has been updated to reflect the following changes:

- Corrected the Reserved and SRC_SDIN_FS register field value in Step 4.12 of Ex. 5-1.
- Updated the QFN thermal characteristics in Table 11-1, Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics.

Data Sheet Reference:

CS43L36: https://www.cirrus.com/products/cs43l36/

5.1 Power-Up Sequence - Page 49

Version F5 (Before change)

Example 5-1. Power-Up Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
4.12	Configure the SRC sample rate detection.	SRC Input Sample Rate. 0x2601	0x20	
		Reserved	0010	—
		SRC_SDIN_FS	0000	ASP sample rate is autodetected.

Version F6 (After change)

Example 5-1. Power-Up Sequence

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
4.12	Configure the SRC sample rate detection.	SRC Input Sample Rate. 0x2601	0x40	
		Reserved	010	—
		SRC_SDIN_FS	00000	ASP sample rate is autodetected.

11. Thermal Characteristics - Page 89

Version F5 (Before change)

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter [1]	Symbol	QFN	WLCSP	Unit
Junction-to-ambient thermal resistance	θ_{JA}	35.0	52.0	°C/W
Junction-to-board thermal resistance	θ_{JB}	9.0	17.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.98	0.15	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	8.9	17.7	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.19	0.04	°C/W

1. Thermal setup:
   Still air @ maximum allowed ambient temperature
   JEDEC 2s2p printed wiring board (JEDEC Standard JESD51-11, June 2001)
   Size: 114.5 x 101.5 x 1.6 mm

Version F6 (After change)

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter [1]	Symbol	QFN	WLCSP	Unit
Junction-to-ambient thermal resistance	θ_{JA}	30.1	52.0	°C/W
Junction-to-board thermal resistance	θ_{JB}	3.8	17.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	2.6	0.15	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	3.6	17.7	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.1	0.04	°C/W

1. Thermal setup:
   Still air @ maximum allowed ambient temperature
   JEDEC 2s2p printed wiring board (JEDEC Standard JESD51-11, June 2001)
   Size: 114.5 x 101.5 x 1.6 mm

Process Change Notification

PCN Number: PCN-2020-140 **PCN Notification Date:** 11/11/2020

Reason for Change:

1. Correcting a typing error for the default value of the “Reserved” and “SRC_SDIN_FS” register fields shown in the Power-up Sequence section. These corrected values will be consistent with what is defined in the Register Description section for the SRC Input Sample Rate register.

2. Updating the QFN thermal characteristics which have been recalculated with an improved thermal simulation model. The model has been accepted in this industry and Cirrus have synchronized and aligned methodology for the calculation.

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No impact to form, fit, quality or reliability.

Anticipated Impact on Material Declaration:

☒ No Impact to the Material Declaration

☐ Material Declarations or Product Content reports are driven from production data and will be available following the production release.

Product Affected:

Device	Cirrus Logic Part Number
1	CS43L36-CNZ
2	CS43L36-CNZR

Changes To Product Identification Resulting From This PCN:

No marking changes, this is a data sheet only change and the data sheet will be revised accordingly