



# FQU5N50CTU\_WS

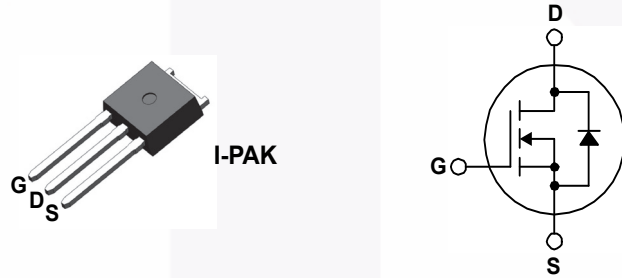
## N-Channel QFET<sup>®</sup> MOSFET 500 V, 4.0 A, 1.4 Ω

### Features

- 4.0 A, 500 V,  $R_{DS(on)} = 1.4 \Omega @ V_{GS} = 10 \text{ V}$
- Low Gate Charge (Typ. 18 nC)
- Low  $C_{rss}$  (Typ. 15 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQU5N50CTU_WS	Units
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	4.0	A
		2.4	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	16	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	300	mJ
$I_{AR}$	Avalanche Current (Note 1)	4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	48	W
		0.38	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQU5N50CTU_WS	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	110	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU5N50CTU_WS	FQU5N50CS	I-PAK	Tube	N/A	N/A	75 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.5	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	--	1.14	1.4	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.0\text{ A}$	--	5.2	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	480	625	pF
$C_{oss}$	Output Capacitance		--	80	105	pF
$C_{rss}$	Reverse Transfer Capacitance		--	15	20	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	--	12	35	ns	
$t_r$	Turn-On Rise Time		--	46	100	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	50	110	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	48	105	ns
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}$	--	18	24	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	2.2	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	9.7	--	nC

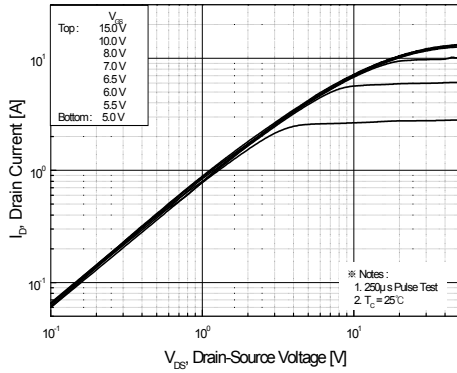
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	4	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 4\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 5\text{ A},$	--	263	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	1.9	--	$\mu\text{C}$

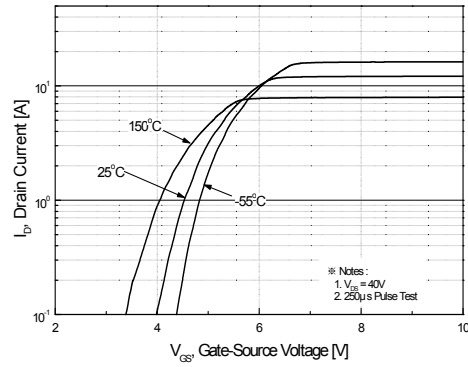
#### Notes:

1. Repetitive rating : pulse width limited by maximum junction temperature.
2.  $L = 21.5\text{ mH}, I_{AS} = 5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

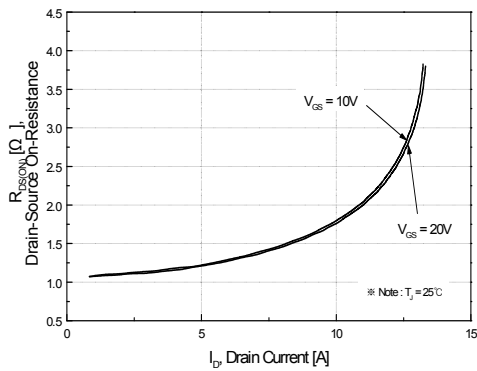
## Typical Characteristics



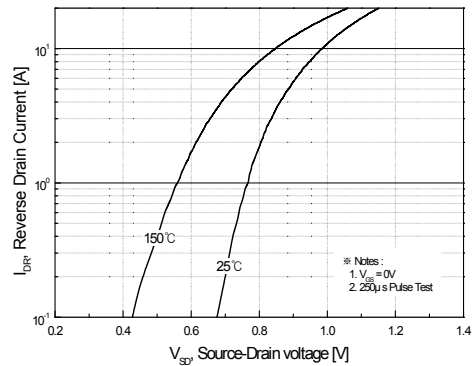
**Figure 1. On-Region Characteristics**



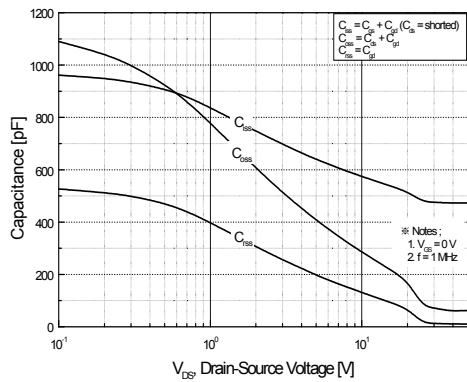
**Figure 2. Transfer Characteristics**



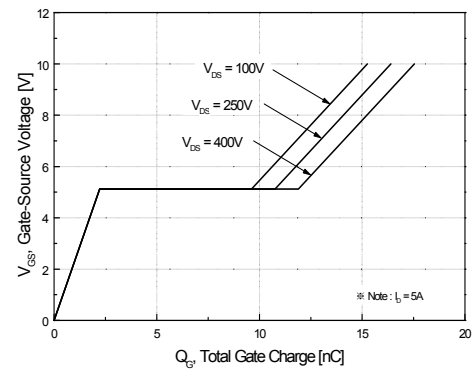
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**

Typical Characteristics (Continued)

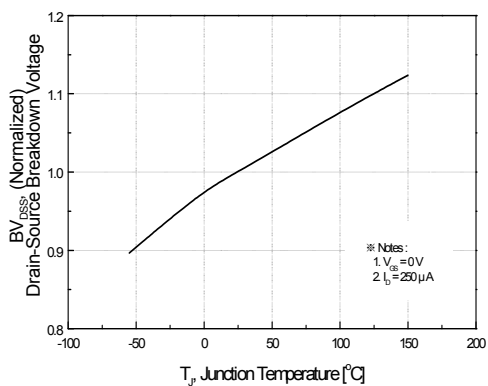


Figure 7. Breakdown Voltage Variation vs Temperature

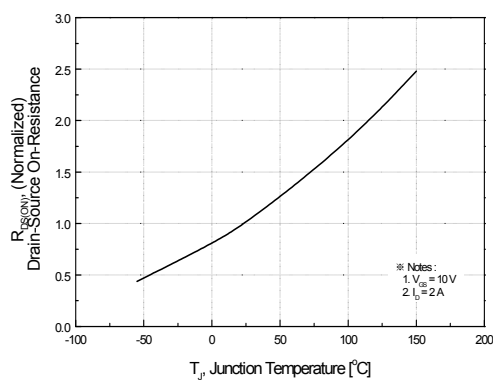


Figure 8. On-Resistance Variation vs Temperature

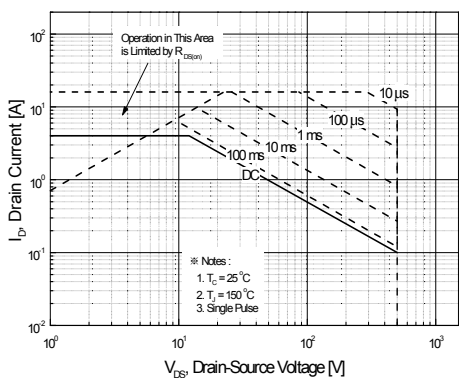


Figure 9. Maximum Safe Operating Area

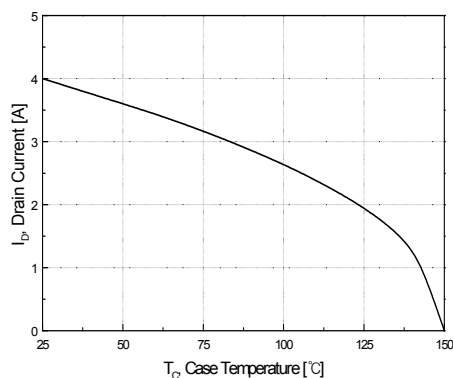


Figure 10. Maximum Drain Current vs Case Temperature

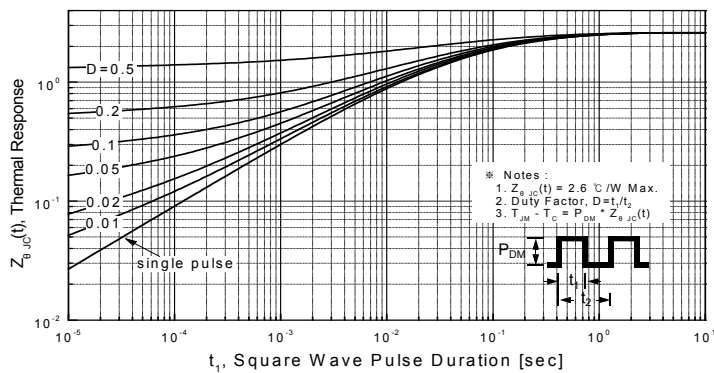
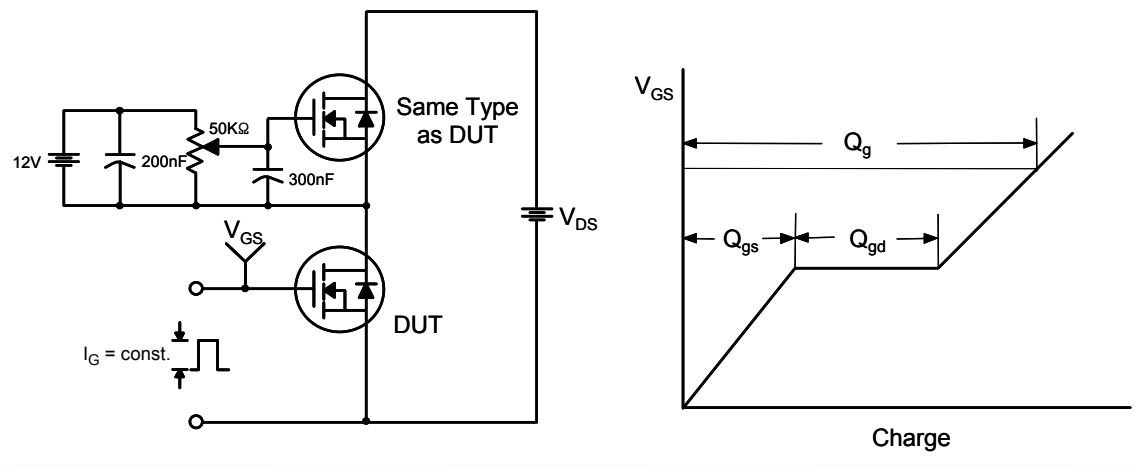
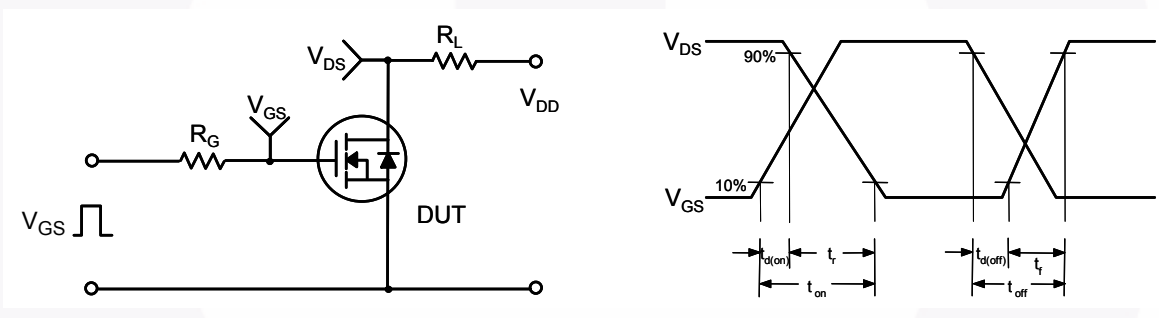


Figure 11. Transient Thermal Response Curve

**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

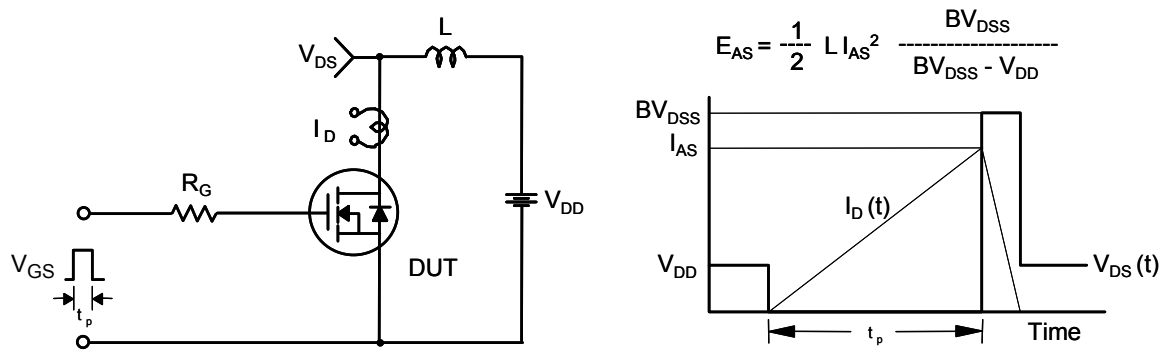
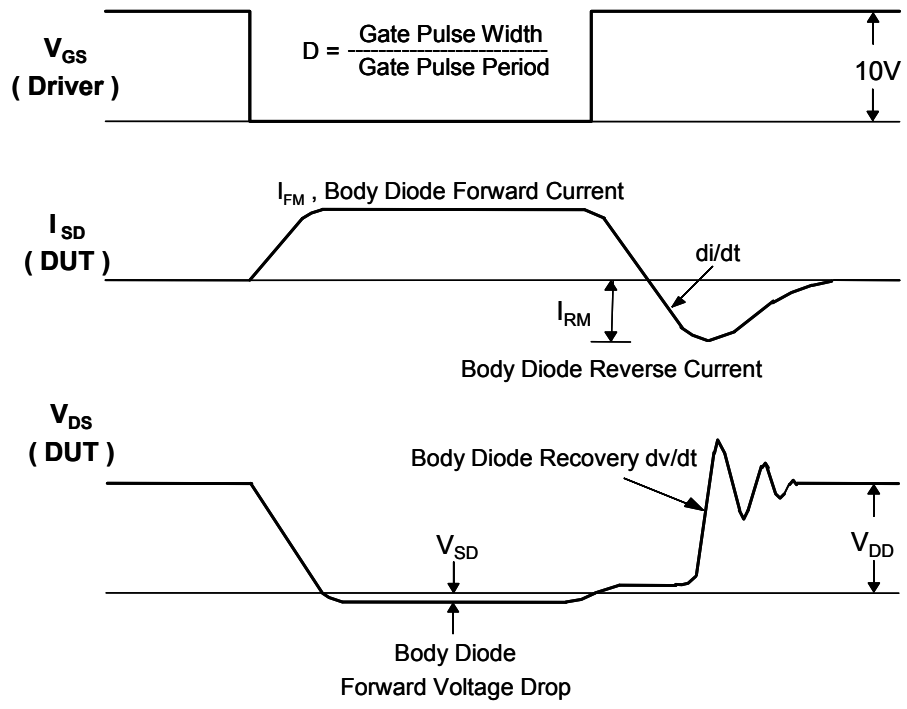
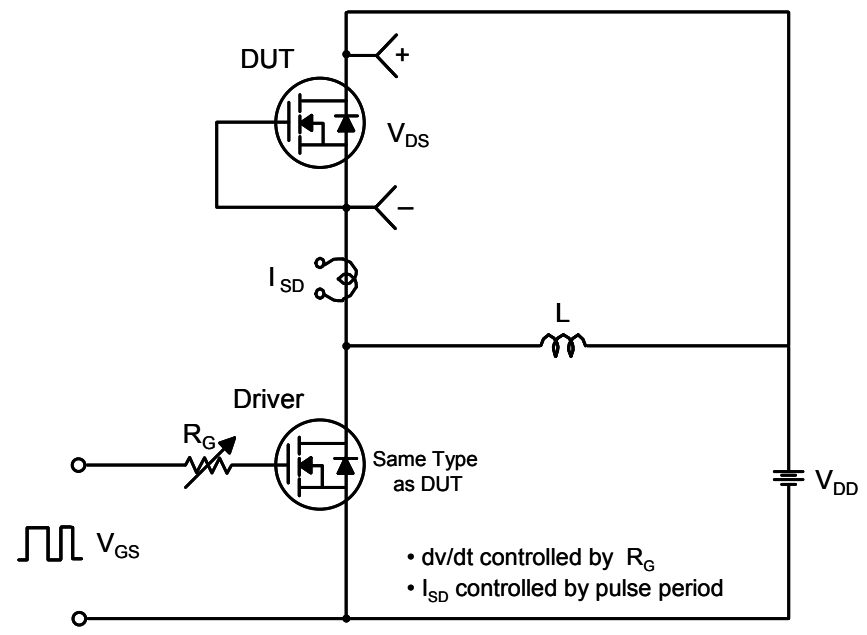
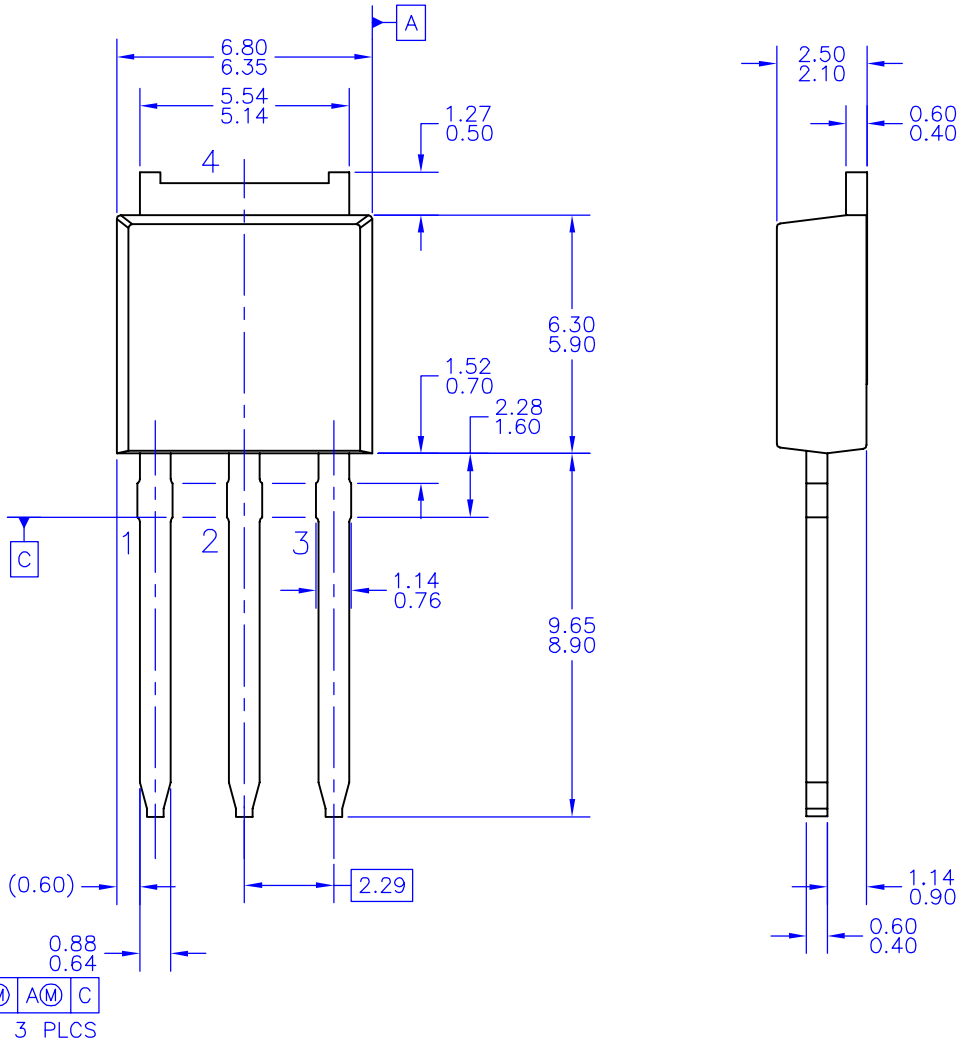


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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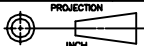
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LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	CB/G31/01	16MAR2001	RM



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- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.






T0251A03REVA

APPROVALS	DATE	 <b>CEBU PHILIPPINES</b>
DRAWN: J. GOMEZ	16MAR2001	
CHECKED: R. MANABIT		
APPROVED: M. GESTOLE		
G.S. BAJE		<b>TO-251 (I-PAK) MOLDED, 3 LEAD, OPTION AA</b>
		SCALE: 8:1 SIZE: A3 FORMERLY: N/A
		DRAWING NUMBER: MKT-T0251A03 REV: A SHEET: 1 OF 1



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