PIC16F87/88

Flash Memory Programming Specification

1.0 DEVICE OVERVIEW

This document includes programming specifications for the following devices:

- PIC16F87
- PIC16F88

2.0 PROGRAMMING THE PIC16F87/88

The PIC16F87/88 is programmed using a serial method. The Serial mode will allow the PIC16F87/88 to be programmed while in the user's system, which allows for increased design flexibility. This programming specification applies to PIC16F87/88 devices in all packages.

2.1 Programming Algorithm Requirements

The programming algorithm used depends on the operating voltage (V_{DD}) of the PIC16F87/88 device.

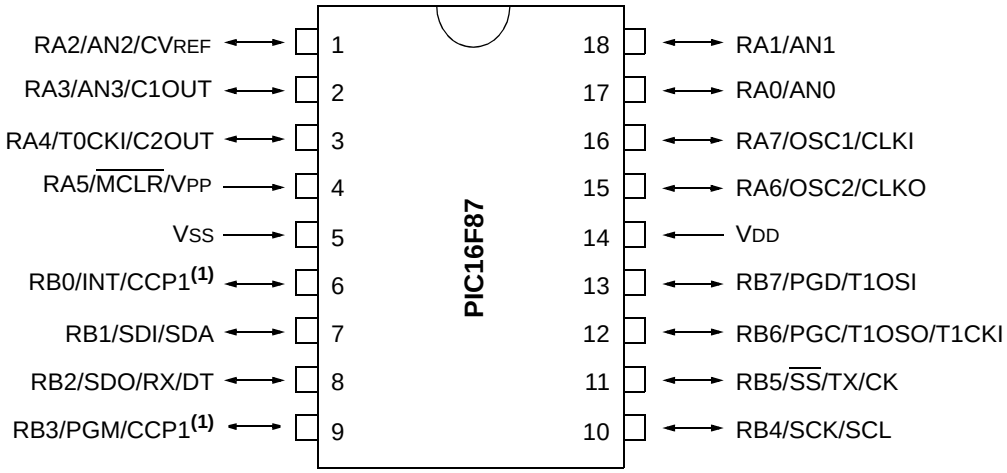
Algorithm #	V_{DD} Range
1	$2.0V \le V_{DD} < 5.5V$
2	$4.5V \le V_{DD} \le 5.5V$

Both algorithms can be used with the two available programming entry methods. The first method, called Low-Voltage ICSP™ (LVP for short), applies V_{DD} to $\overline{MCLR}$ and uses the I/O pin RB3 to enter Programming mode. When RB3 is driven to V_{DD} from ground, the PIC16F87/88 device enters Programming mode. The second method follows the normal Microchip Programming mode entry of holding pins RB6 and RB7 low, while raising the $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (13V ± 0.5V).

2.2 Programming Mode

The Programming mode for the PIC16F87/88 allows programming of user program memory, data memory, special locations used for ID, and the Configuration Words.

FIGURE 2-1: PIC16F87 18-PIN DIP, SOIC



Note 1: Location of CCP1 function is determined by CCPMX.

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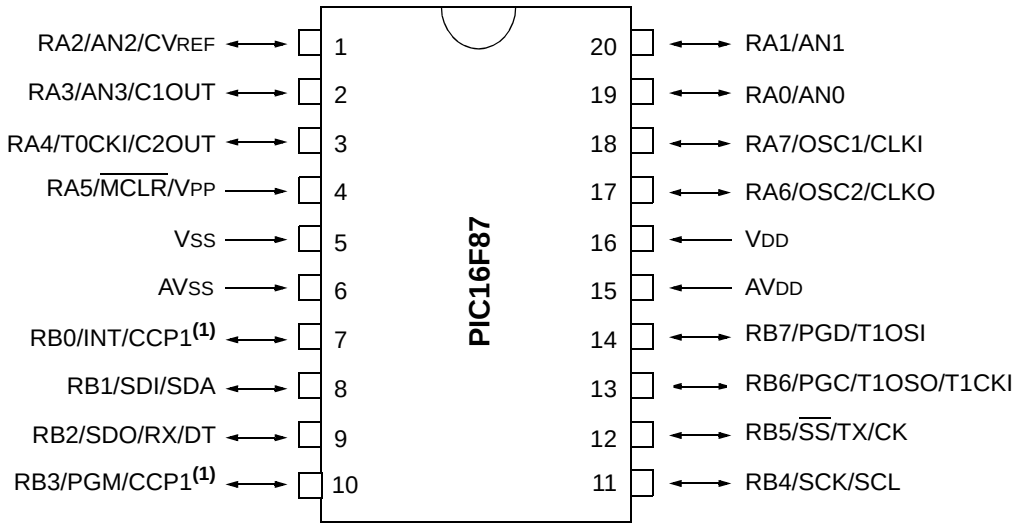
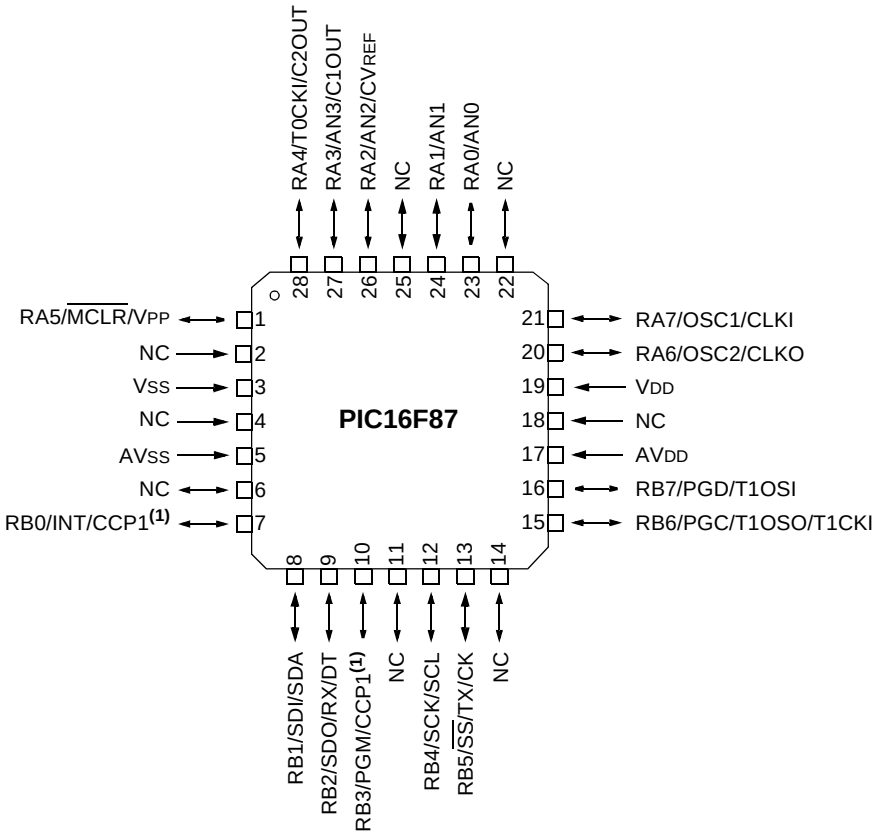
FIGURE 2-2: PIC16F87 20-PIN SSOP



Note 1: Location of CCP1 function is determined by CCPMX.

FIGURE 2-3: PIC16F87 28-PIN QFN



Note 1: Location of CCP1 function is determined by CCPMX.

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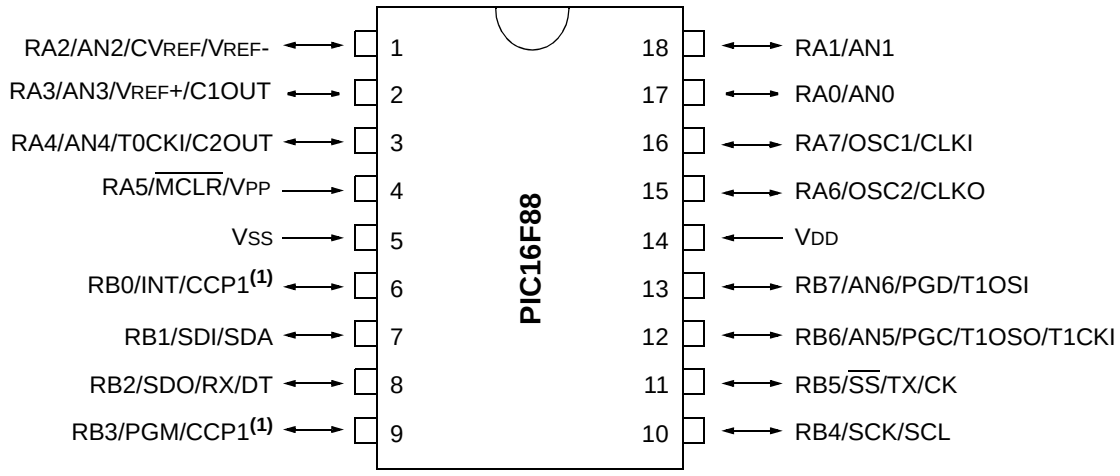
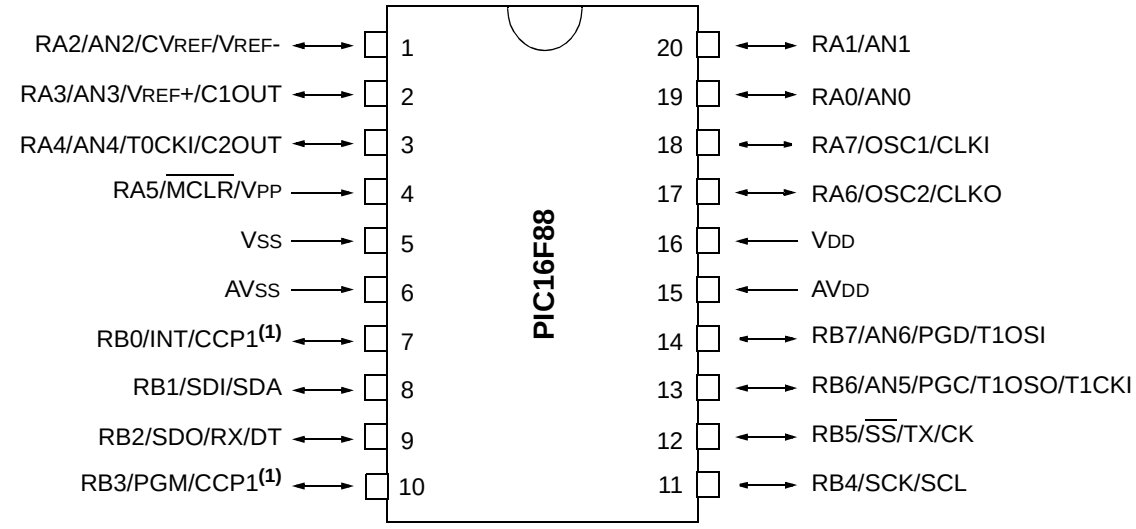
FIGURE 2-4: PIC16F88 18-PIN DIP, SOIC



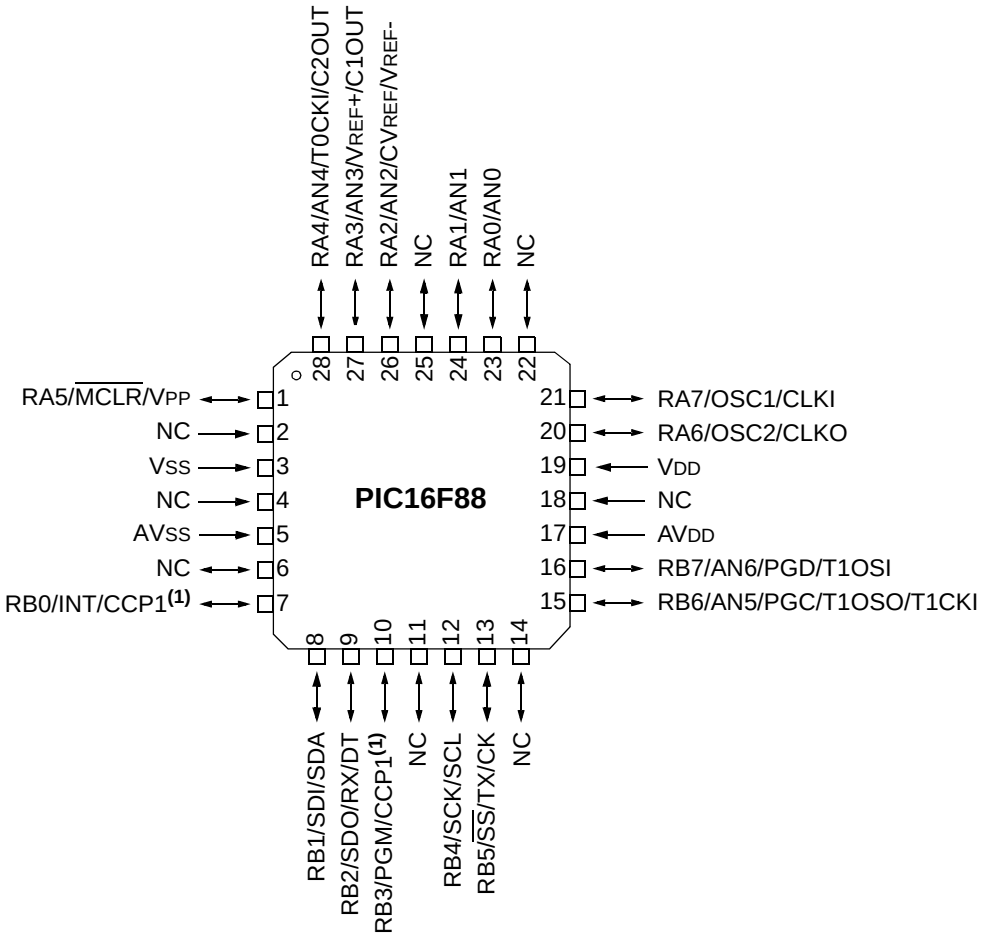
Note 1: Location of CCP1 function is determined by CCPMX.

FIGURE 2-5: PIC16F88 20-PIN SSOP



Note 1: Location of CCP1 function is determined by CCPMX.

FIGURE 2-6: PIC16F88 28-PIN QFN



Note 1: Location of CCP1 function is determined by CCPMX.

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16F87/88

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB3	PGM	I	Low-Voltage ICSP™ Programming Input if LVP Configuration bit equals '1'
RB6	CLOCK	I	Clock Input
RB7	DATA	I/O	Data Input/Output
$\overline{MCLR}$	VPP	P*	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

* To activate the Programming mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since $\overline{MCLR}$ is used for a level source, this means that $\overline{MCLR}$ does not draw any significant current.

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3.0 PROGRAM MODE ENTRY

3.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K), of which 4K (0000h-0FFFh) is physically implemented. In Programming mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x0FFF, then increment to 0x1000 and access 0x0000. Once the PC reaches 0x1FFF, it will increment to 0x2000. From 0x2000, the PC will increment up to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program mode, as described in **Section 3.4 "Program Mode"**.

Device	Program Flash
PIC16F87	4K
PIC16F88	4K

In the configuration memory space, 0x2000-0x201F are physically implemented. However, only locations 0x2000 through 0x2008 are available. Other locations are reserved. Locations beyond 0x201F will physically access user memory (see Figure 3-1).

3.2 Data EEPROM Memory

The EEPROM data memory space is a separate block of high-endurance memory that the user accesses using a special sequence of instructions. The amount of data EEPROM memory depends on the device and is shown below in number-of-bytes.

Device	# of Bytes
PIC16F87	256
PIC16F88	256

The contents of data EEPROM memory have the capability to be embedded into the HEX file.

The programmer should be able to read data EEPROM information from a HEX file and conversely (as an option) write data EEPROM contents to a HEX file, along with program memory information and Configuration bit information.

The 256 data memory locations are logically mapped and use PC<7:0>. The format for data memory storage is one data byte per address location, LSb aligned.

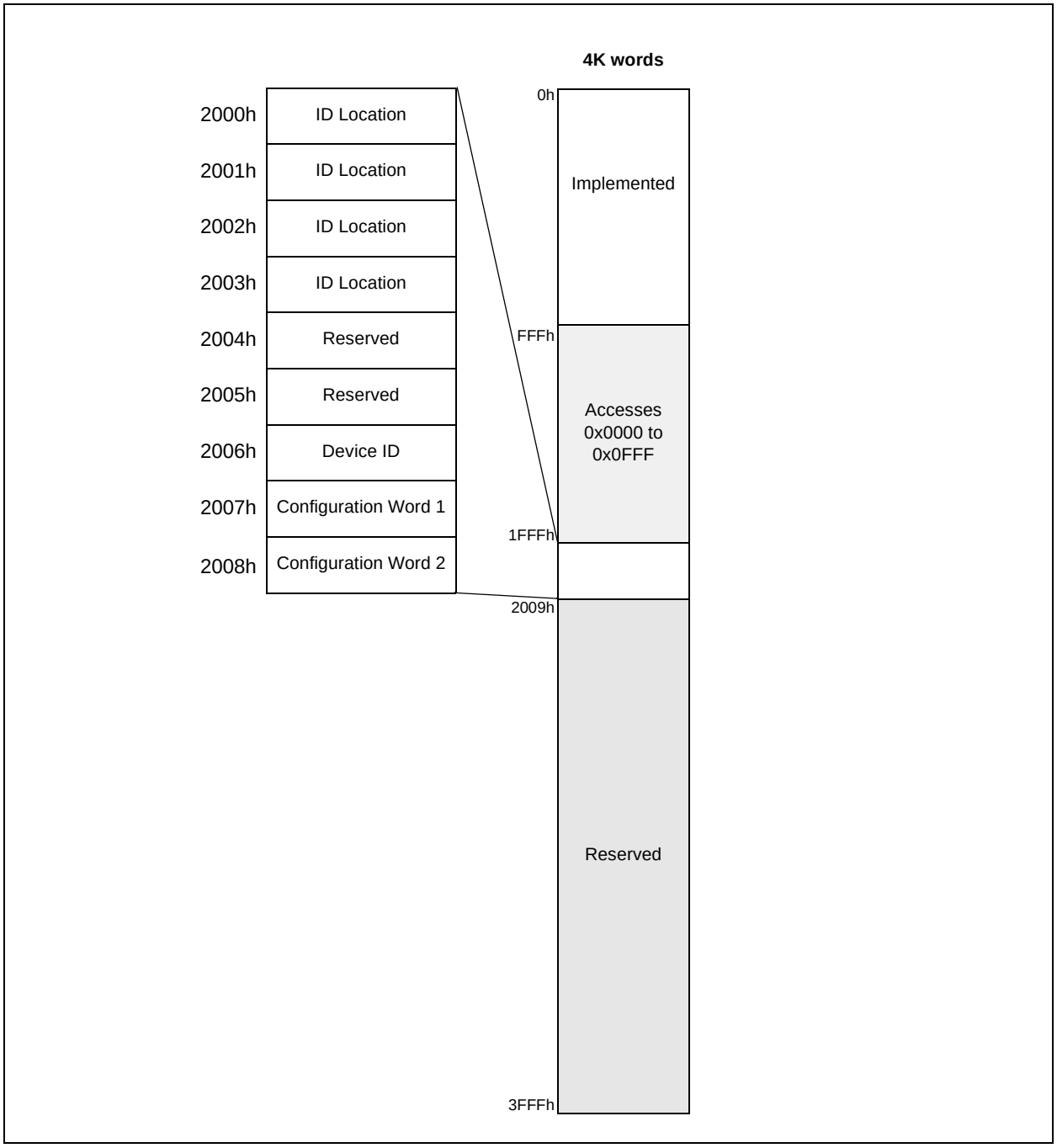
3.3 ID Locations

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000:0x2003]. It is recommended that the user use only the four Least Significant bits of each ID location. In some devices, the ID locations read out in an unscrambled fashion once code-protection is enabled.

For these devices, it is recommended that ID location be written as "11 1111 1000 bbbb", where 'bbbb' is ID information.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 6-1.

FIGURE 3-1: PROGRAM MEMORY MAPPING



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3.4 Program Mode

Program mode is entered by holding pins RB6 and RB7 low, while raising MCLR pin from VIL to VIHH (high voltage). In this mode, the state of the RB3 pin does not effect programming. Low-Voltage ICSP Programming mode is entered by raising RB3 from VIL to VDD, and then applying VDD to MCLR. Once in this mode, the user program memory, as well as the configuration memory, can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory accessed is the user program memory. RB6 and RB7 are Schmitt Trigger inputs in this mode.

Note:	The Osc must not have 72 osc clocks while the device MCLR is between VIL and VIHH.

The sequence that enters the device into the Programming mode places all other logic into the RESET state (the MCLR pin was initially at VIL). This means all I/O are in the RESET state (high-impedance inputs).

Note:	The MCLR pin should be raised from below VIL to above the minimum VIHH (VPP), within 250 µs of VDD rise. This ensures that the device always enters Programming mode before any instructions that may be in program memory can be executed. Otherwise, unintended instruction execution could occur when the INTRC clock source is configured as the primary clock. Refer to Figure 7-1.

A device RESET will clear the PC and set the address to '0'. The 'Increment Address' command will increment the PC. The 'Load Configuration' command will set the PC to 0x2000. The available commands are shown in Table 3-1.

The normal sequence for programming four program memory words at a time is as follows:

1. Set pointer to row location.
2. Issue a 'Begin Erase' command.
3. Wait tprog2.
4. Issue an 'End Programming' command.
5. Load a word at the current program memory address using the 'Load Data' command.
6. Issue an 'Increment Address' command.
7. Load a word at the current program memory address using the 'Load Data' command.
8. Repeat Step 6 and Step 7 two times.
9. Issue a 'Begin Programming' command to begin programming.
10. Wait tprog1.
11. Issue an 'End Programming' command.
12. Increment to the next address.
13. Repeat steps 5 through 12 seven times to program one row.

The address and program counter are reset to 0x0000 by resetting the device (taking MCLR below VIL) and re-entering Programming mode. Program and configuration memory may then be read or verified using the 'Read Data' and 'Increment Address' commands.

3.4.1 LOW-VOLTAGE ICSP PROGRAMMING MODE

Low-voltage ICSP Programming mode allows a PIC16F87/88 device to be programmed using VDD only. However, when this mode is enabled by a Configuration bit (LVP), the PIC16F87/88 device dedicates RB3 to control entry/exit into Programming mode.

When the LVP bit is set to '1', the Low-voltage ICSP Programming entry is enabled. Since the LVP Configuration bit allows Low-voltage ICSP Programming entry in its erased state, an erased device will have the LVP bit enabled at the factory. While LVP is '1', RB3 is dedicated to Low-voltage ICSP Programming. The following LVP steps assume the LVP bit is set in the Configuration register.

1. Apply VDD to the VDD pin.
2. Drive MCLR low.
3. Apply VDD to the RB3/PGM pin.
4. Apply VDD to the MCLR pin.

All other specifications for High-voltage ICSP apply.

To disable Low-voltage ICSP mode, the LVP bit must be programmed to '0'. This must be done while entered with the High-voltage Entry mode (LVP bit = 1). RB3 is now a general purpose I/O pin.

3.4.2 SERIAL PROGRAM OPERATION

The RB6 pin is used as a clock input pin, while the RB7 pin is used to enter command bits, and input or output data during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock, with the Least Significant bit (LSb) of the command being input first. The data on RB7 is required to have a minimum setup (tset1) and hold (thold1) time (see AC/DC specifications), with respect to the falling edge of the clock. Commands with associated data (read and load) are specified to have a minimum delay (tdly1) of 1 μs between the command and the data. After this delay, the clock pin is cycled 16 times, with the first cycle being a Start bit (0) and the last cycle being a Stop bit (0). Data is transferred LSb first.

During a read operation, the LSb will be transmitted onto RB7 on the rising edge of the second cycle, while, during a load operation, the LSb will be latched on the falling edge of the second cycle. A minimum 1 μs delay (tdly2) is specified between consecutive commands.

All commands and data words are transmitted LSb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow decoding of commands and reversal of data pin configuration, a time separation of at least 1 μs (tdly1) is required between a command and a data word, or another command.

The available commands are described in the following paragraphs and listed in Table 3-1.

3.4.2.1 Load Configuration

Upon receipt of the Load Configuration command, the PC will be set to 0x2000 and the data sent with the command is discarded. The four ID locations and the Configuration Words can then be programmed using the normal programming sequence, as described in **Section 3.4 "Program Mode"**. A description of the memory mapping schemes of the program memory for normal operation and Configuration mode operation is shown in Figure 3-1. Once the configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify Test mode by taking $\overline{MCLR}$ low (V_{IL}).

3.4.2.2 Load Data for Program Memory

After receiving this command, the chip will load one word (with 14 bits as a "data word") to be programmed into user program memory when 16 cycles are applied. A timing diagram for this command is shown in Figure 7-1.

3.4.2.3 Load Data for Data Memory

After receiving this command, the chip will load a 14-bit "data word" when 16 cycles are applied. However, the data memory is only 8 bits wide and, thus, only the first 8 bits of data after the Start bit will be programmed into the data memory (8 data bits and 6 zeros). It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains up to 256 bytes. If the device is code protected, the data is read as all zeros. A timing diagram for this command is shown in Figure 7-2.

3.4.2.4 Read Data from Program Memory

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The RB7 pin will go into Output mode on the second rising clock edge, reverting to Input mode (high-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 7-3.

3.4.2.5 Read Data from Data Memory

After receiving this command, the chip will transmit data bits out of the data memory, starting with the second rising edge of the clock input. The RB7 pin will go into Output mode on the second rising edge, reverting to Input mode (high-impedance) after the 16th rising edge. As previously stated, the data memory is 8-bits wide and, therefore, only the first 8 bits that are output are actual data. A timing diagram for this command is shown in Figure 7-4.

3.4.2.6 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 7-5.

Note:	Upon entering Programming mode, a "Load Data for Program Memory" or "Load Data for Data Memory" command of 0x01 must be given before a Begin Erase or Begin Programming command is initiated. This will ensure that the programming pointer is pointing to the correct location in data or program memory.

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3.4.2.7 Begin Erase (Program and Data Memory)

The erase block size for program memory is 32 words (row) and 1 word for data memory. The row or word to be programmed must first be erased. This is done by setting the pointer to a location in the row or word and then performing a 'Begin Erase' command. The row or word is then erased. The user must allow the combined time for row erase and programming, as specified in the electrical specifications, for programming to complete. This is an externally timed event.

The internal timer is not used for this command, so the 'End Programming' command must be used to stop erase.

Note 1:	The code-protect bits cannot be erased with this command.
2:	All 'Begin Erase' operations can take place over the entire V_{DD} range.

A timing diagram for this command is shown in Figure 7-6.

3.4.2.8 Begin Programming Only

Programming of program and data memory will begin once this command is received and decoded. The user must allow the time for programming, as specified in the electrical specifications, for programming to complete. An 'End Programming' command is required.

The internal timer is not used for this command, so the 'End Programming' command must be used to stop programming.

1. If the address is pointing to user memory, the user memory alone will be affected.
2. If the address is pointing to the physically implemented configuration memory (2000h-2008h), the configuration memory will be written. The Configuration Words will not be written unless the address is specifically pointing to the corresponding address.

A timing diagram for this command is shown in Figure 7-7.

3.4.2.9 End Programming

After receiving this command, the chip stops programming the memory (configuration memory or user program memory) that it was programming at the time.

Note:	This command will also set the write data shift latches to all '1's to avoid issues with downloading only one word before the write.

TABLE 3-1: COMMAND MAPPING FOR PIC16F87/88

Command	Mapping (MSB … LSB)					Data	Voltage Range
Load Configuration	0	0	0	0	0	0, data (14), 0	2.0V-5.5V
Load Data for Program Memory	0	0	0	1	0	0, data (14), 0	2.0V-5.5V
Read Data from Program Memory	0	0	1	0	0	0, data (14), 0	2.0V-5.5V
Increment Address	0	0	1	1	0		2.0V-5.5V
Begin Erase	0	1	0	0	0	externally timed	2.0V-5.5V
Begin Programming Only Cycle	1	1	0	0	0	externally timed	2.0V-5.5V
Bulk Erase Program Memory	0	1	0	0	1	externally timed	4.5V-5.5V
Bulk Erase Data Memory	0	1	0	1	1	externally timed	4.5V-5.5V
Chip Erase	1	1	1	1	1	internally timed	4.5V-5.5V
Load Data for Data Memory	0	0	0	1	1	0, zeroes (6), data (8), 0	2.0V-5.5V
Read Data from Data Memory	0	0	1	0	1	0, zeroes (6), data (8), 0	2.0V-5.5V
End Programming	1	0	1	1	1		

3.5 Erasing Program and Data Memory

Depending on the state of the code protection bits, program and data memory will be erased using different methods. The first two commands are used when both program and data memories are not code protected. The third command is used when either memory is code protected, or if you want to also erase the code protect bits. A device programmer should determine the state of the code protection bits and then apply the proper command to erase the desired memory.

3.5.1 ERASING PROGRAM AND DATA MEMORY

When both program and data memories are not code-protected, they can be individually erased by the following 'Bulk Erase' commands. If it is desired to erase both program and data memory with a single command, the 'Chip Erase' command must be used whether code protection is disabled or enabled (detailed in **Section 3.5.1.3 "Chip Erase"**).

3.5.1.1 Bulk Erase Program Memory

When this command is performed, and is followed by a 'Begin Erase' command, the entire program memory will be erased.

If the address is pointing to user memory, only the user memory will be erased.

If the address is pointing to the configuration memory (2000h-2008h), then both the user memory and the configuration memory will be erased. The Configuration Words will not be erased, even if the address is pointing to location 2007h.

Previously, a load data with 0FFh command was recommended before any 'Bulk Erase'. On these devices, this will not be required.

The 'Bulk Erase' command is disabled when the CP bit is programmed to '0', enabling code-protect.

A timing diagram for this command is shown in Figure 7-8.

3.5.1.2 Bulk Erase Data Memory

When this command is performed, and is followed by a 'Begin Erase' command, the entire data memory will be erased.

The 'Bulk Erase Data' command is disabled when the CPD bit is programmed to '0', enabling protected data memory. A timing diagram for this command is shown in Figure 7-9.

Note:	All 'Bulk Erase' operations must take place at the 4.5V to 5.5V VDD range.

3.5.1.3 Chip Erase

This command, when performed, will erase the program memory, EE data memory, and all of the code protection bits. All on-chip Flash and EEPROM memory is erased, regardless of the address contained in the PC.

When a Chip Erase command is issued and the PC points to (0000h-1FFFh), the Configuration Words (2007h and 2008h) and the user program memory will be erased. When a Chip Erase command is issued and the PC points to (2000h-2008h), all of the configuration memory, program memory, and data memory will be erased.

The Chip Erase is internally self-timed to ensure that all program and data memory are erased before the code protect bits are erased. A timing diagram for this command is shown in Figure 7-10.

Note:	The Chip Erase operation must take place at the 4.5V to 5.5V VDD range.

3.5.2 ERASING CODE-PROTECTED MEMORY

For the PIC16F87/88 devices, once code protection is enabled, all protected program and data memory locations read all '0's and further programming is disabled. The ID locations and Configuration Words read out unscrambled and can be reprogrammed normally. The only command to erase a code-protected PIC16F87/88 device is the 'Chip Erase'. This erases program memory, data memory, Configuration bits and ID locations, as described in **Section 3.5.1.3 "Chip Erase"**. **Since all data within the program and data memory will be erased when this command is executed, the security of the data or code is not compromised.**

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FIGURE 3-2: ALGORITHM 1 FLOWCHART – PROGRAM MEMORY (2.0V ≤ VDD < 5.5V)

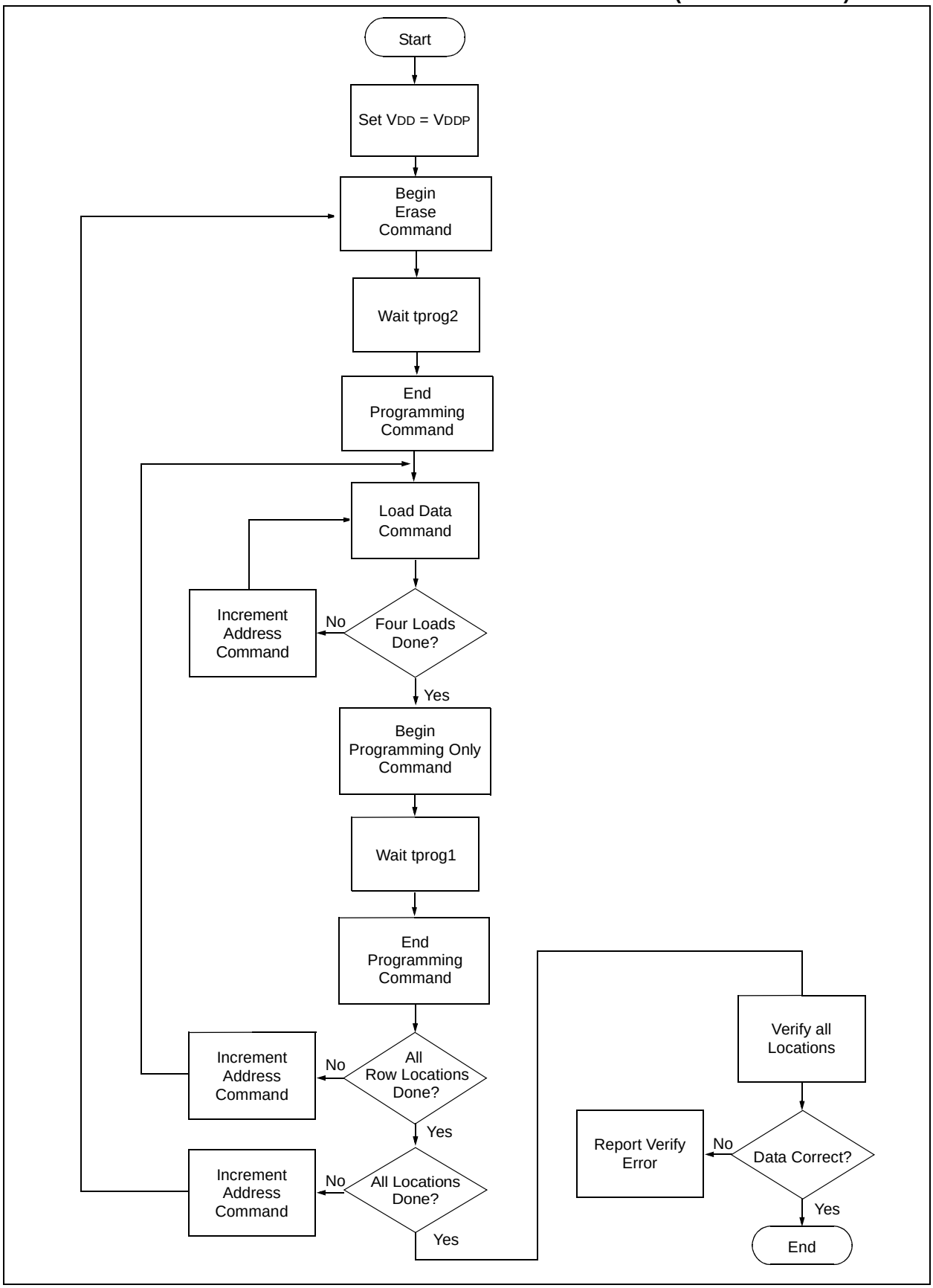

FIGURE 3-3: ALGORITHM 2 FLOWCHART – PROGRAM MEMORY (4.5V ≤ VDD ≤ 5.5V)

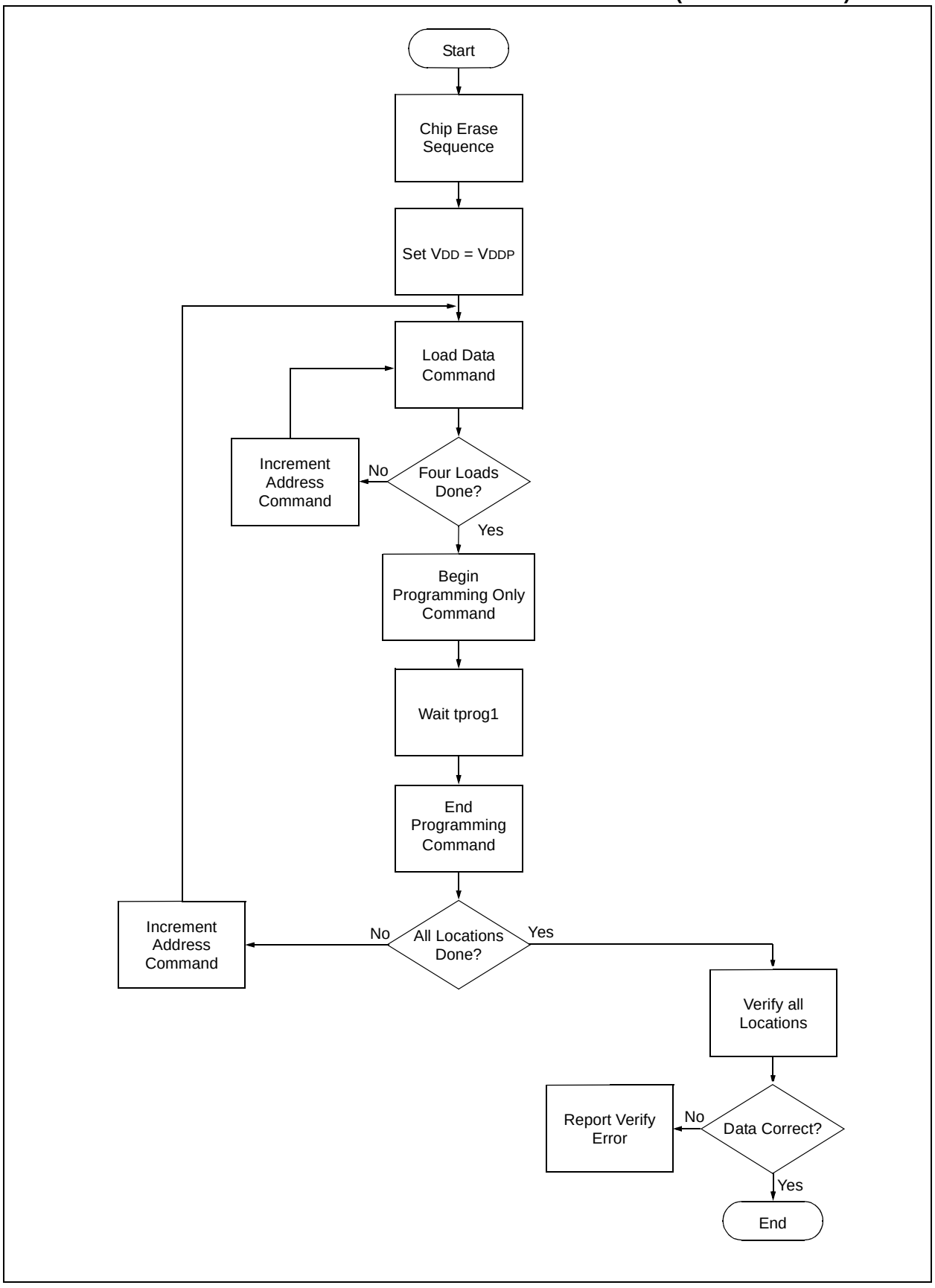

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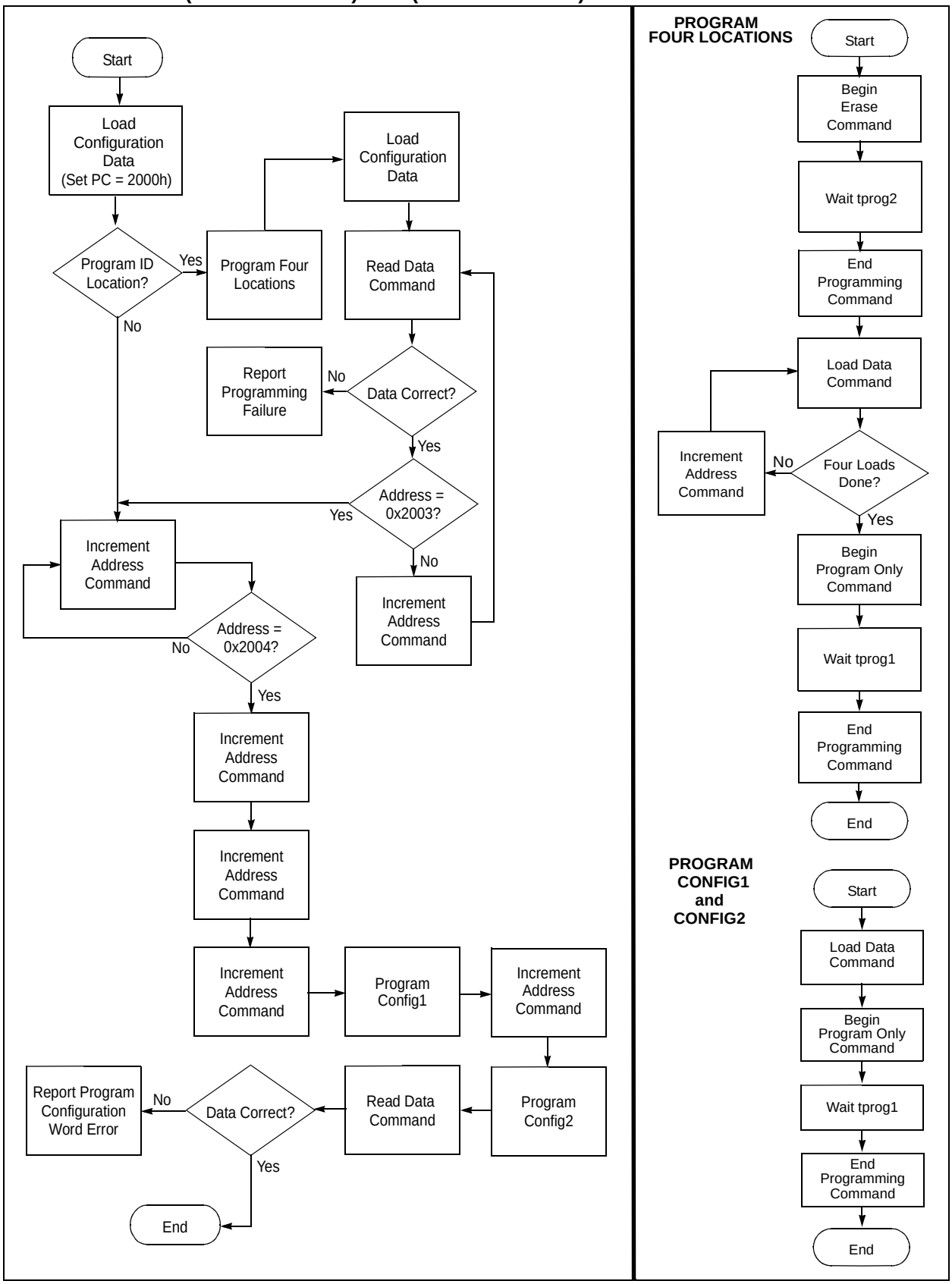
FIGURE 3-4: FLOWCHART – PIC16F87/88 CONFIGURATION MEMORY (2.0V ≤ VDD < 5.5V) AND (4.5V ≤ VDD < 5.5V)



4.0 CONFIGURATION WORD

The PIC16F87/88 has several Configuration bits. These bits can be written to '0' or '1' with the 'Begin Program Only' command. A 'Begin Erase' command is not required when programming configuration memory.

4.1 Device ID Word

The device ID word for the PIC16F87/88 is located at 2006h.

TABLE 4-1: DEVICE ID VALUE

Device	Device ID Value	
	Dev	Rev
PIC16F87	00 0111 0010	XXXX
PIC16F88	00 0111 0110	XXXX

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REGISTER 4-1: CONFIGURATION WORD 1 (2007h) REGISTER

CP	CCPMX	DEBUG	WRT1	WRT0	CPD	LVP	BOREN	MCLRE	FOSC2	$\overline{\text{PWRTEN}}$	WDTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13 **CP:** Flash Program Memory Code Protection bits
1 = Code protection off
0 = 0000h to 0FFFh code protected (all protected)

bit 12 **CCPMX: CCP** Mux bit
1 = CCP1 function on RB0
0 = CCP1 function on RB3

bit 11 **DEBUG:** In-Circuit Debugger Mode bit
1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins
0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger

bit 10-9 **WRT1:WRT0:** Flash Program Memory Write Enable bits
11 = Write protection off
10 = 0000h to 00FFh write-protected, 0100h to 0FFFh may be modified by EECON control
01 = 0000h to 07FFh write-protected, 0800h to 0FFFh may be modified by EECON control
00 = 0000h to 0FFFh write-protected

bit 8 **CPD:** Data EE Memory Code Protection bit
1 = Code protection off
0 = Data EE memory code-protected

bit 7 **LVP:** Low-voltage Programming Enable bit
1 = RB3/PGM pin has PGM function, Low-voltage Programming enabled
0 = RB3 is digital I/O, HV on $\overline{\text{MCLR}}$ must be used for programming

bit 6 **BOREN:** Brown-out Reset Enable bit
1 = BOR enabled
0 = BOR disabled

bit 5 **MCLRE:** RA5/$\overline{\text{MCLR}}$ Pin Function Select bit
1 = RA5/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RA5/$\overline{\text{MCLR}}$ pin function is digital I/O, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 3 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 4, 1-0 **FOSC2:FOSC0:** Oscillator Selection bits
111 = EXTRC oscillator; CLKO function on RA6/OSC2/CLKO
110 = EXTRC oscillator; port I/O function on RA6/OSC2/CLKO
101 = INTRC oscillator; CLKO function on RA6/OSC2/CLKO
100 = INTRC oscillator; port I/O function on RA6/OSC2/CLKO
011 = EXTCLK; port I/O function on RA6/OSC2/CLKO
010 = HS oscillator
001 = XT oscillator
000 = LP oscillator

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

REGISTER 4-2: CONFIGURATION WORD 2 (2008h) REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1		
—	—	—	—	—	—	—	—	—	—	—	—	IESO	FCMEN
bit 13													bit 0

bit 13-2 Unimplemented: Read as '1'

bit 1 **IESO:** Internal External Switch Over bit
1 = Internal External Switch Over mode enabled
0 = Internal External Switch Over mode disabled

bit 0 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = Fail-Safe Clock Monitor enabled
0 = Fail-Safe Clock Monitor disabled

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

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5.0 EMBEDDING CONFIGURATION WORD AND ID INFORMATION IN HEX FILE

To allow portability of code, the programmer is required to read the Configuration Word and ID locations from the HEX file when loading the HEX file. If Configuration Word information was not present in the HEX file, a simple warning message may be issued. Similarly, while saving a HEX file, Configuration Word and ID information must be included. An option to not include this information may be provided.

Specifically for the PIC16F87/88, the EEPROM data memory should also be embedded in the HEX file (see **Section 3.2 "Data EEPROM Memory"**).

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

6.0 CHECKSUM COMPUTATION

Checksum is calculated by reading the contents of the PIC16F87/88 memory locations and totaling the opcodes, up to the maximum user-addressable location (e.g., 0xFFF for the PIC16F87/88). Any carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16F87/88 devices is shown in Table 6-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Words, appropriately masked
- Masked ID locations (when applicable)

The Least Significant 16 bits of this sum are the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The Configuration Words and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 6-1: CHECKSUM COMPUTATION

Device	Code-Protect	Checksum*	Blank Value	0x25E6 at 0 and Max Address
PIC16F87	OFF	SUM(0000:0FFF) + (CONFIG0 & 3FFF) + (CONFIG1 & 0003)	3002	FBD0
	ON	(CONFIG0 & 3FFF) + (CONFIG1 & 0003) + SUM_ID	5004	IBD2
PIC16F88	OFF	SUM(0000:0FFF) + (CONFIG0 & 3FFF) + (CONFIG1 & 0003)	3002	FBD0
	ON	(CONFIG0 & 3FFF) + (CONFIG1 & 0003) + SUM_ID	5004	IBD2

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = ID locations masked by 0xF, then made into a 16-bit value with ID0 as the Most Significant nibble.
For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND

7.0 PROGRAM MODE ELECTRICAL CHARACTERISTICS

TABLE 7-1: TIMING REQUIREMENTS FOR PROGRAM MODE

AC/DC CHARACTERISTICS POWER SUPPLY PINS	**Standard Operating Procedure (unless otherwise stated)** Operating Temperature $0 \le T_A \le +70°C$ Operating Voltage $2.0V \le V_{DD} \le 5.5V$					
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
General						
V_{DD} level for Begin Erase, Begin Program operations and EECON1 writes of program memory	V_{DD}	2.0	—	5.5	V	
V_{DD} level for Begin Erase, Begin Program operations and EECON1 writes of data memory	V_{DD}	2.0	—	5.5	V	
V_{DD} level for Bulk Erase, Chip Erase, and Begin Program operations of program and data memory	V_{DD}	4.5	—	5.5	ms	
Begin Programming Only cycle time	tprog1	1	—	—	ms	Externally Timed, > 4.5V
		2	—	—	ms	Externally Timed, < 4.5V
Begin Erase	tprog2	1	—	—	ms	Externally Timed, > 4.5V
		2	—	—	ms	Externally Timed, < 4.5V
Bulk Erase cycle time	tprog3	10	—	—	ms	Externally Timed
Chip Erase cycle time	tprog4	10	—	—	ms	Internally Timed
High voltage on $\overline{MCLR}$ and RA4/T0CKI for Program mode entry	V_{IHH}	V_{DD} + 3.5	—	13.5	V	
$\overline{MCLR}$ rise time (V_{SS} to V_{HH}) for Program mode entry	tVHHR	—	—	1.0	µs	
(RB6, RB7) input high level	V_{IH1}	0.8 V_{DD}	—	—	V	Schmitt Trigger input
(RB6, RB7) input low level	V_{IL1}	0.2 V_{DD}	—	—	V	Schmitt Trigger input
RB<7:4> setup time before $\overline{MCLR}\uparrow$ (Program mode selection pattern setup time)	tset0	100	—	—	ns	
RB<7:4> hold time after $\overline{MCLR}\uparrow$ (Program mode selection pattern setup time)	thld0	5	—	—	µs	
Serial Program						
Data in setup time before clock↓	tset1	100	—	—	ns	
Data in hold time after clock↓	thld1	100	—	—	ns	
Data input not driven to next clock input (delay required between command/data or command/ command)	tdly1	1.0	—	—	µs	$2.0V \le V_{DD} < 4.5V$
		100	—	—	ns	$4.5V \le V_{DD} \le 5.5V$
Delay between clock↓ to clock↑ of next command or data	tdly2	1.0	—	—	µs	$2.0V \le V_{DD} < 4.5V$
		100	—	—	ns	$4.5V \le V_{DD} \le 5.5V$
Clock↑ to data out valid (during read data)	tdly3	80	—	—	ns	
Setup time between V_{DD} rise and $\overline{MCLR}$ rise	tpu	tset0	—	250	µs	

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FIGURE 7-1: LOAD DATA FOR USER PROGRAM MEMORY COMMAND (PROGRAM)

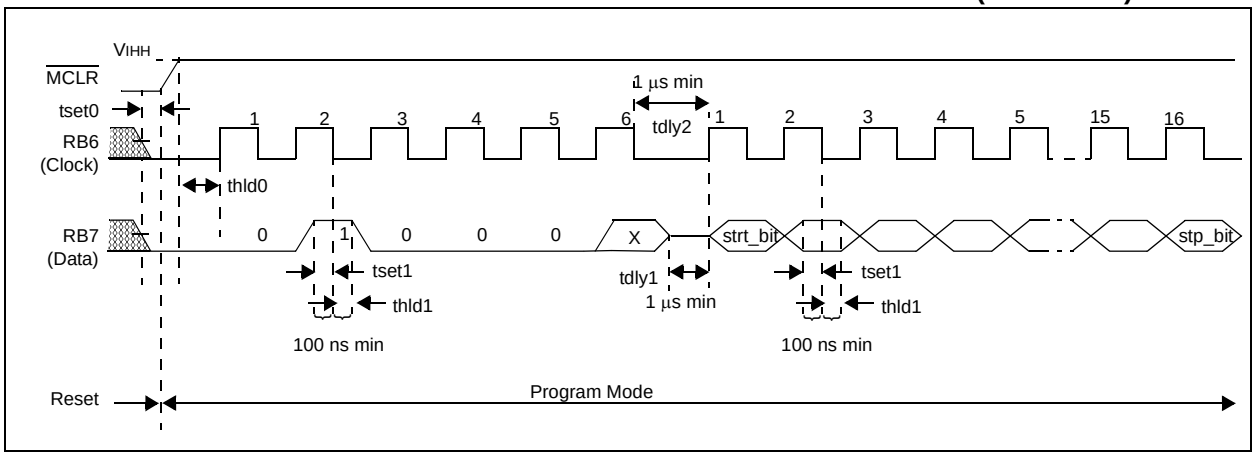

FIGURE 7-2: LOAD DATA FOR USER DATA MEMORY COMMAND (PROGRAM)

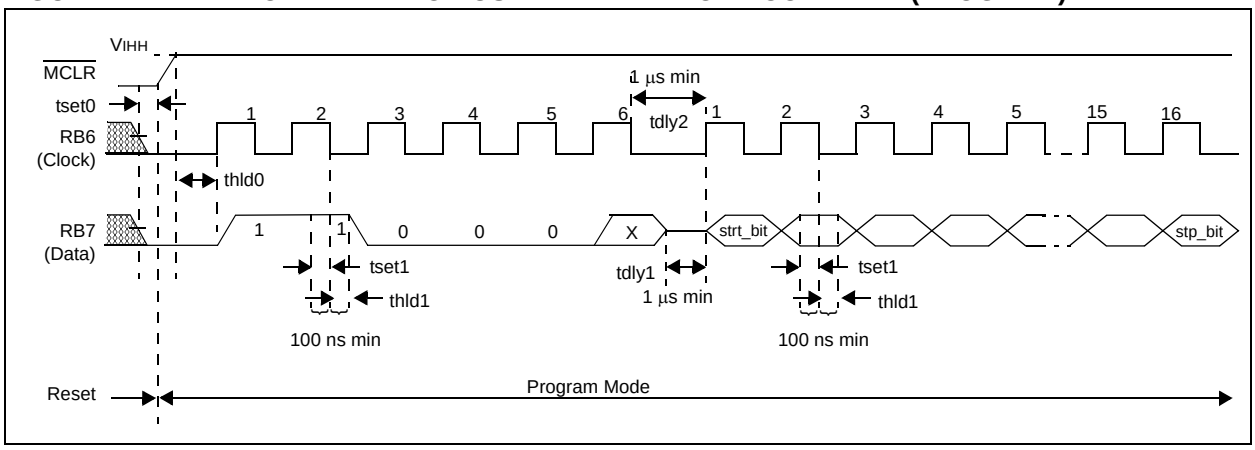

FIGURE 7-3: READ DATA FROM PROGRAM MEMORY COMMAND (PROGRAM)

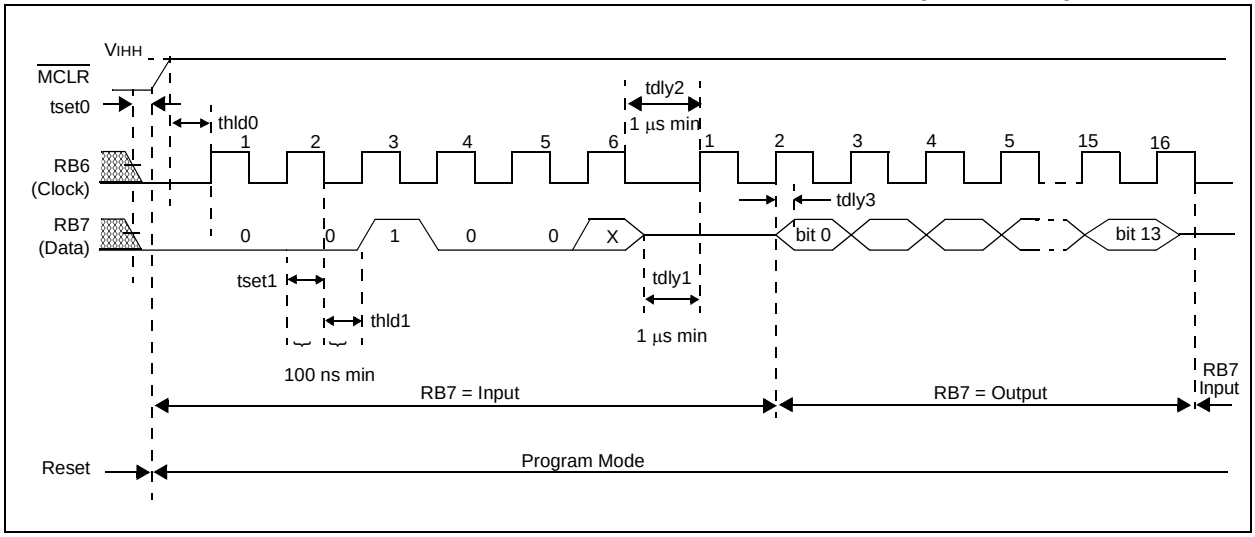

FIGURE 7-4: READ DATA FROM DATA MEMORY COMMAND (PROGRAM)

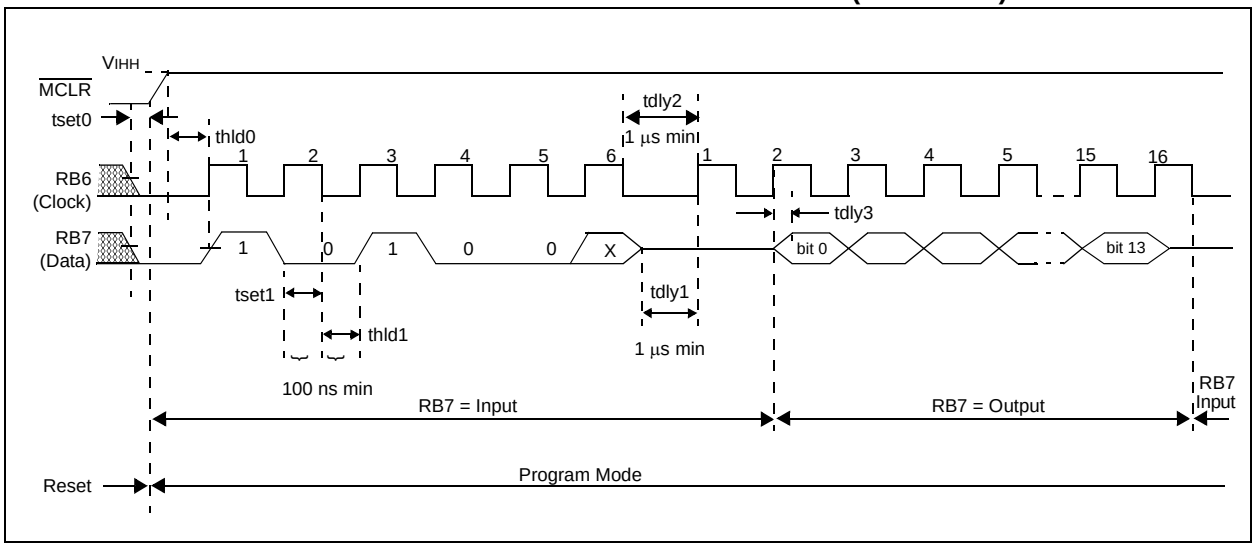

FIGURE 7-5: INCREMENT ADDRESS COMMAND (SERIAL PROGRAM)

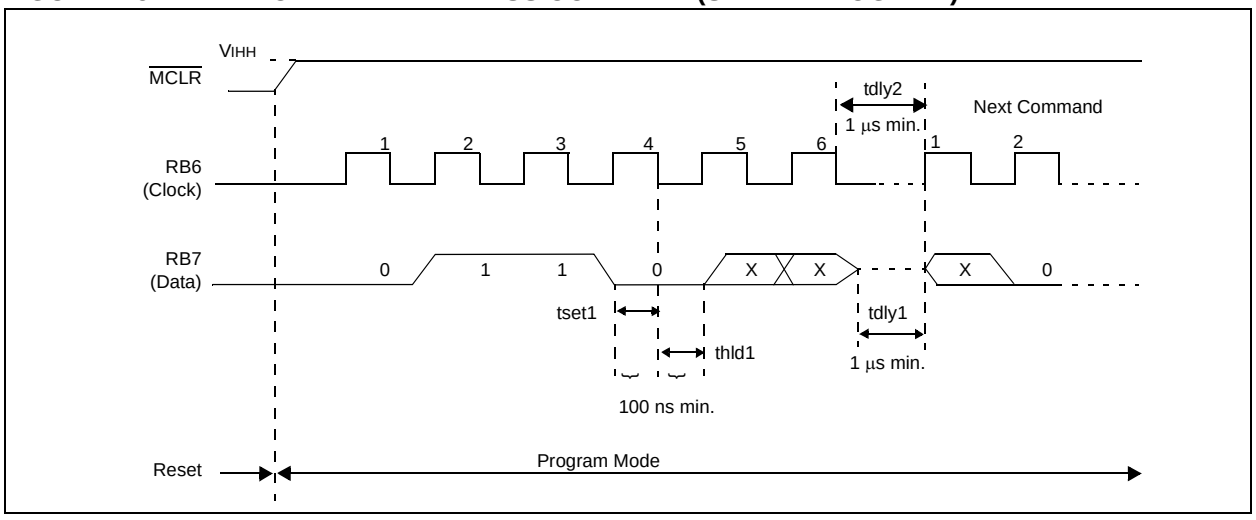

FIGURE 7-6: BEGIN ERASE (SERIAL PROGRAM)

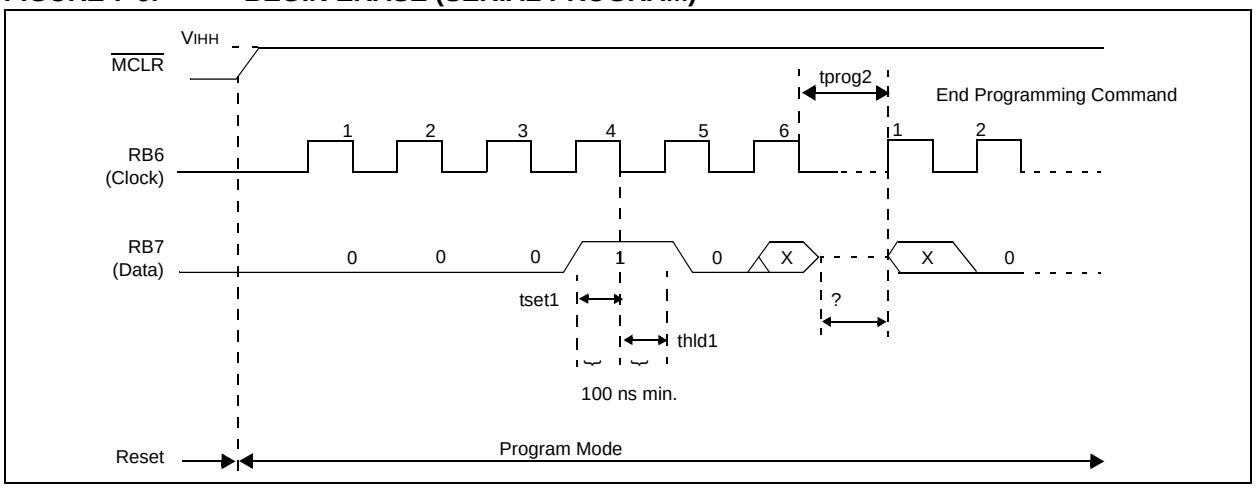

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FIGURE 7-7: BEGIN PROGRAMING ONLY COMMAND (SERIAL PROGRAM)

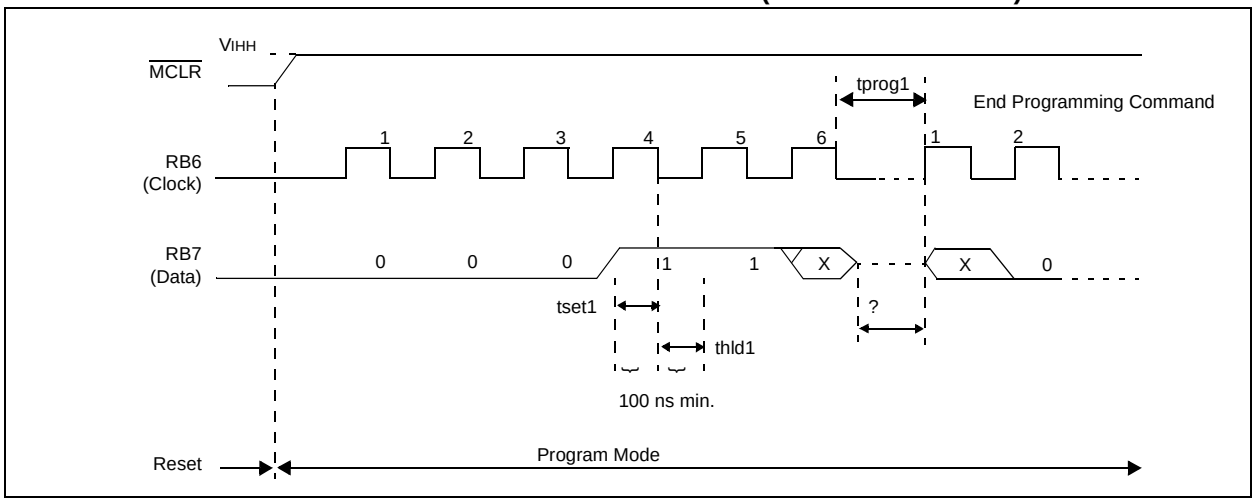


FIGURE 7-8: BULK ERASE PROGRAM MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

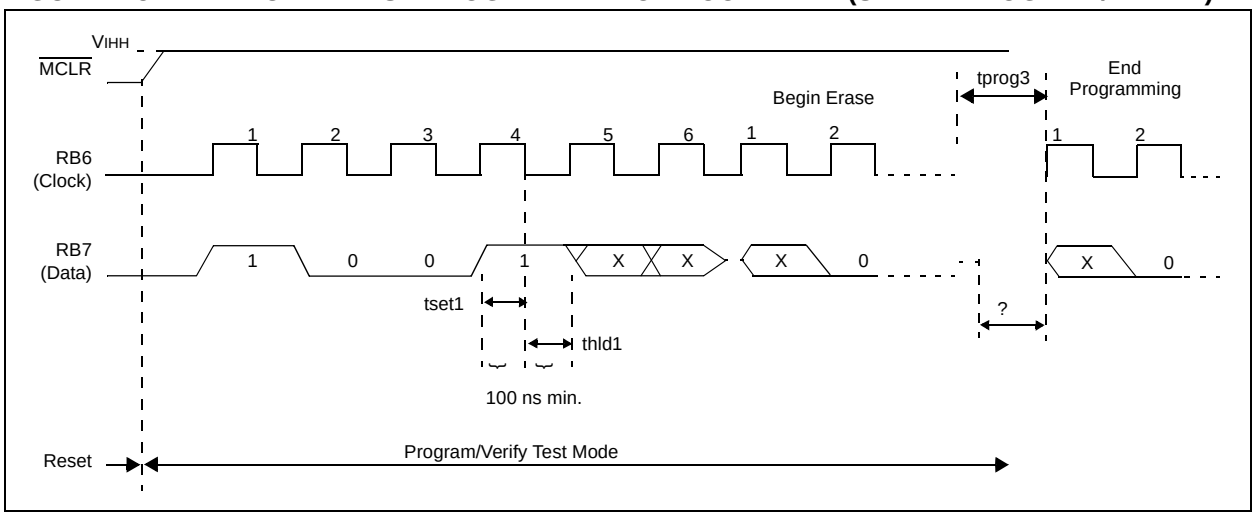


FIGURE 7-9: BULK ERASE DATA MEMORY COMMAND (SERIAL PROGRAM/VERIFY)

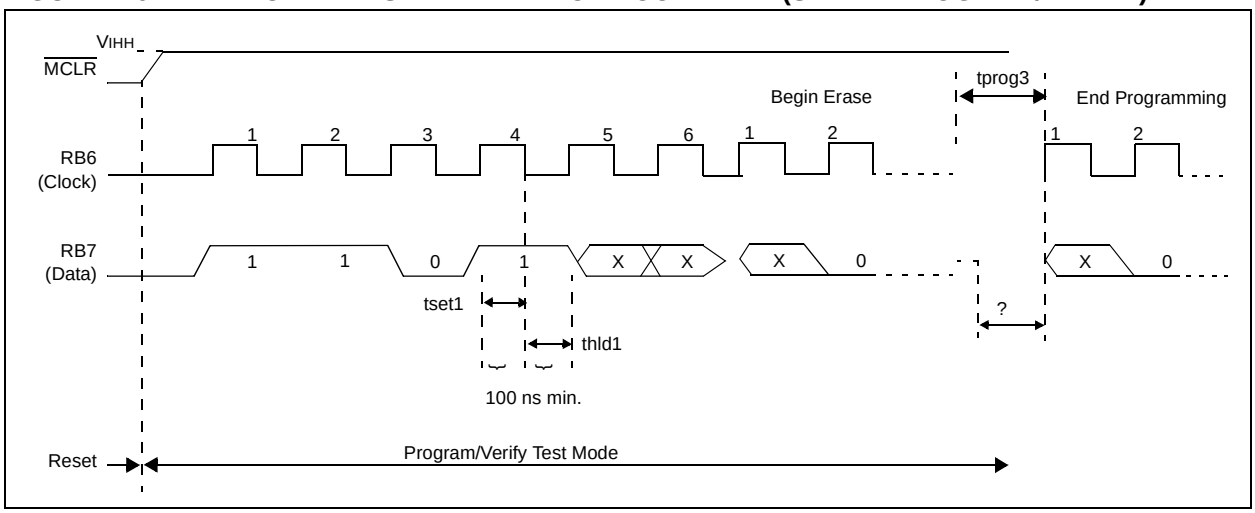


FIGURE 7-10: CHIP ERASE COMMAND (SERIAL PROGRAM)

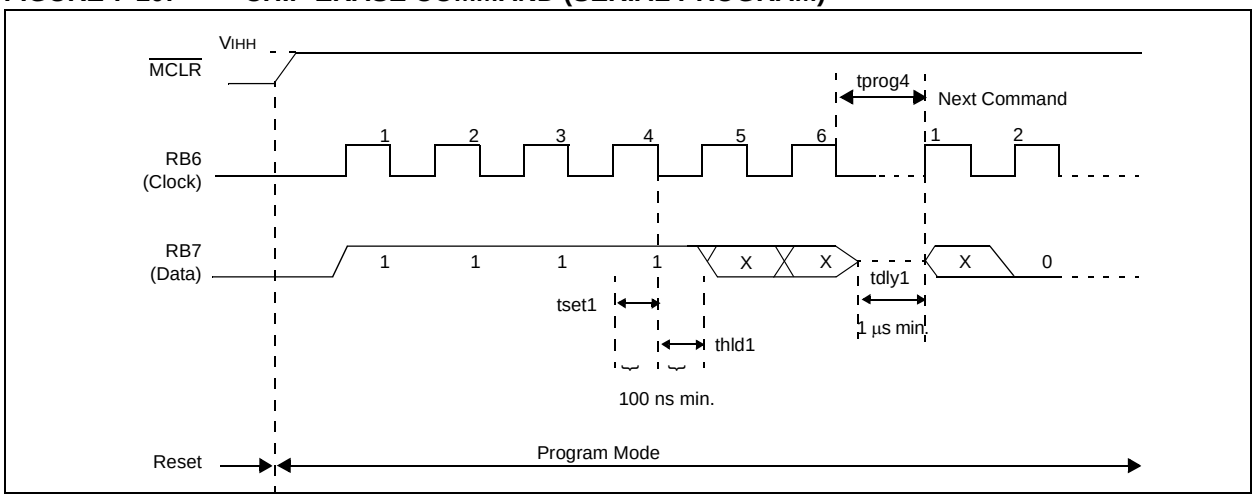
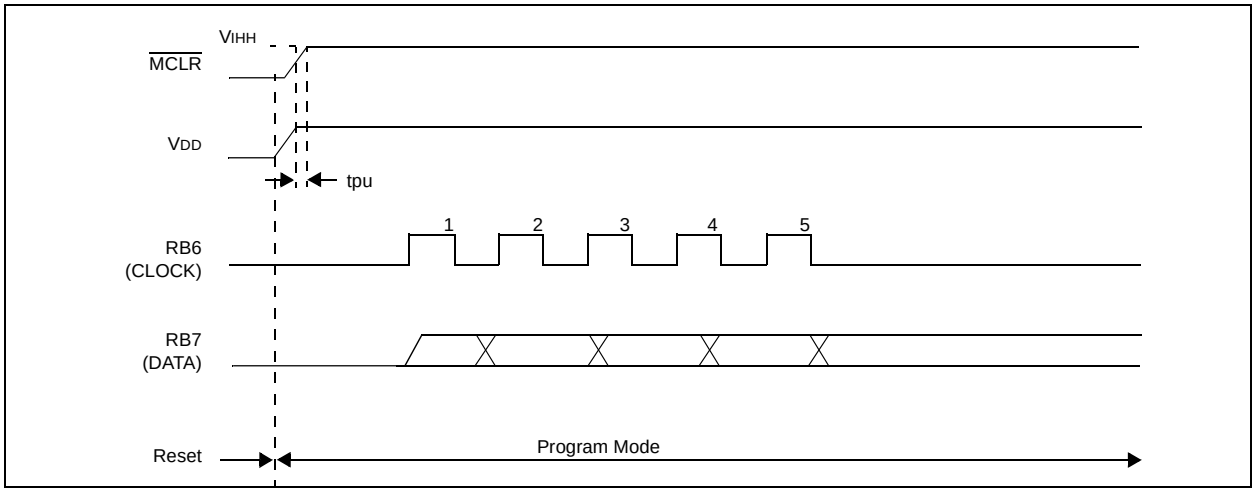


FIGURE 7-11: PROGRAM MODE ENTRY



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