TL16C750E UART with 128-Byte FIFO

1 Features

- Supports wide supply voltage range of 1.62 V to 5.5 V
  - 6 Mbps (48-MHz oscillator input clock) at 5 V and 3.3 V
  - 3 Mbps (48-MHz oscillator input clock) at 5 V and 3.3 V
  - 2 Mbps (32-MHz oscillator input clock) at 3.3 V
  - 1.5 Mbps (24-MHz oscillator input clock) at 2.5 V
  - 1 Mbps (16-MHz oscillator Input clock) at 1.8 V
- Characterized for operation from –40°C to 105°C
- 128-byte transmit or receive FIFO
- 6-bit fractional baud rate divider
- Software-selectable baud-rate generator
- Programmable and selectable transmit and Receive FIFO Trigger Levels for DMA, interrupt generation, and software or hardware flow control
- Software/Hardware flow control
  - Programmable Xon and Xoff characters with optional Xon any character
  - Programmable Auto-RTS and Auto-CTS-modem control functions (CTS, RTS, DSR, DTR, RI, and CD)
- DMA signaling capability for both received and transmitted data
- RS-485 mode support
- Infrared data association (IrDA) capability
- Programmable sleep mode
- Programmable serial interface characteristics
  - 5, 6, 7, or 8-bit characters with 1, 1.5, or 2 stop bit generation
  - Even, odd, or no parity bit generation and detection
- False start bit and line break detection
- Internal test and loopback capabilities

2 Applications

- Industrial computing
- Communications equipment
- White goods

3 Description

The TL16C750E is a single universal asynchronous receiver transmitter (UART) with 128-byte FIFOs, fractional baud rate support, automatic hardware, software flow control and data rates up to 6 Mbps. The device offers enhanced features such as fractional baud rate and a transmission character control register (TCR) that stores received FIFO threshold level to start or stop transmission during hardware and software flow control automatically without intervention from the CPU.

With the FIFO RDY register, the software gets the status of TXRDY or RXRDY, saving extra GPIO usage. On-chip status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The TL16C750E incorporates the functionality of UART, the UART having its own register set and FIFO.

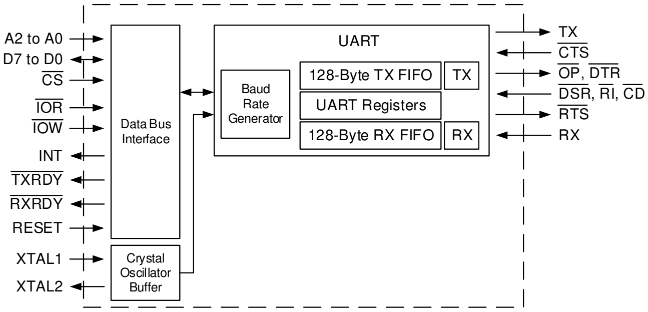
This version includes the Alternate Function Register (AFR) and this is used to enable some extra functionality beyond the capabilities of the TL16C750 version. One addition is the IrDA mode, which supports Standard IrDA (SIR) mode with baud rates from 2400 to 115.2 kbps. The third addition is support for RS-485 bus drivers or transceivers by providing an output pin (DTRx) per channel, which is timed to keep the RS-485 driver enabled as long as transmit data is pending.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL16C750E	TQFP (48)	7.00 mm × 7.00 mm

[1] For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

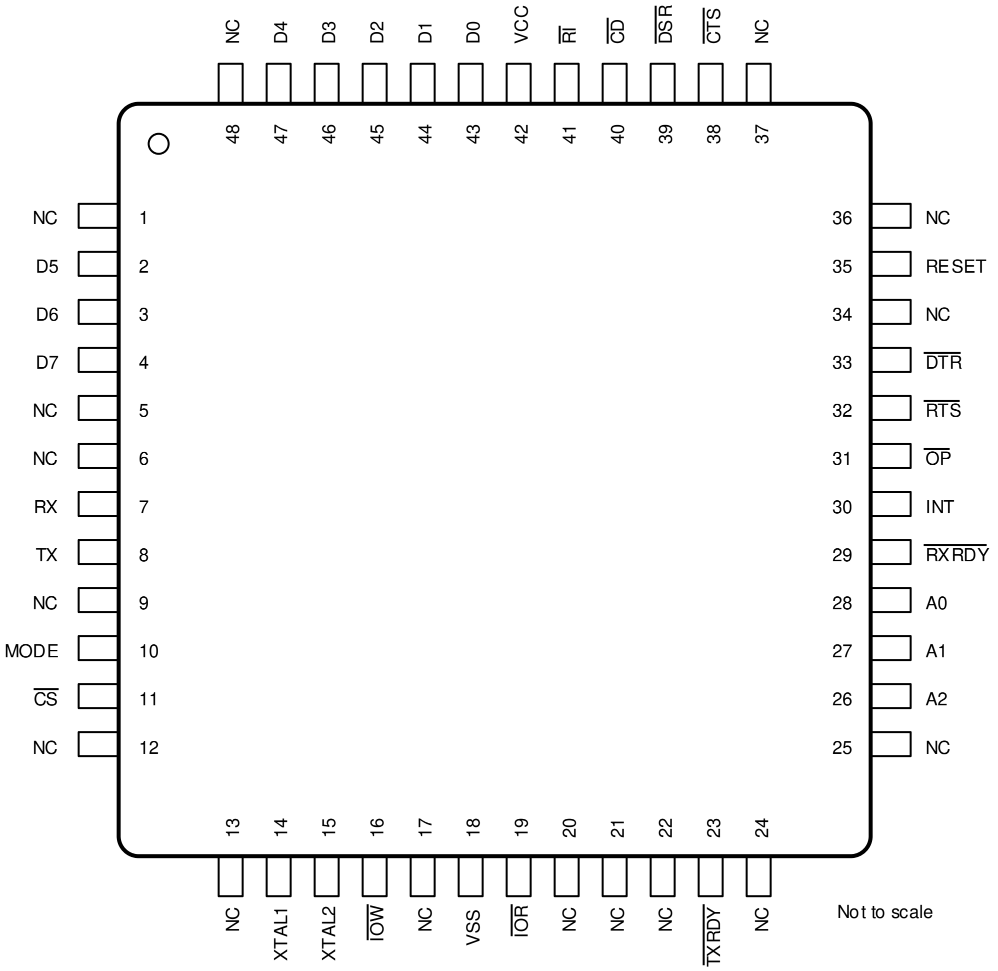
DATE	REVISION	NOTES
December 2019	*	Initial Release

5 Description (continued)

Another name for the UART function is asynchronous communications element (ACE), and these terms are used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that two such devices are incorporated into the TL16C750E device.

6 Pin Configuration and Functions

PFB Package
48-Pin TQFP
Top View



N.C. – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	28	I	Address bit 0 select. Internal registers address selection. Refer to Figure 30 for register address map.
A1	27	I	Address bit 1 select. Internal registers address selection. Refer to Figure 30 for register address map.
A2	26	I	Address bit 2 select. Internal registers address selection. Refer to Figure 30 for register address map.
CD	40	I	Carrier detect (active low). A low on these pins indicates that a carrier has been detected by the modem.
CS	11	I	Chip select. When CS is low, this input enables the ACE. When this input is high, the ACE remains inactive. When MODE is pulled low for "IOR Unused" mode, this will be pulled low and the state of IOW is read to determine if the transaction is a read or a write
CTS	38	I	Clear to send. CTS is a modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register. Bit 0 (∆CTS) of the modem status register indicates that CTS has changed states since the last read from the modem status register. If the modem status interrupt is enabled when CTS changes levels and the auto-CTS mode is not enabled, an interrupt is generated. CTS is also used in the auto-CTS mode to control the transmitter.
D0, D1, D2 D3, D4, D5, D6, D7	43, 44, 45 46, 47, 2, 3, 4	I/O	Data bus (bidirectional). These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
DSR	39	I	Data set ready. DSR is a modem status signal. Its condition can be checked by reading bit 5 (DSR) of the modem status register. Bit 1 (∆DSR) of the modem status register indicates DSR has changed levels since the last read from the modem status register. If the modem status interrupt is enabled when DSR changes levels, an interrupt is generated.
DTR	33	O	Data terminal ready. When active (low), DTR informs a modem or data set that the ACE is ready to establish communication. DTR is placed in the active level by setting the DTR bit of the modem control register. DTR is placed in the inactive level either as a result of a master reset, during loop mode operation, or clearing the DTR bit. These pins can also be used in the RS-485 mode to control an external RS-485 driver or transceiver.
MODE	10	I	Interface mode select pin. This pin must be tied to VCC or to GND. If MODE is pulled to VCC, IOR is used in communication. If MODE is pulled to GND, IOR is NOT used for communication. Only the state of IOW is sampled when CS is toggled low to determine if the transaction is a read or a write. In this mode, IOR must be connected to VCC
V$_{SS}$	18	GND	Power Reference
INT	30	O	Interrupt. When active, INT informs the CPU that the ACE has an interrupt to be serviced. Four conditions that cause an interrupt to be issued are: a receiver error, received data that is available or timed out (FIFO mode only), an empty transmitter holding register, or an enabled modem status interrupt. INT is reset (deactivated) either when the interrupt is serviced or as a result of a master reset.
IOR	19	I	Read inputs. When IOR is active (low) while the ACE is selected, the CPU is allowed to read status information or data from ACE register.
IOW	16	I	Write input (active low strobe). A valid low level on IOW transfers the contents of the data bus (D0 through D7) from the external CPU to an internal register that is defined by address bits A0 through A2.
NC	1, 5, 6, 9, 12, 13, 17, 20, 21, 22, 24, 25, 34, 36, 37, 48		No internal connection
OP	31	O	The state of this pin is defined by the user through the software settings of the MCR register, bit 3. INT is set to active mode and OP to logic 0 when the MCR-3 is set to logic 1. INT is set to the 3-state mode and OP to a logic 1 when MCR-3 is set to a logic 0
RESET	35	I	Reset. RESET resets the internal registers and all the outputs. The UART transmitter output and the receiver input are disabled during reset time.
RI	41	I	Ring indicator. RI is a modem status signal. Its condition can be checked by reading bit 6 (RI) of the modem status register. Bit 2 (TERI) of the modem status register indicates that RI has transitioned from a low to a high level since the last read from the modem status register. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
RTS	32	O	Request to send. When active, RTS informs the modem or data set that the ACE is ready to receive data. RTS is set to the active level by setting the RTS modem control register bit and is set to the inactive (high) level either as a result of a master reset or during loop mode operations or by clearing bit 1 (RTS) of the MCR. In the auto-RTS mode, RTS is set to the inactive level by the receiver threshold control logic
RX	7	I	Receive data input. During the local loopback mode, this RX input pin is disabled and TX data is internally connected to the UART RX input internally. During normal mode, RX should be held high when no data is being received. This input also can be used in IrDA mode. For more information, see *IrDA Overview*.
RXRDY	29	O	Receive ready (active low). RXRDY goes low when the trigger level has been reached or a timeout interrupt occurs. It go high when the RX FIFO is empty or there is an error in RX FIFO.
TX	8	O	Transmit data. This output is associated with serial transmit data from the TL16C750E device. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input.
TXRDY	23	O	Transmit ready (active low). TXRDY goes low when there are a trigger level number of spaces available. They go high when the TX buffer is full.
V$_{CC}$	42	PWR	Power supply inputs

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
XTAL1	14	I	Crystal or external clock input. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 27). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	15	O	Output of the crystal oscillator or buffered clock. See also XTAL1. XTAL2 is used as a crystal oscillator output or buffered clock output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	6	V
V_I	Input voltage	–0.5	V_{CC} + 0.5	V
V_O	Output voltage	–0.5	V_{CC} + 0.5	V
T_A	Operating free-air temperature	–40	105	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC} = 1.8 V ±10%						
V_{CC}	Supply voltage		1.62	1.8	1.98	V
V_I	Input voltage		–0.3		0.9 × V_{CC}	V
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.4	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			–0.5	mA
I_{OL}	Low-level output current	All outputs			1	mA
	Oscillator/clock speed				16	MHz
T_A	Operating free-air temperature		-40		105	℃
V_{CC} = 2.5 V ±10%						
V_{CC}	Supply voltage		2.25	2.5	2.75	V
V_I	Input voltage		–0.3		0.9 × V_{CC}	V
V_{IH}	High-level input voltage		1.8			V
V_{IL}	Low-level input voltage				0.6	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			–1	mA
I_{OL}	Low-level output current	All outputs			2	mA
	Oscillator/clock speed				24	MHz
T_A	Operating free-air temperature		-40		105	℃
V_{CC} = 3.3 V ±10%						

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_I	Input voltage		–0.3		V_{CC}	V
V_{IH}	High-level input voltage		0.7 × V_{CC}			V
V_{IL}	Low-level input voltage				0.8	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			–1.8	mA
I_{OL}	Low-level output current	All outputs			3.2	mA
	Oscillator or clock speed				48	MHz
T_A	Operating free-air temperature		-40		105	℃
V_{CC} = 5 V ±10%						
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I	Input voltage		–0.3		V_{CC}	V
V_{IH}	High-level input voltage	Except XTAL1	2			V
		XTAL1	0.7 × V_{CC}			
V_{IL}	Low-level input voltage	Except XTAL1			0.8	V
		XTAL1			0.3 × V_{CC}	
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			–4	mA
I_{OL}	Low-level output current	All outputs			4	mA
	Oscillator or clock speed				48	MHz
T_A	Operating free-air temperature		-40		105	℃

7.4 Thermal Information

THERMAL METRIC[1]		PFB (TQFP)	UNIT
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC} = 1.8 V							
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA		1.3			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA				0.5	
I_I	Input current	V_{CC} = 1.98 V, V_I = 0 to 1.98 V	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 1.98 V, V_O = 0 to 1.98 V	Chip selected in write mode or chip deselect			±20	µA
I_{CC}	Supply current	V_{CC} = 1.98 V, $\overline{DSR}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V	All other inputs at 0.4 V, No load on outputs, XTAL1 at 16 MHz, Baud rate = 1 Mb/s			6	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	
C_I	Input capacitance				6	10	
C_O	Output capacitance				10	15	
V_{CC} = 2.5 V							

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA		1.8			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.5	
I_I	Input current	V_{CC} = 2.75 V, V_I = 0 to 2.75 V	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 2.75 V, V_O = 0 to 2.75 V	Chip selected in write mode or chip deselect			±20	µA
I_{CC}	Supply current	V_{CC} = 2.75 V, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V	All other inputs at 0.6 V, No load on outputs, XTAL1 at 24 MHz, Baud rate = 1.5 Mb/s			13	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	
C_I	Input capacitance				6	10	
C_O	Output capacitance				10	15	
V_{CC} = 3.3 V							
V_{OH}	High-level output voltage	I_{OH} = –1.8 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA				0.5	
I_I	Input current	V_{CC} = 3.6 V, V_I = 0 to 3.6 V	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 3.6 V, V_O = 0 to 3.6 V	Chip selected in write mode or chip deselect			±20	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, $\overline{DSR}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V	All other inputs at 0.8 V, No load on outputs, XTAL1 at 32 MHz, Baud rate = 2 Mb/s			25	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	
C_I	Input capacitance				6	10	
C_O	Output capacitance				10	15	
V_{CC} = 5 V							
V_{OH}	High-level output voltage	I_{OH} = –4 mA		4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.5	
I_I	Input current	V_{CC} = 5.5 V, V_I = 0 to 5.5 V	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 5.5 V, V_O = 0 to 5.5 V	Chip selected in write mode or chip deselect			±20	µA
I_{CC}	Supply current	V_{CC} = 5.5 V, $\overline{DSR}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V	All other inputs at 0.8 V, No load on outputs, XTAL1 at 48 MHz, Baud rate = 3 Mb/s			60	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	
C_I	Input capacitance				6	10	
C_O	Output capacitance				10	15	

7.6 Timing Requirements

T_A = -40°C to 105°C, V_{CC} = 1.8 V to 5 V ±10% (unless otherwise noted)

		LIMITS								UNIT
		1.8 V		2.5 V		3.3 V		5 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
IOR Used (MODE = VCC)										
t_{RESET}	Reset pulse width	200		200		200		200		ns
C_P	CP clock period	63		42		20		20		ns
t_{3w}	Oscillator or clock speed		16		24		48		48	MHz

Timing Requirements (continued)

T_A = -40°C to 105°C, V_{CC} = 1.8 V to 5 V ±10% (unless otherwise noted)

			LIMITS								UNIT
			1.8 V		2.5 V		3.3 V		5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{6s}	Address setup time		65		45		30		20		ns
t_{6h}	Address hold time	See Figure 2 and Figure 4	15		10		7		5		ns
t_{7w}	IOR strobe width	See Figure 2 and Figure 4	85		70		50		40		ns
t_{9w}	Read cycle delay	See Figure 4	85		70		60		50		ns
t_{12d}	Delay from IOR to data	See Figure 4		90		55		35		25	ns
t_{12h}	Data disable time			45		30		20		15	ns
t_{13w}	IOW strobe width	See Figure 2	85		70		50		40		ns
t_{15w}	Write cycle delay	See Figure 2	85		70		60		50		ns
t_{16s}	Data setup time	See Figure 2	70		50		30		20		ns
t_{16h}	Data hold time	See Figure 2	35		25		15		10		ns
t_{17d}	Delay from IOW to output	50-pF load, see Figure 6		80		50		35		25	ns
t_{18d}	Delay to set interrupt from MODEM input	50-pF load, see Figure 6		120		80		50		35	ns
t_{19d}	Delay to reset interrupt from IOR	50-pF load		100		65		40		30	ns
t_{20d}	Delay from stop to set interrupt	See Figure 8		1		1		1		1	baudrate
t_{21d}	Delay from IOR to reset interrupt	50-pF load, see Figure 8		100		65		40		30	ns
t_{22d}	Delay from stop to interrupt	See Figure 14		1		1		1		1	baudrate
t_{23d}	Delay from initial IOW reset to transmit start	See Figure 14	8	24	8	24	8	24	8	24	baudrate
t_{24d}	Delay from IOW to reset interrupt	See Figure 14		90		60		35		25	ns
t_{25d}	Delay from stop to set RXRDY	See Figure 10 and Figure 12		1		1		1		1	baudrate
t_{26d}	Delay from IOR to reset RXRDY	See Figure 10 and Figure 12		100		65		40		30	ns
t_{27d}	Delay from IOW to set TXRDY	See Figure 16 and		80		50		35		25	ns
t_{28d}	Delay from start to reset TXRDY	See Figure 16 and		16		16		16		16	baudrate
No IOR (MODE = GND)											
t_{RESET}	Reset pulse width		200		200		200		200		ns
C_P	CP clock period		63		42		20		20		ns
t_{3w}	Oscillator or clock speed			16		24		48		48	MHz
t_{6s}	Address setup time		70		45		30		20		ns
t_{6h}	Address hold time	See Figure 3 and Figure 5	15		10		7		5		ns
t_{9w}	Read cycle delay	See Figure 5	85		70		60		50		ns
t_{12d}	Delay from CS to data	See Figure 5		95		65		40		25	ns
t_{12h}	Data disable time			45		30		20		15	ns
t_{13w}	IOW strobe width	See Figure 3	85		70		50		40		ns
t_{15w}	Write cycle delay	See Figure 3	85		70		60		50		ns
t_{16s}	Data setup time	See Figure 3	75		50		30		25		ns
t_{16h}	Data hold time	See Figure 3	80		50		35		25		ns
t_{17d}	Delay from CS to output	50-pF load, see Figure 6		80		50		35		25	ns
t_{18d}	Delay to set interrupt from MODEM input	50-pF load, see Figure 6		120		75		45		35	ns
t_{19d}	Delay to reset interrupt from CS	50-pF load		95		65		40		30	ns
t_{20d}	Delay from stop to set interrupt	See Figure 8		1		1		1		1	baudrate
t_{21d}	Delay from IOR to reset interrupt	50-pF load, see Figure 8		85		55		40		30	ns
t_{22d}	Delay from stop to interrupt	See Figure 14		1		1		1		1	baudrate
t_{23d}	Delay from initial CS reset to transmit start	See Figure 14	8	24	8	24	8	24	8	24	baudrate
t_{24d}	Delay from IOW to reset interrupt	See Figure 14		90		60		40		25	ns
t_{25d}	Delay from stop to set RXRDY	See Figure 10 and Figure 12		1		1		1		1	baudrate
t_{26d}	Delay from CS to reset RXRDY	See Figure 10 and Figure 12		95		60		35		25	ns

Timing Requirements (continued)

T_A = -40°C to 105°C, V_{CC} = 1.8 V to 5 V ±10% (unless otherwise noted)

			LIMITS								UNIT
			1.8 V		2.5 V		3.3 V		5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{27d}	Delay from CS to set TXRDY	See Figure 16 and		80		50		35		25	ns
t_{28d}	Delay from start to reset TXRDY	See Figure 16 and		16		16		16		16	baudrate
t_{29h}	IOW hold time to CS	See Figure 3 and Figure 5	15		10		7		5		ns
t_{29s}	IOW setup time to CS	See Figure 3 and Figure 5	70		50		30		20		ns

7.7 Typical Characteristics

Tested as per electrical characteristics table

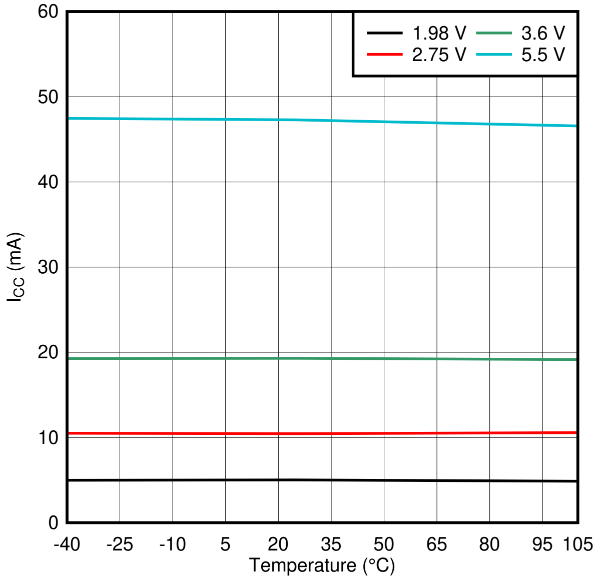


Figure 1. I_{CC} vs Temperature

8 Parameter Measurement Information

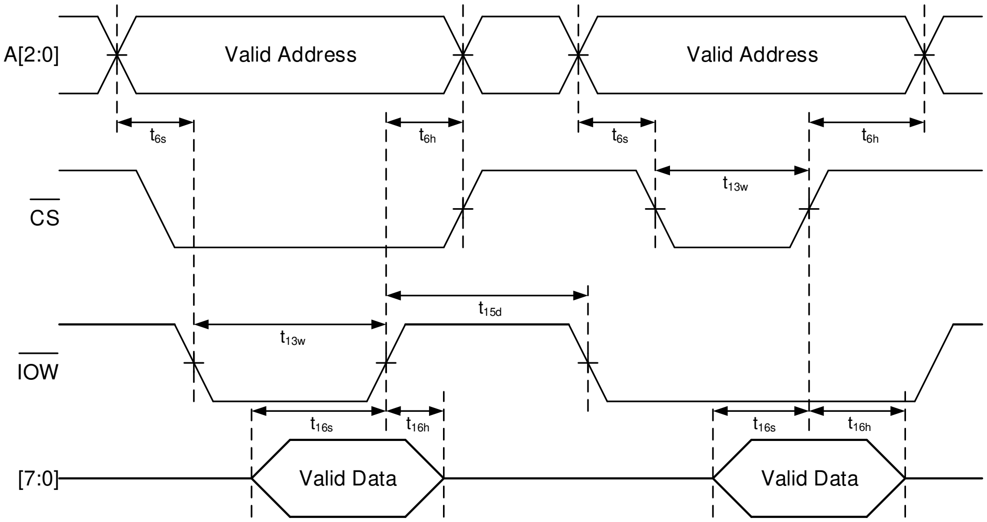


Figure 2. General Write Timing ($\overline{IOR}$ and $\overline{IOW}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

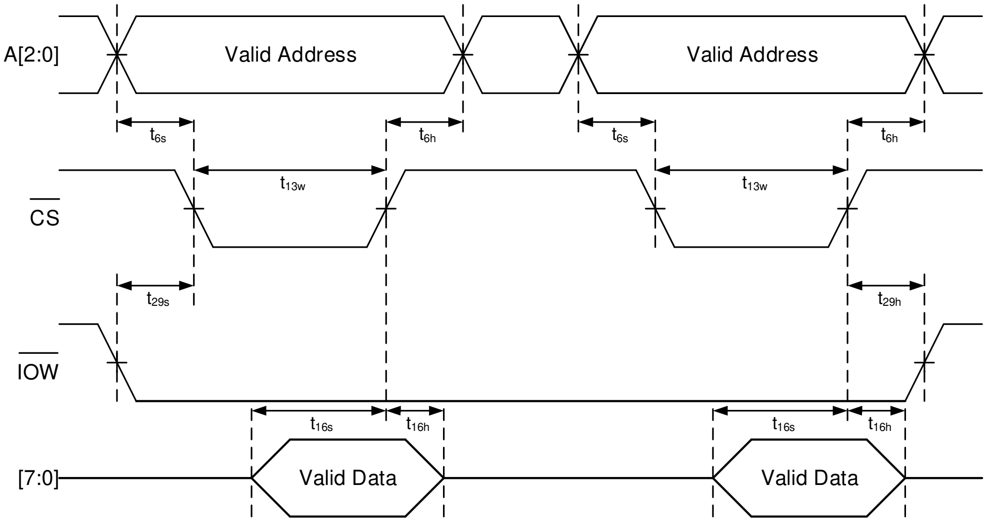


Figure 3. General Write Timing ($\overline{\text{IOW}}$ Only Mode, MODE = GND)

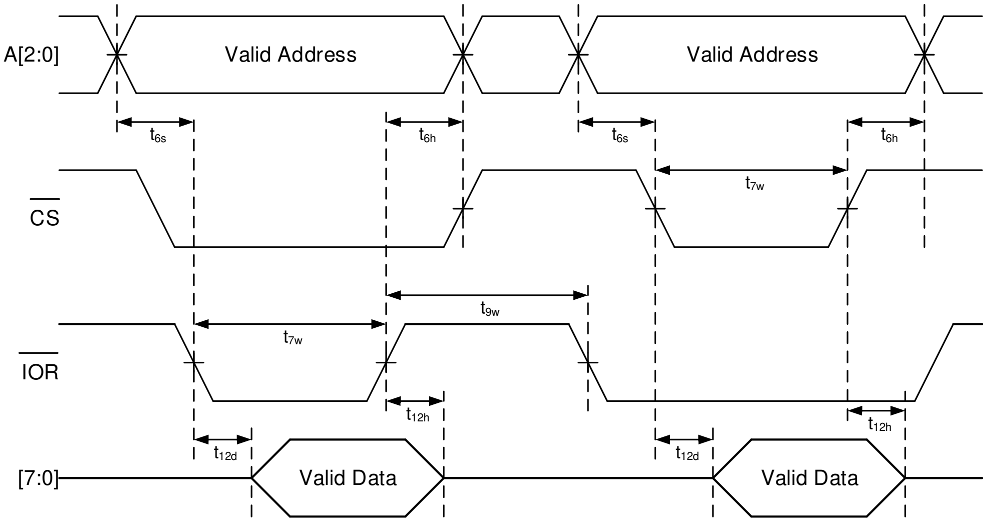


Figure 4. General Read Timing ($\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

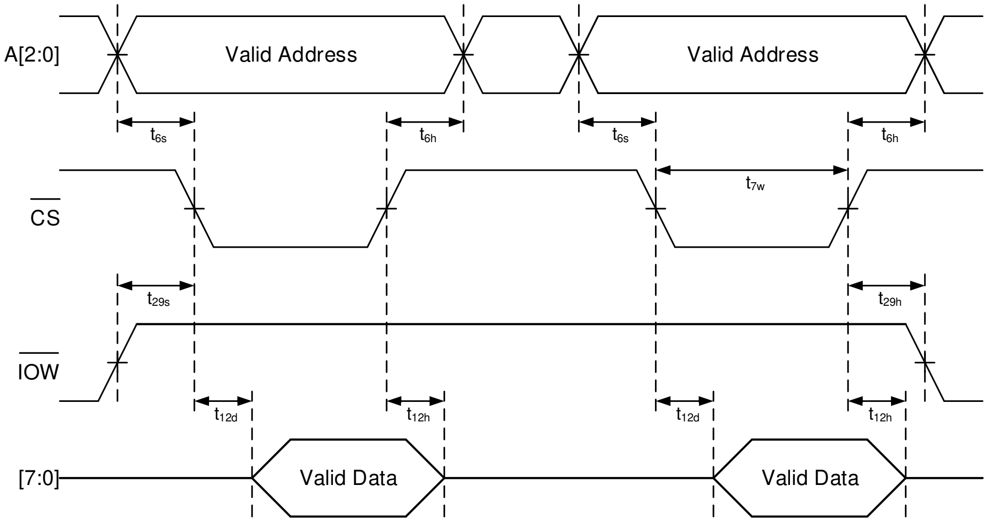


Figure 5. General Read Timing ($\overline{IOW}$ Only Mode, MODE = GND)

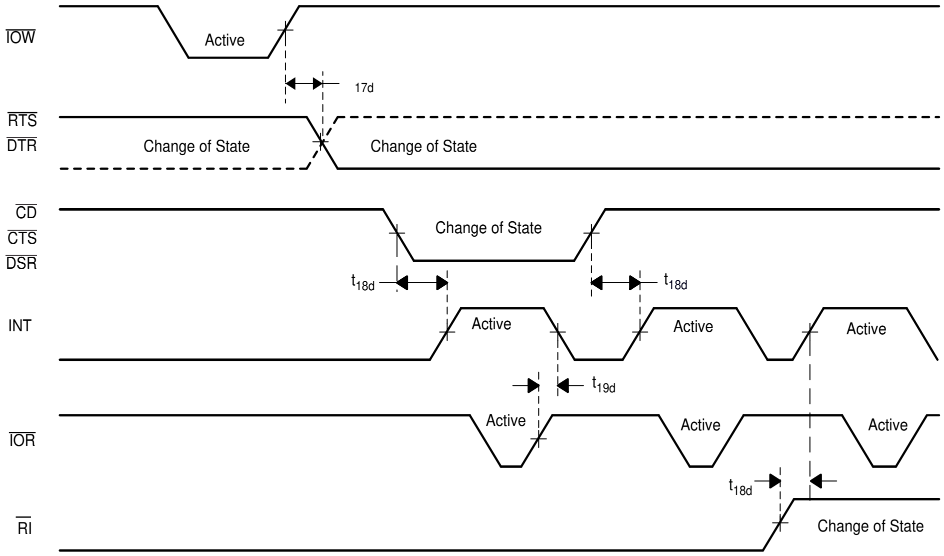


Figure 6. Modem or Output Timing ($\overline{IOR}$ and $\overline{IOW}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

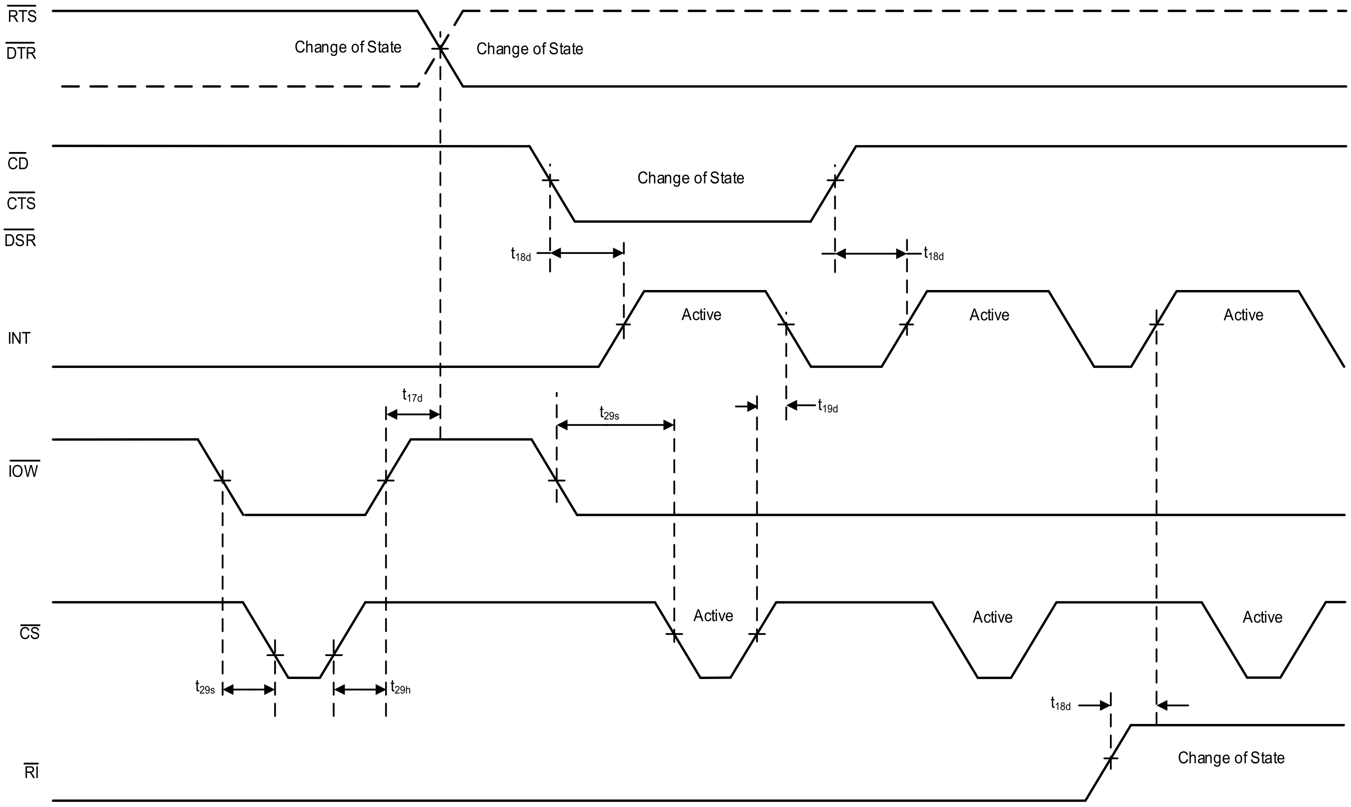


Figure 7. Modem or Output Timing (IOW Only Mode, MODE = GND)

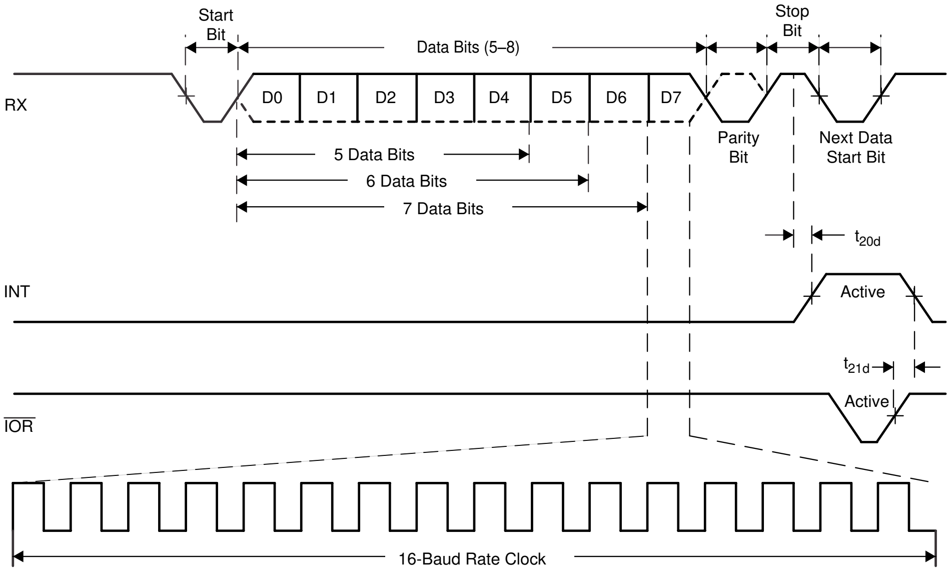


Figure 8. Receive Timing (IOR and IOW Mode, MODE = VCC)

Parameter Measurement Information (continued)

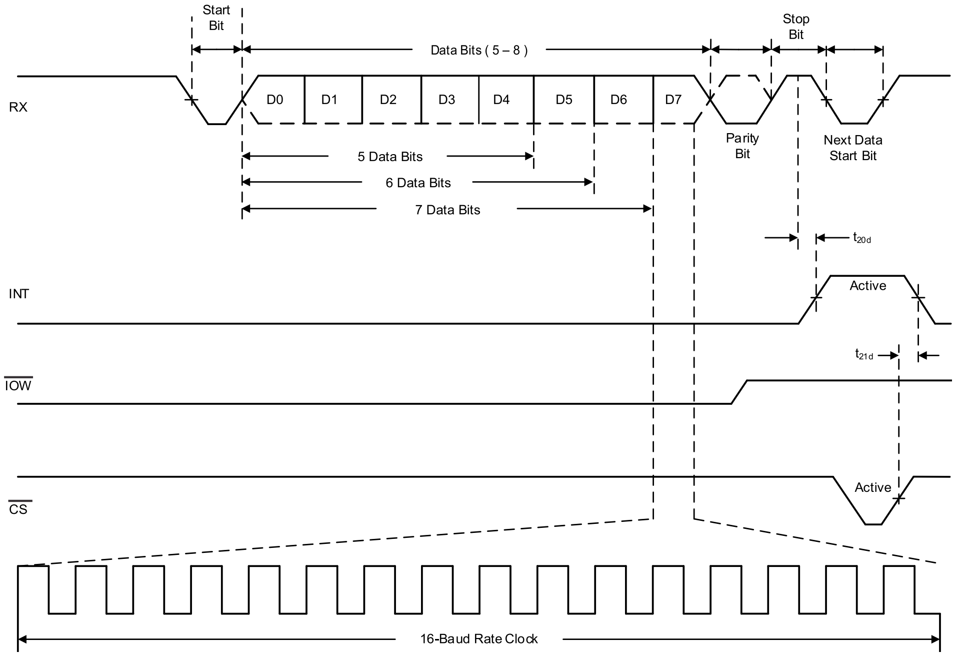


Figure 9. Receive Timing ($\overline{\text{IOW}}$ Only Mode, MODE = GND)

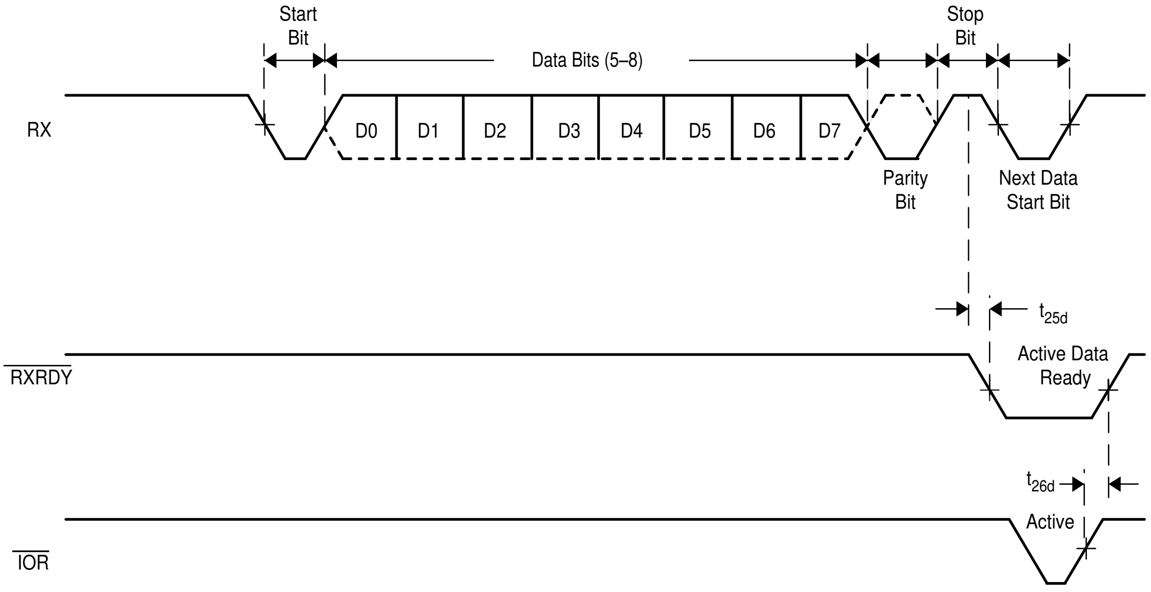


Figure 10. Receive Ready Timing in Non-FIFO Mode ($\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

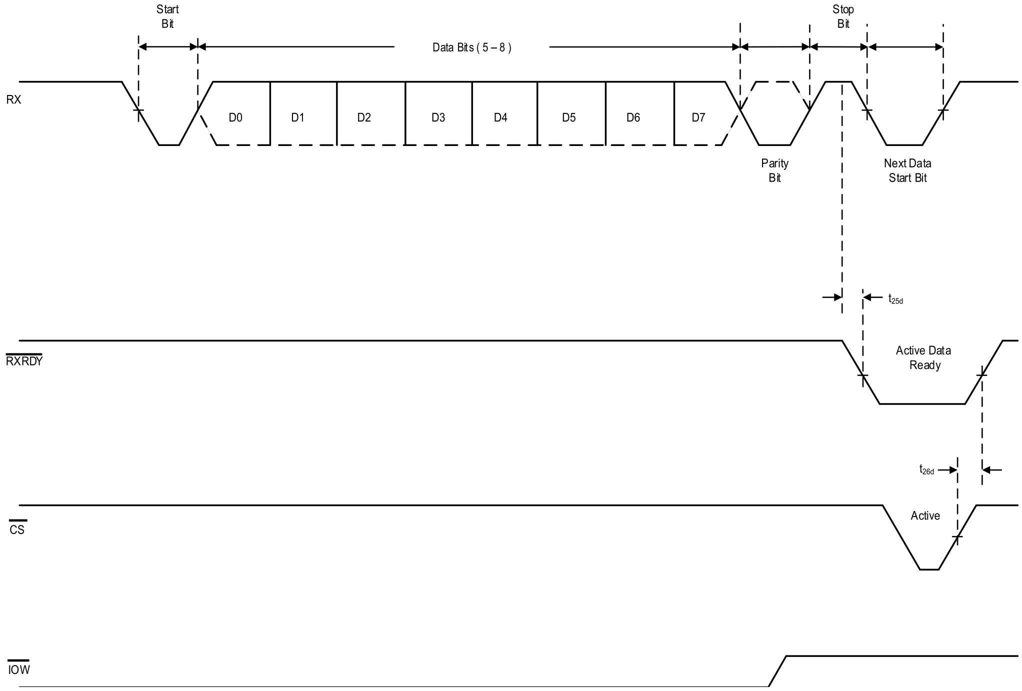


Figure 11. Receive Ready Timing in Non-FIFO Mode ($\overline{IOW}$ Only Mode, MODE = GND)

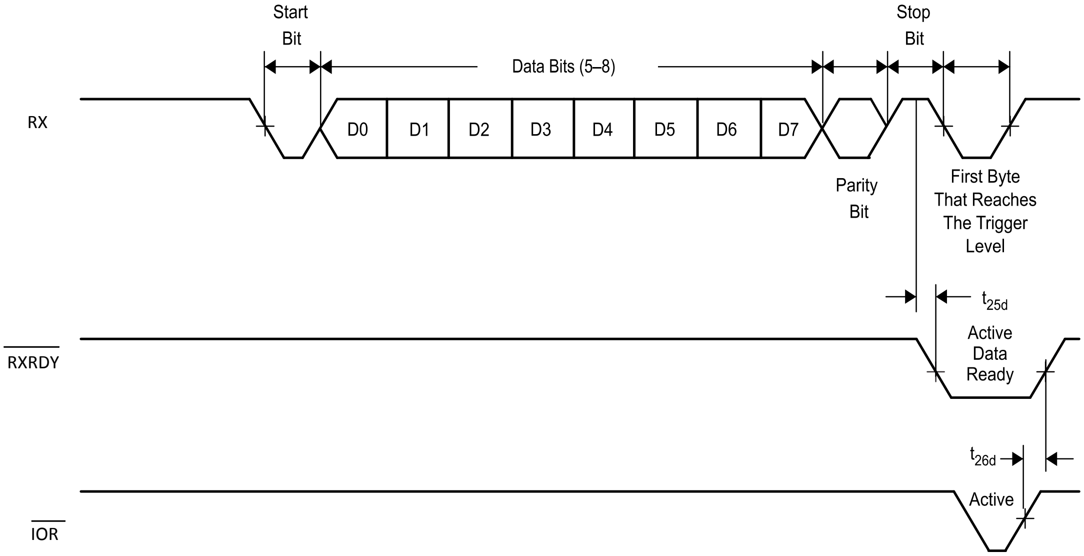


Figure 12. Receive Timing in FIFO Mode ($\overline{IOR}$ and $\overline{IOW}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

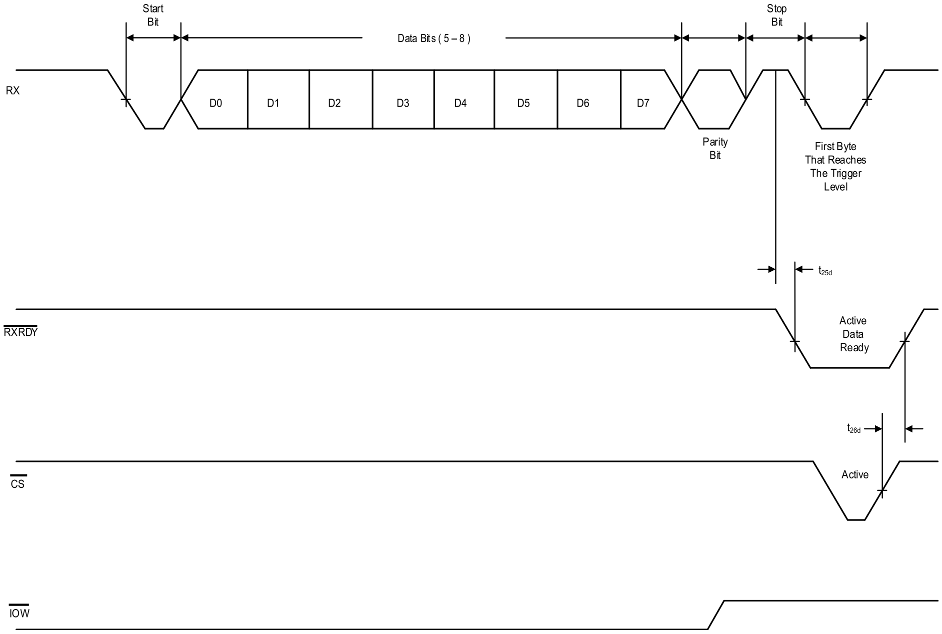


Figure 13. Receive Timing in FIFO Mode ($\overline{\text{IOW}}$ Only Mode, MODE = GND)

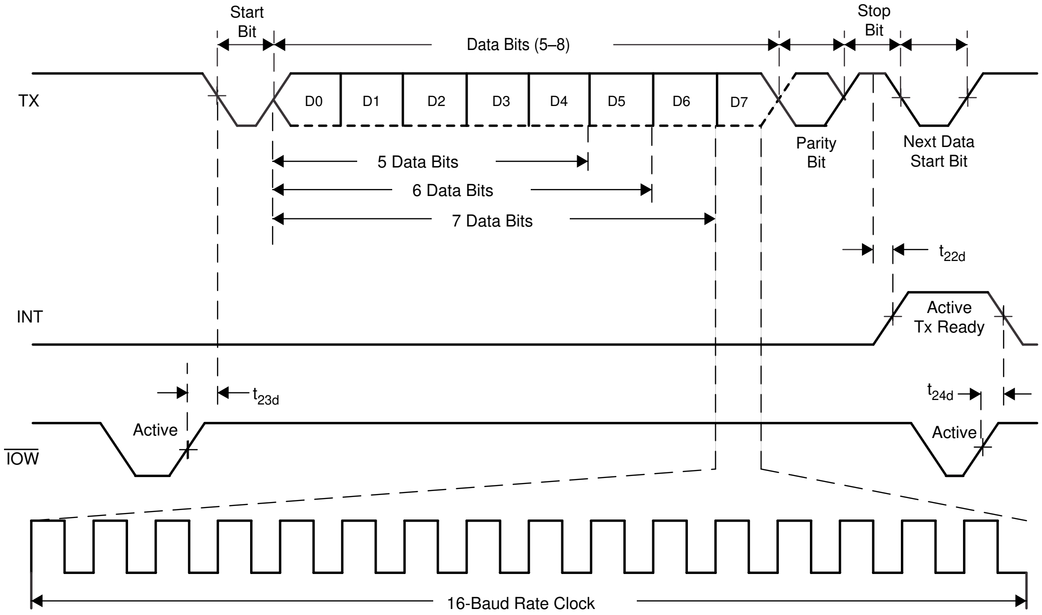


Figure 14. Transmit Timing ($\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

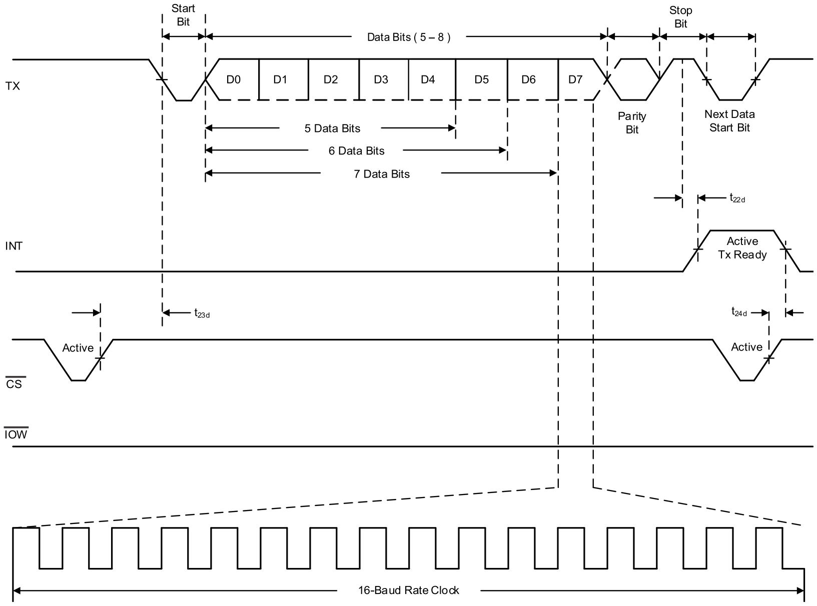


Figure 15. Transmit Timing ($\overline{\text{IOW}}$ Only Mode, MODE = GND)

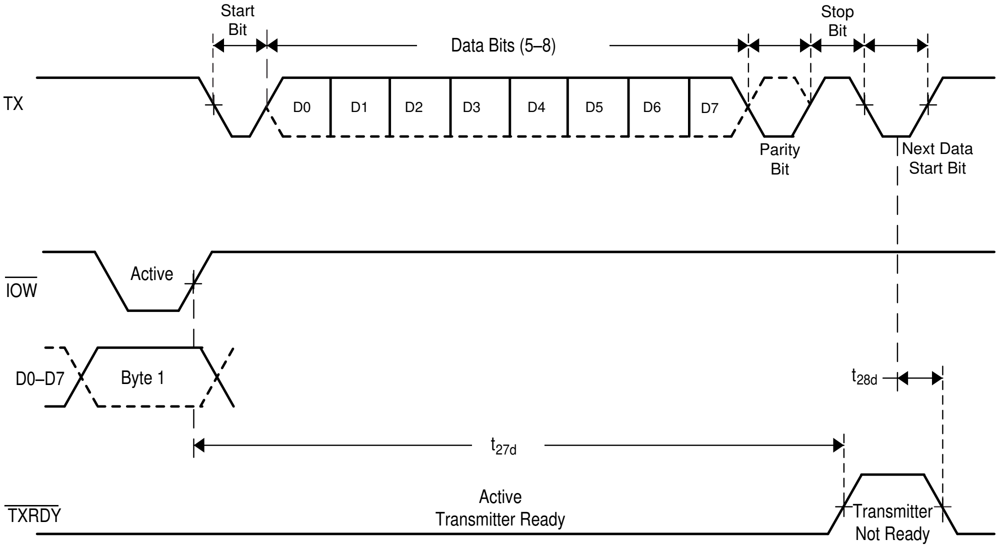


Figure 16. Transmit Ready Timing in Non-FIFO Mode ($\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ Mode, MODE = VCC)

Parameter Measurement Information (continued)

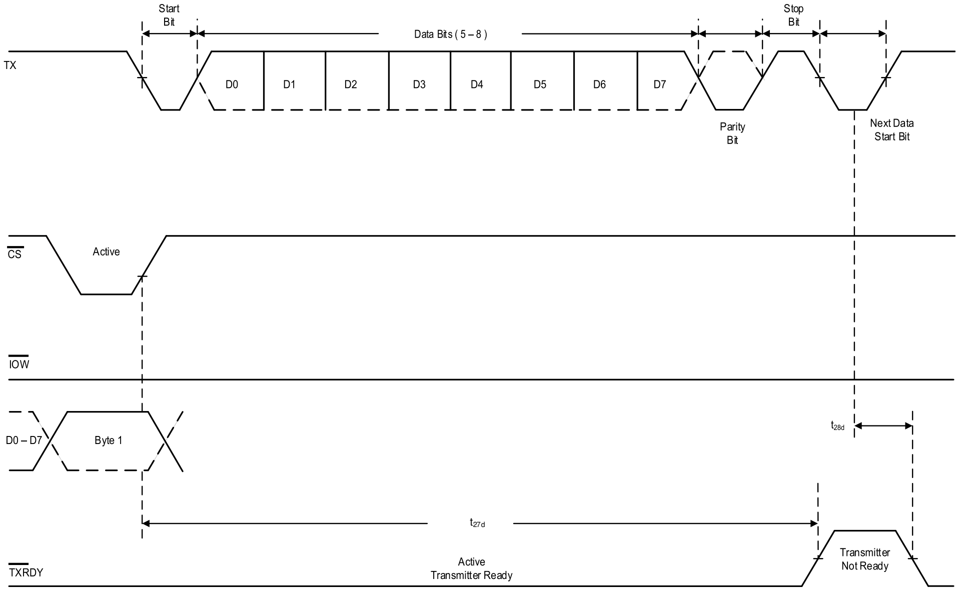


Figure 17. Transmit Ready Timing in Non-FIFO Mode ($\overline{\text{IOW}}$ Only Mode, MODE = GND)

9 Detailed Description

9.1 Overview

The TL16C750E UART is pin-compatible with the TL16C550D UART in the PFB package. It provides more enhanced features. All additional features are provided through a special enhanced features register.

The TL16C750E UART performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-parallel conversion on data characters transmitted by the processor. The complete status of the TL16C750E UART can be read at any time during functional operation by the processor.

The UART transmits data sent to it from the peripheral 8-bit bus on the TX signal and receives characters on the RX signal. Characters can be programmed to be 5, 6, 7, or 8 bits. The UART has a 128-byte receive FIFO and transmit FIFO and can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate based upon a programmable divisor and its input clock. It can transmit even, odd, or no parity and 1-, 1.5-, or 2-stop bits. The receiver can detect break, idle or framing errors, FIFO overflow, and parity errors. The transmitter can detect FIFO underflow. The UART also contains a software interface for modem control operations, software flow control and hardware flow control capabilities.

9.2 Functional Block Diagrams

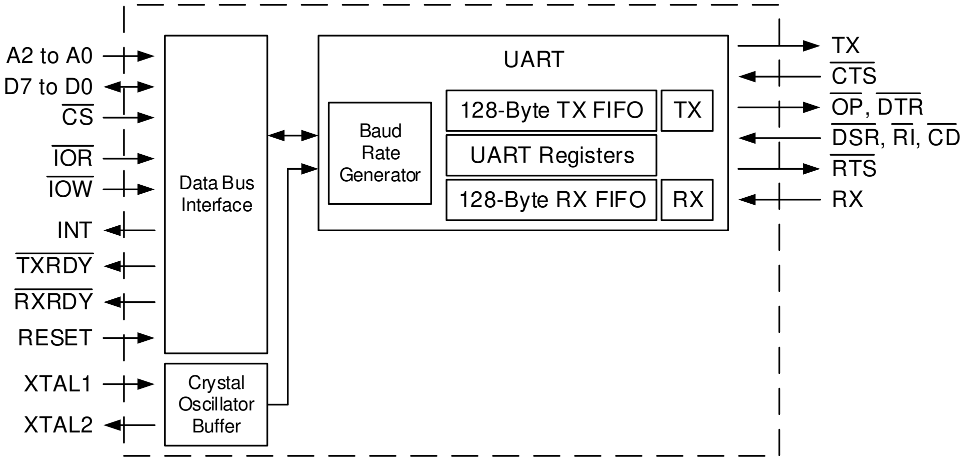
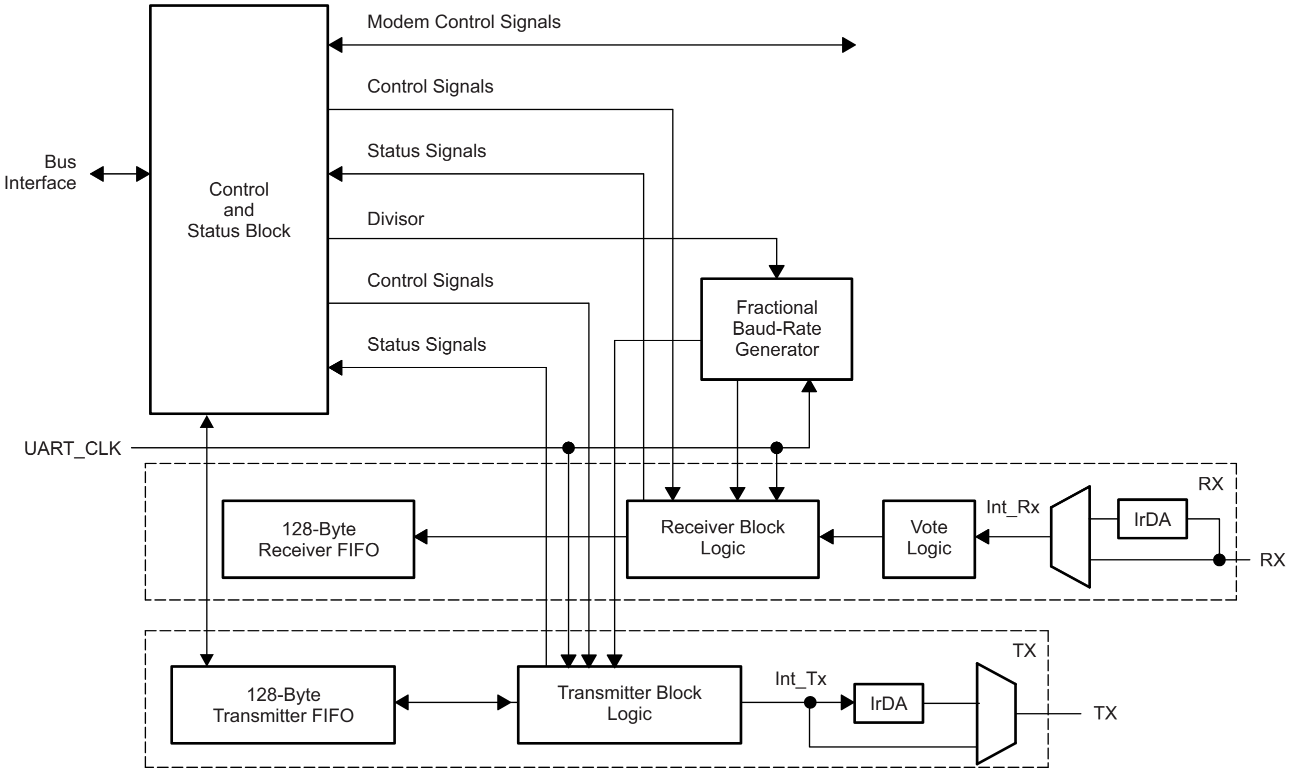


Figure 18. TL16C750E Functional Block Diagram

Functional Block Diagrams (continued)



NOTE: The vote logic determines whether the RX data is a logic 1 or 0. It takes three samples of the RX line and uses a majority vote to determine the logic level received. The vote logic operates on all bits received.

Figure 19. TL16C750E Functional Block Diagram – Control Blocks

9.3 Feature Description

9.3.1 UART Modes

The TL16C750E UART can be placed in an alternate mode (FIFO mode) relieving the processor of excessive software overhead by buffering received and transmitted characters.

The TL16C750E UART has selectable hardware flow control and software flow control. Both schemes significantly reduce software overhead and increase system efficiency by automatically controlling serial data flow. Hardware flow control uses the $\overline{\text{RTS}}$ output and $\overline{\text{CTS}}$ input signals. Software flow control uses programmable Xon and Xoff characters.

9.3.2 Trigger Levels

The TL16C750E UART provides independent selectable and programmable trigger levels for both receiver and transmitter DMA and interrupt generation. After reset, both transmitter and receiver FIFOs are disabled and so, in effect, the trigger level is the default value of one byte. The selectable trigger levels are available through the FCR. The programmable trigger levels are available through the TLR.

Both the receiver and transmitter FIFOs can store up to 128 bytes (including three additional bits of error status per byte for the receiver FIFO) and have selectable or programmable trigger levels. Primary outputs $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ allow signaling of DMA transfers.

Feature Description (continued)

NOTE

When writing data into the transmit FIFO, the transmission starts immediately, which shifts the first element out of the FIFO. Depending on the speed of the processor, it may be possible to get a pulse on the $\overline{\text{TXRDY}}$ pin, since the level falls below the trigger threshold.

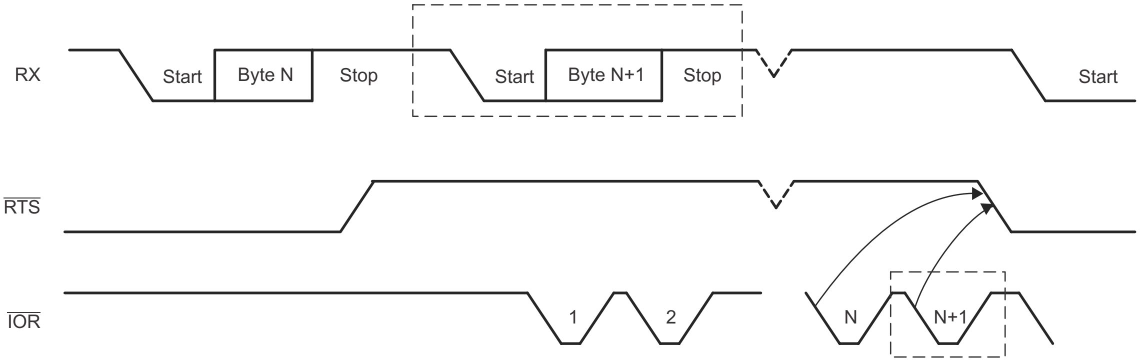
9.3.3 Hardware Flow Control

Hardware flow control is composed of auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$. Auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ can be enabled or disabled independently by programming EFR[7:6].

With auto-$\overline{\text{CTS}}$, $\overline{\text{CTS}}$ must be active before the UART can transmit data. Auto-$\overline{\text{RTS}}$ only activates the $\overline{\text{RTS}}$ output when there is enough room in the FIFO to receive data and deactivates the $\overline{\text{RTS}}$ output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the TCR determine the levels at which $\overline{\text{RTS}}$ is activated or deactivated. If both auto-$\overline{\text{CTS}}$ and auto-$\overline{\text{RTS}}$ are enabled, when $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$, data transmission does not occur unless the receiver FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If not enabled, overrun errors occur if the transmit data rate exceeds the receive FIFO servicing latency.

9.3.4 Auto-$\overline{\text{RTS}}$

Auto-$\overline{\text{RTS}}$ data flow control originates in the receiver block (see Figure 18). Figure 20 shows $\overline{\text{RTS}}$ functional timing. The receiver FIFO trigger levels used in Auto-$\overline{\text{RTS}}$ are stored in the TCR. $\overline{\text{RTS}}$ is active if the RX FIFO level is below the HALT trigger level in TCR[3:0]. When the receiver FIFO HALT trigger level is reached, $\overline{\text{RTS}}$ is deasserted. The sending device (for example, another UART) may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it may not recognize the deassertion of $\overline{\text{RTS}}$ until it has begun sending the additional byte. $\overline{\text{RTS}}$ is automatically reasserted once the receiver FIFO reaches the RESUME trigger level programmed via TCR[7:4]. This reassertion allows the sending device to resume transmission.



A. N = receiver FIFO trigger level B.

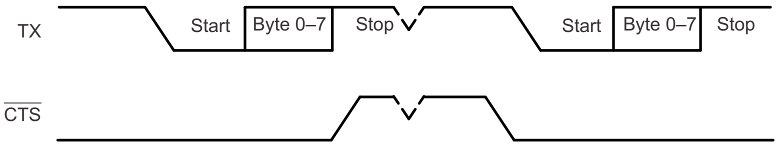
B. The two blocks in dashed lines cover the case where an additional byte is sent as described in Auto-$\overline{\text{RTS}}$.

Figure 20. $\overline{\text{RTS}}$ Functional Timing

9.3.5 Auto-$\overline{\text{CTS}}$

The transmitter circuitry checks $\overline{\text{CTS}}$ before sending the next data byte. When $\overline{\text{CTS}}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{\text{CTS}}$ must be deasserted before the middle of the last stop bit that is currently being sent. The auto-$\overline{\text{CTS}}$ function reduces interrupts to the host system. When flow control is enabled, the $\overline{\text{CTS}}$ state changes and need not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{\text{CTS}}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. Figure 21 shows $\overline{\text{CTS}}$ functional timing, and Figure 22 shows an example of autoflow control.

Feature Description (continued)



A. When $\overline{\text{CTS}}$ is low, the transmitter keeps sending serial data out.

B. When $\overline{\text{CTS}}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte, but it does not send the next byte.

C. When $\overline{\text{CTS}}$ goes from high to low, the transmitter begins sending data again.

Figure 21. $\overline{\text{CTS}}$ Functional Timing

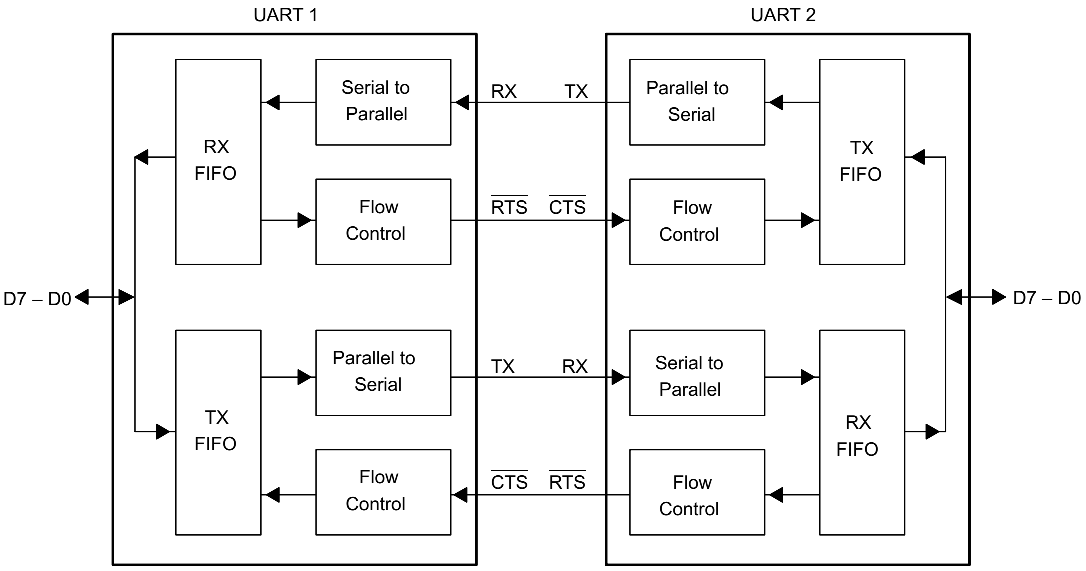


Figure 22. Autoflow Control (Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$) Example

9.3.6 Software Flow Control

Software flow control is enabled through the enhanced feature register and the modem control register. Different combinations of software flow control can be enabled by setting different combinations of EFR[3−0]. Table 1 shows software flow control options.

Two other enhanced features relate to software flow control:

- **Xon Any Function [MCR(5)**: Operation resumes after receiving any character after recognizing the Xoff character.
- **Special Character [EFR(5)]**: Incoming data is compared to Xoff2. Detection of the special character sets the Xoff interrupt [IIR(4)] but does not halt transmission. The Xoff interrupt is cleared by a read of the IIR. The special character is transferred to the RX FIFO.

NOTE

It is possible for an Xon1 character to be recognized as an Xon Any character, which could cause an Xon2 character to be written to the RX FIFO.

Table 1. Software Flow Control Options EFR[3:0]

BIT 3	BIT 2	BIT 1	BIT 0	TX, RX SOFTWARE FLOW CONTROLS
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1, Xon2: Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1, Xon2: Xoff1, Xoff2 Receiver compares Xon1 and Xon2: Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2: Xoff1 and Xoff2

When software flow control operation is enabled, the TL16C750E device compares incoming data with Xoff1 and Xoff2 programmed characters (in certain cases Xoff1 and Xoff2 must be received sequentially). [1] When an Xoff character is received, transmission is halted after completing transmission of the current character. Xoff character detection also sets IIR[4] and causes INT to go high (if enabled via IER[5]).

To resume transmission an Xon1 and Xon2 character must be received (in certain cases Xon1 and Xon2 must be received sequentially). When the correct Xon characters are received IIR[4] is cleared and the Xoff interrupt disappears.

NOTE

If a parity, framing, or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RCV FIFO.

Xoff1 and Xoff2 characters are transmitted when the RX FIFO has passed the programmed trigger level TCR[3:0].

Xon1 and Xon2 characters are transmitted when the RX FIFO reaches the trigger level programmed via TCR[7:4].

NOTE

If, after an Xoff character has been sent, software flow control is disabled, the UART transmits Xon characters automatically to enable normal transmission to proceed. A feature of the TL16C750E UART design is that if the software flow combination (EFR[3:0]) changes after an Xoff has been sent, the originally programmed Xon is automatically sent. If the RX FIFO is still above the trigger level, the newly programmed Xoff1 or Xoff2 is transmitted.

The transmission of Xoff and Xon follows the exact same protocol as transmission of an ordinary byte from the FIFO. This means that even if the word length is set to be 5, 6, or 7 characters, then the 5, 6, or 7 least significant bits of Xoff1, Xoff2 and Xon1, Xon2 are transmitted. The transmission of 5, 6, or 7 bits of a character is seldom done, but this functionality is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously. Figure 23 shows a software flow control example.

[1] When pairs of Xon and Xoff characters are programmed to occur sequentially, received Xon1 and Xoff1 characters is written to the RX FIFO if the subsequent character is not Xon2 and Xoff2.

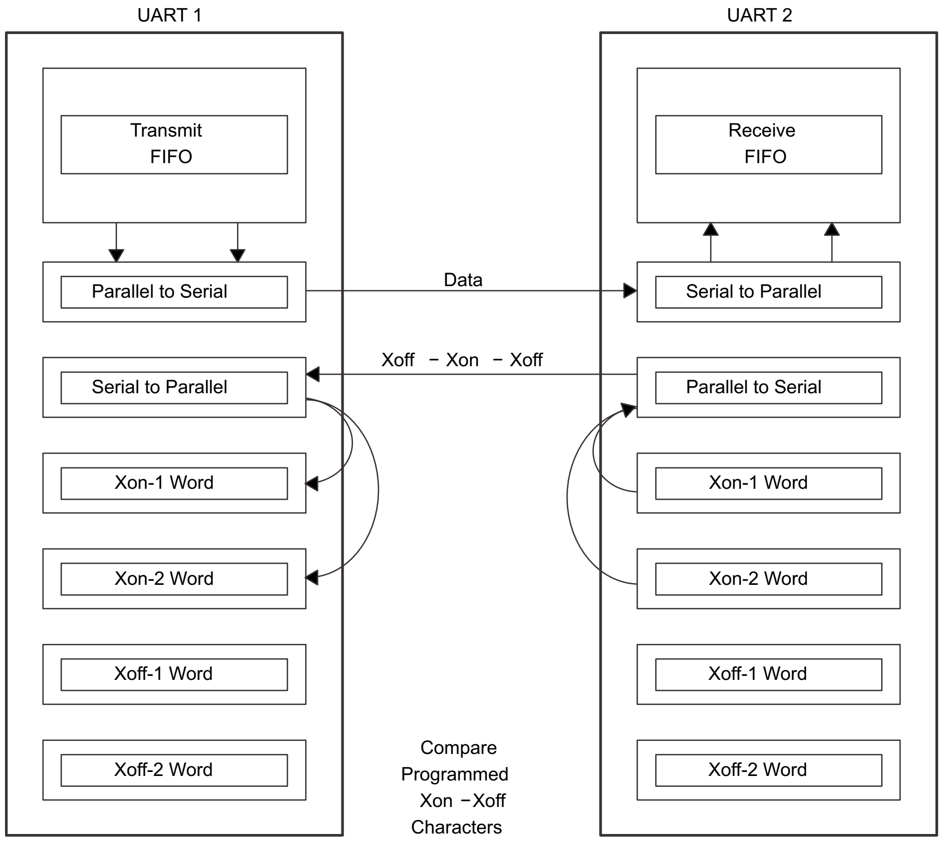


Figure 23. Software Flow Control Example

9.3.7 Software Flow Control Example

Assumptions: UART1 is transmitting a large text file to UART2. Both UARTs are using software flow control with single character Xoff (0F) and Xon (0D) tokens. Both have Xoff threshold (TCR [3:0] = 7) set to 56 and Xon threshold (TCR[7:4] = 4) set to 32. Both have the interrupt receive threshold (TLR[7:4] = 6) set to 48.

UART1 begins transmission and sends 48 characters, at which point UART2 generates an interrupt to its processor to service the RCV FIFO, but assumes the interrupt latency is fairly long. UART1 continues sending characters until a total of 56 characters have been sent. At this time UART2 transmits a 0F to UART1, informing UART1 to halt transmission. UART1 likely sends the 57th character while UART2 is sending the Xoff character. Now, UART2 is serviced and the processor reads enough data out of the RCV FIFO that the level drops to 32. UART2 now sends a 0D to UART1, informing UART1 to resume transmission.

NOTE

It is possible that there could be a glitch on the $\overline{\text{RXRDY}}$ pin when the Xoff2 character is received with a parity error. A read to the LSR register shows that bit 7 is set, due to an error in the RX FIFO.

9.3.8 Reset

Table 2 summarizes the state of outputs after reset.

Table 2. Register Reset Functions[1]

REGISTER	NAME	RESET CONTROL	RESET STATE
IER	Interrupt enable register	RESET	0x00
IIR	Interrupt identification register	RESET	0x01
FCR	FIFO control register	RESET	0x00
LCR	Line control register	RESET	0x1D
MCR	Modem control register	RESET	0x00
LSR	Line status register	RESET	0x60
MSR	Modem status register	RESET	Bits 0 to 3 cleared. Bits 4 to 7 input signals.
EFR	Enhanced feature register	RESET	0x00
RHR	Receiver holding register	RESET	Pointer logic cleared
THR	Transmitter holding register	RESET	Pointer logic cleared
TCR	Transmission control register	RESET	0x00
TLR	Trigger level register	RESET	0x00
AFR	Alternate function register	RESET	0x10

[1] Registers DLL, DLH, SPR, Xon1, Xon2, Xoff1, and Xoff2 are not reset by the top-level reset signal RESET, that is, they hold their initialization values during reset.

Table 3 summarizes the state of outputs after reset.

Table 3. Signal Reset Functions

SIGNAL	RESET CONTROL	RESET STATE
TX	RESET	High
$\overline{\text{RTS}}$	RESET	High
$\overline{\text{DTR}}$	RESET	High
$\overline{\text{RXRDY}}$	RESET	High
$\overline{\text{TXRDY}}$	RESET	Low

9.3.9 Interrupts

The TL16C750E UART has interrupt generation and prioritization (six prioritized levels of interrupts) capability. The interrupt enable register (IER) enables each of the six types of interrupts and the INT signal in response to an interrupt generation. The IER also can disable the interrupt system by clearing bits 0 to 3, 5 to 7. When an interrupt is generated, the interrupt identification register (IIR) indicates that an interrupt is pending and provides the type of interrupt through IIR[5−0]. Table 4 summarizes the interrupt control functions.

Table 4. Interrupt Control Functions

IIR[5–0]	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
000001	None	None	None	None
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO	FE < PE < BI: All erroneous characters are read from the RX FIFO. OE: Read LSR
001100	2	RX timeout	Stale data in RX FIFO	Read RHR
000100	2	RHR interrupt	DRDY (data ready) (FIFO disable) RX FIFO above trigger level (FIFO enable)	Read RHR
000010	3	THR interrupt	TFE (THR empty) (FIFO disable) TX FIFO passes above trigger level (FIFO enable)	Read IIR or a write to the THR
001000	4	Modem status	MSR[3:0] != 0	Read MSR
010000	5	Xoff interrupt	Receive Xoff character or characters/special character	Receive Xon character or characters/Read of IIR
100000	6	$\overline{\text{CTS}}$, $\overline{\text{RTS}}$	$\overline{\text{RTS}}$ pin or $\overline{\text{CTS}}$ pin change state from active (low) to inactive (high)	Read IIR

It is important to note that for the framing error, parity error, and break conditions, LSR[7] generates the interrupt. LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO. LSR[4–2] always represent the error status for the received character at the top of the RX FIFO. Reading the RX FIFO updates LSR[4–2] to the appropriate status for the new character at the top of the FIFO. If the RX FIFO is empty, then LSR[4–2] is all 0.

For the Xoff interrupt, if an Xoff flow character detection caused the interrupt, the interrupt is cleared by an Xon flow character detection. If a special character detection caused the interrupt, the interrupt is cleared by a read of the ISR.

9.3.10 Interrupt Mode Operation

In interrupt mode (if any bit of IER[3:0] is 1), the processor is informed of the status of the receiver and transmitter by an interrupt signal, INT. Therefore, it is not necessary to continuously poll the line status register (LSR) to see if any interrupt needs to be serviced. Figure 24 shows interrupt mode operation.

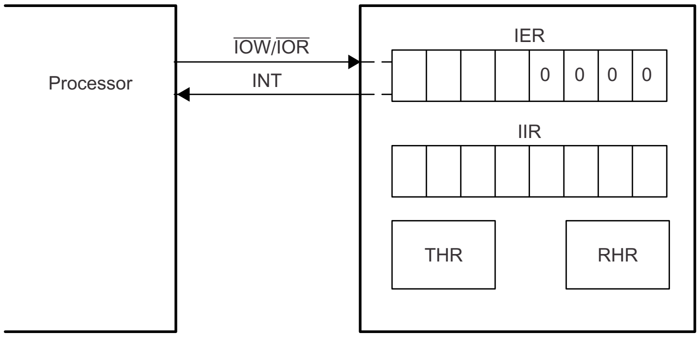


Figure 24. Interrupt Mode Operation

9.3.11 Polled Mode Operation

In polled mode (IER[3:0] = 0000), the status of the receiver and transmitter can then be checked by polling the line status register (LSR). This mode is an alternative to the interrupt mode of operation where the status of the receiver and transmitter is automatically known by means of interrupts sent to the CPU. Figure 25 shows polled mode operation.

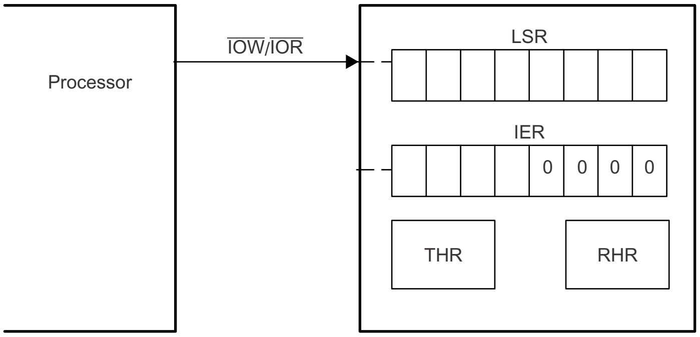


Figure 25. FIFO Polled Mode Operation

9.3.12 Break and Timeout Conditions

An RX timeout condition is detected when the receiver line, RX, has been high for a time equivalent to (4 × programmed word length) + 12 bits and there is at least one byte stored in the RX FIFO.

When a break condition occurs, the TX line is pulled low. A break condition is activated by setting LCR[6].

9.3.13 Programmable Baud Rate Generator with Fractional Divisor

The TL16C750E UART contains a programmable baud generator that divides reference clock by a divisor in the range between 1 and (2^{16} − 1) and a decimal resolution of 1/64. The output frequency of the baud rate generator is 8× or 16× the baud rate, depending on the value of DLF[7]. An additional divide-by-4 prescaler is also available and can be selected by MCR[7] as shown in the following. The formula for the divisor is:

$$\text{Divisor} = (\text{XTAL crystal input frequency} / \text{prescaler}) / (\text{desired baud rate} \times \text{baud divider})$$

Where 'baud divider' is either 8 or 16, depending on the value of DLF[7]. By default, DLF[7] = 0, which corresponds to a baud divider of 16 and

$$\text{Prescaler} = \begin{cases} \text{1 when MCR[7] is set to 0 after reset} \\ \text{4 when MCR[7] is set to 1 after reset} \end{cases}$$

Figure 26 shows the internal prescaler and baud rate generator circuitry.

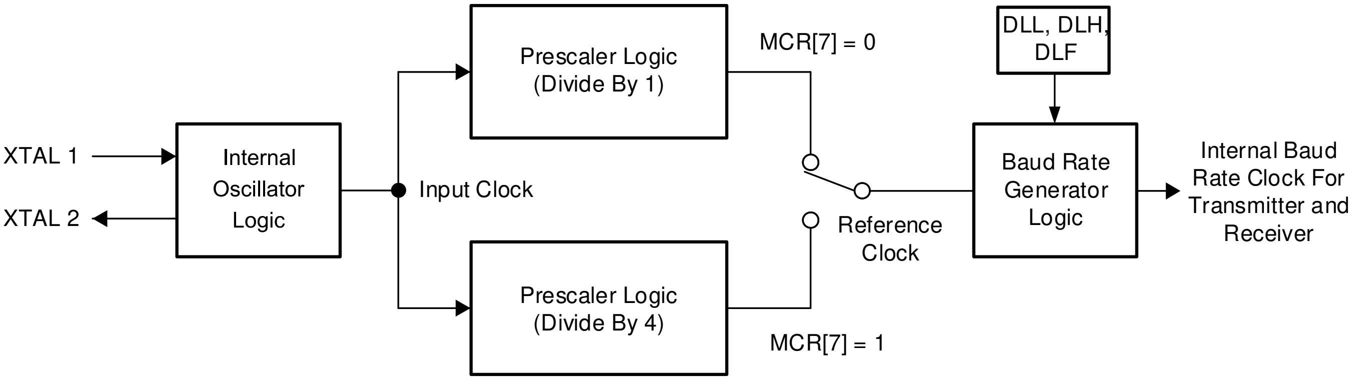

XTAL 1
XTAL 2
Internal Oscillator Logic
Input Clock
Prescaler Logic (Divide By 1)
Prescaler Logic (Divide By 4)
MCR[7] = 0
MCR[7] = 1
Reference Clock
DLL, DLH, DLF
Baud Rate Generator Logic
Internal Baud Rate Clock For Transmitter and Receiver

Figure 26. Prescaler and Baud Rate Generator Block Diagram

DLL and DLH must be written to in order to program the baud rate. DLL and DLH are the least significant and most significant byte of the baud rate divisor. If DLL and DLH are both 0, the UART is effectively disabled, because no baud clock is generated. The programmable baud rate generator is provided to select both the transmit and receive clock rates. Table 5 and Table 6 show the baud rate and divisor correlation for the crystal with frequency 1.8432 and 3.072 MHz, respectively.

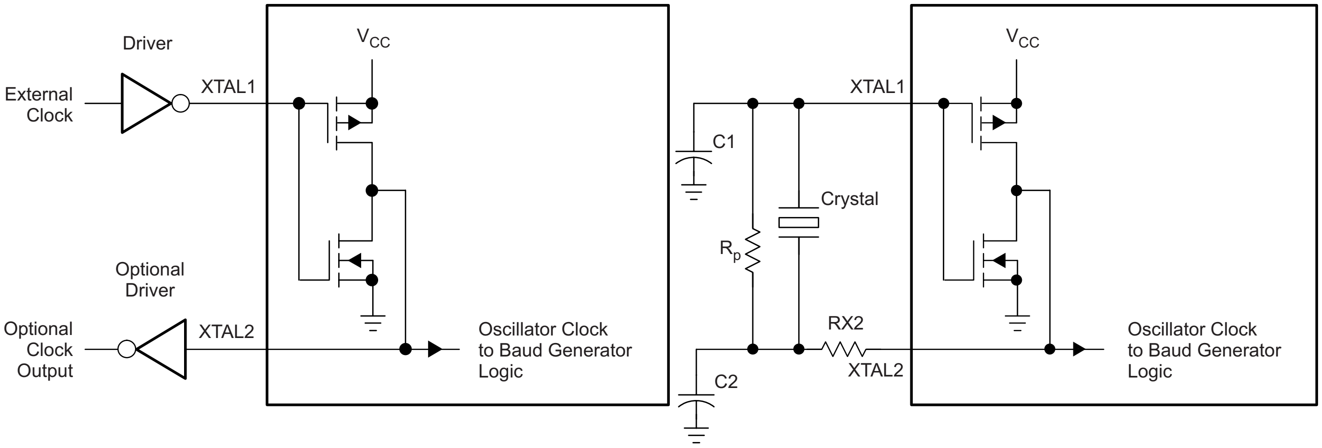
Table 5. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	0
75	1536	0
110	1047	0.026
134.5	857	0.058
150	768	0
300	384	0
600	192	0
1200	96	0
1800	64	0
2000	58	0.69
2400	48	0
3600	32	0
4800	24	0
7200	16	0
9600	12	0
19200	6	0
38400	3	0
56000	2	2.86

Table 6. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	0
75	2560	0
110	1745	0.026
134.5	1428	0.034
150	1280	0
300	640	0
600	320	0
1200	160	0
1800	107	0.312
2000	96	0
2400	80	0
3600	53	0.628
4800	40	0
7200	27	1.23
9600	20	0
19200	10	0
38400	5	0

Figure 27 shows the crystal clock circuit reference.



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A. For crystal with fundamental frequency from 1 to 24 MHz

B. For input clock frequency higher than 24 MHz, the crystal is not allowed and the oscillator must be used, because the TL16C750E internal oscillator cell can only support the crystal frequency up to 24 MHz.

Figure 27. Typical Crystal Clock Circuits

9.3.14 Fractional Divisor

The TL16C750E supports fractional divisors with a fractional resolution of 64 steps. This makes it possible to achieve many baud rates with a single crystal selection.

The following register settings must be configured to use the fractional divider:

- LCR[7] = 1
- LCR ≠ 0xBF
- EFR[4] = 1
- MCR ≠ 0bx1x0x1xx

NOTE

A 'x' denotes a do not care value of the bit.

To calculate the values necessary to put into the registers, the following functions are needed:

- TRUNC(X): Truncate X, return just the integer portion of a real number. EX: TRUNC(3.14) = 3
- ROUND(X): Round X to the nearest integer. EX: ROUND(3.1) = 3 and ROUND(3.6) = 4
- >>: Bit shift towards the right operation. EX: 0x1000 >> 8 = 0x0010. Or 0b0001 0000 0000 0000 >> 8 = 0b0000 0000 0001 0000
- &: Bitwise AND function, used to mask bits. EX: 0x1234 & 0x00FF = 0x0034 and 0x8765 & 0xFF00 = 0x8700

Calculating the required divisor is calculated by
Divisor = (XTAL crystal input frequency / prescaler) / (desired baud rate × baud divider)

Where 'baud divider' is either 8 or 16, depending on the value of DLF[7]. By default, DLF[7] = 0, which corresponds to a baud divider of 16.

Once the required divisor is found, then the register values can be calculated from
DLH = TRUNC(Divisor) >> 8
DLL = TRUNC(Divisor) & 0x00FF
DLF = ROUND((Divisor-TRUNC(Divisor)) x 128)

Table 7. Baud Rates Using a 24-MHz Crystal and a 16× Baud Divider

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	CLOSEST DIVISOR OBTAINABLE	DLH VALUE (HEX)	DLL VALUE (HEX)	DLF VALUE (HEX)	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL (%)
400	3750	3750	0x0E	0xA6	0x00	0
2400	625	625	0x02	0x71	0x00	0
4800	312.5	312 32/64	0x01	0x38	0x20	0
9600	156.25	156 16/64	0x00	0x9C	0x10	0
10000	150	150	0x00	0x96	0x00	0
19200	78.125	78 8/64	0x00	0x4E	0x08	0
25000	60	60	0x00	0x3C	0x00	0
28800	52.0833	52 5/64	0x00	0x34	0x05	0.01
38400	39.0625	39 4/64	0x00	0x27	0x04	0
50000	30	30	0x00	0x1E	0x00	0
57600	26.0417	26 3/64	0x00	0x1A	0x03	0.02
75000	20	20	0x00	0x14	0x00	0
100000	15	15	0x00	0x0F	0x00	0
115200	13.0208	13 1/64	0x00	0x0D	0x01	0.04
153600	9.7656	9 49/64	0x00	0x09	0x31	0
200000	7.5	7 32/64	0x00	0x07	0x20	0
225000	6.6667	6 43/64	0x00	0x06	0x2B	0.08
230400	6.5104	6 33/64	0x00	0x06	0x21	0.08
250000	6	6	0x00	0x06	0x00	0
300000	5	5	0x00	0x05	0x00	0
400000	3.75	3 48/64	0x00	0x03	0x30	0
460800	3.2552	3 16/64	0x00	0x03	0x10	0.16
500000	3	3	0x00	0x03	0x00	0
750000	2	2	0x00	0x02	0x00	0
921600	1.6276	1 40/64	0x00	0x01	0x28	0.16
1000000	1.5	1 32/64	0x00	0x01	0x20	0

9.4 Device Functional Modes

9.4.1 Device Interface Mode

There are 2 options for the interface between the processor and this device. The MODE pin selects the behavior of the interface by being connected to VCC or to GND.

9.4.1.1 $\overline{\text{IOR}}$ Used (MODE = V_{CC})

When this mode is selected, both $\overline{\text{IOW}}$ and $\overline{\text{IOR}}$ are used to determine if a read or a write is occurring to the selected address. When $\overline{\text{CS}}$ is pulled low, the device is in an active state and ready for communication. $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ may then go low to start the transaction to/from the processor. If $\overline{\text{IOR}}$ is pulled low, a read is performed. If $\overline{\text{IOW}}$ is pulled low, a write is performed.

9.4.1.2 $\overline{\text{IOR}}$ Unused (MODE = GND)

When this mode is selected, only the state of $\overline{\text{IOW}}$ is used to determine if a read or a write is occurring to the selected address. When $\overline{\text{CS}}$ is pulled low, the $\overline{\text{IOW}}$ pin is sampled. If $\overline{\text{IOW}}$ is low, then a write occurs. If $\overline{\text{IOW}}$ is high, then a read occurs.

9.4.2 DMA Signaling

There are two modes of DMA operation, DMA mode 0 or 1, selected by FCR[3].

In DMA mode 0 or FIFO disable (FCR[0] = 0), DMA occurs in single character transfers. In DMA mode 1, multicharacter (or block) DMA transfers are managed to relieve the processor for longer periods of time.

9.4.2.1 Single DMA Transfers (DMA Mode 0 or FIFO Disable)

Transmitter: When empty, the $\overline{\text{TXRDY}}$ signal becomes active. $\overline{\text{TXRDY}}$ goes inactive after one character has been loaded into it.

Receiver: $\overline{\text{RXRDY}}$ is active when there is at least one character in the FIFO. It becomes inactive when the receiver is empty.

Figure 28 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode 0 or FIFO disable.

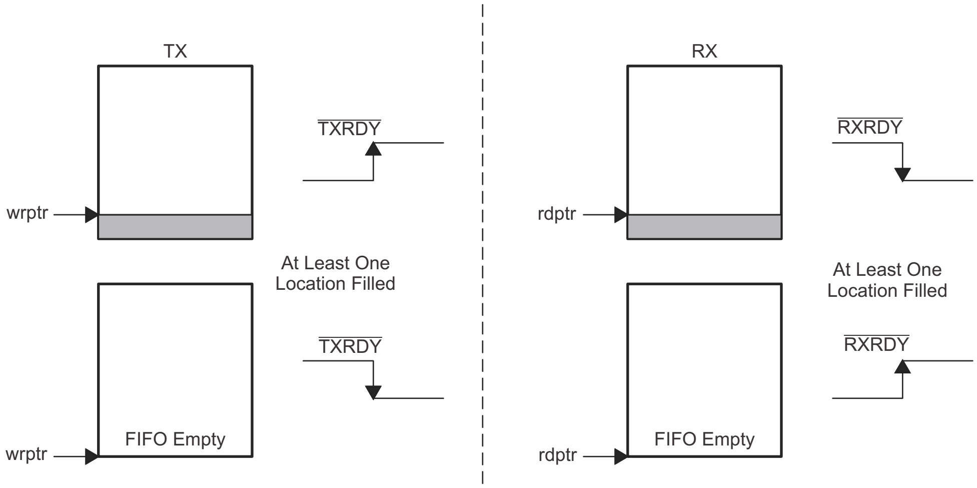

TX
$\overline{\text{TXRDY}}$
wrptr
At Least One
Location Filled
$\overline{\text{TXRDY}}$
wrptr
FIFO Empty
RX
$\overline{\text{RXRDY}}$
rdptr
At Least One
Location Filled
$\overline{\text{RXRDY}}$
rdptr
FIFO Empty

Figure 28. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 0 or FIFO Disable

9.4.2.2 Block DMA Transfers (DMA Mode 1)

Transmitter: $\overline{\text{TXRDY}}$ is active when a trigger level number of spaces are available. It becomes inactive when the FIFO is full.

Receiver: $\overline{\text{RXRDY}}$ becomes active when the trigger level has been reached or when a timeout interrupt occurs. It goes inactive when the FIFO is empty or an error in the RX FIFO is flagged by LSR(7).

Device Functional Modes (continued)

Figure 29 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode 1.

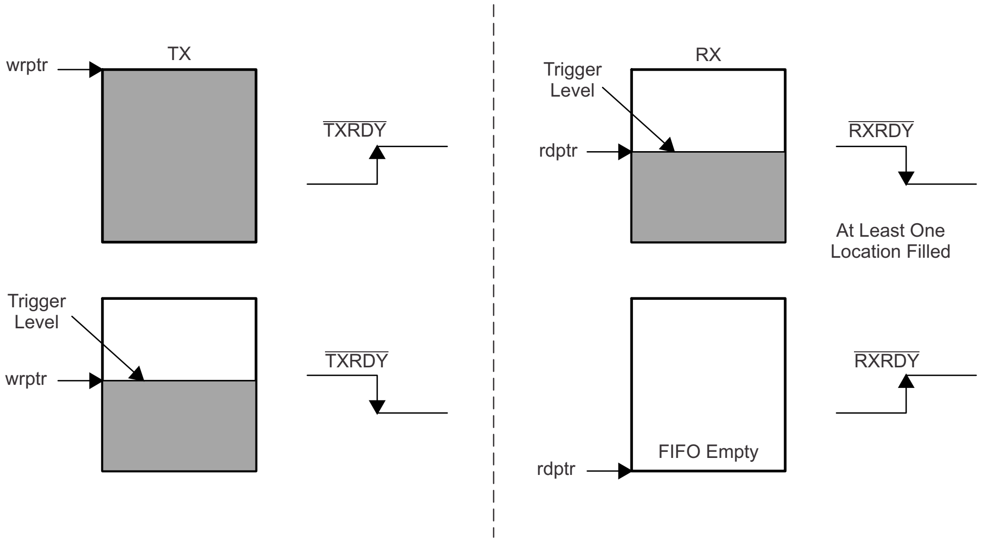

TX
wrptr
$\overline{\text{TXRDY}}$
Trigger Level
wrptr
$\overline{\text{TXRDY}}$
RX
Trigger Level
rdptr
$\overline{\text{RXRDY}}$
At Least One Location Filled
$\overline{\text{RXRDY}}$
FIFO Empty
rdptr

Figure 29. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 1

9.4.3 Sleep Mode

Sleep mode is an enhanced feature of the TL16C750E UART. It is enabled when EFR[4], the enhanced functions bit, is set and when IER[4] is set. Sleep mode is entered when:

- The serial data input line, RX, is idle (see *Break and Timeout Conditions*).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending except THR and timeout interrupts.

Sleep mode is not entered if there is data in the RX FIFO.

In sleep mode, the UART clock and baud rate clock are stopped. Because most registers are clocked using these clocks, the power consumption is greatly reduced. The UART wakes up when any change is detected on the RX line, when there is any change in the state of the modem input pins, or if data is written to the TX FIFO.

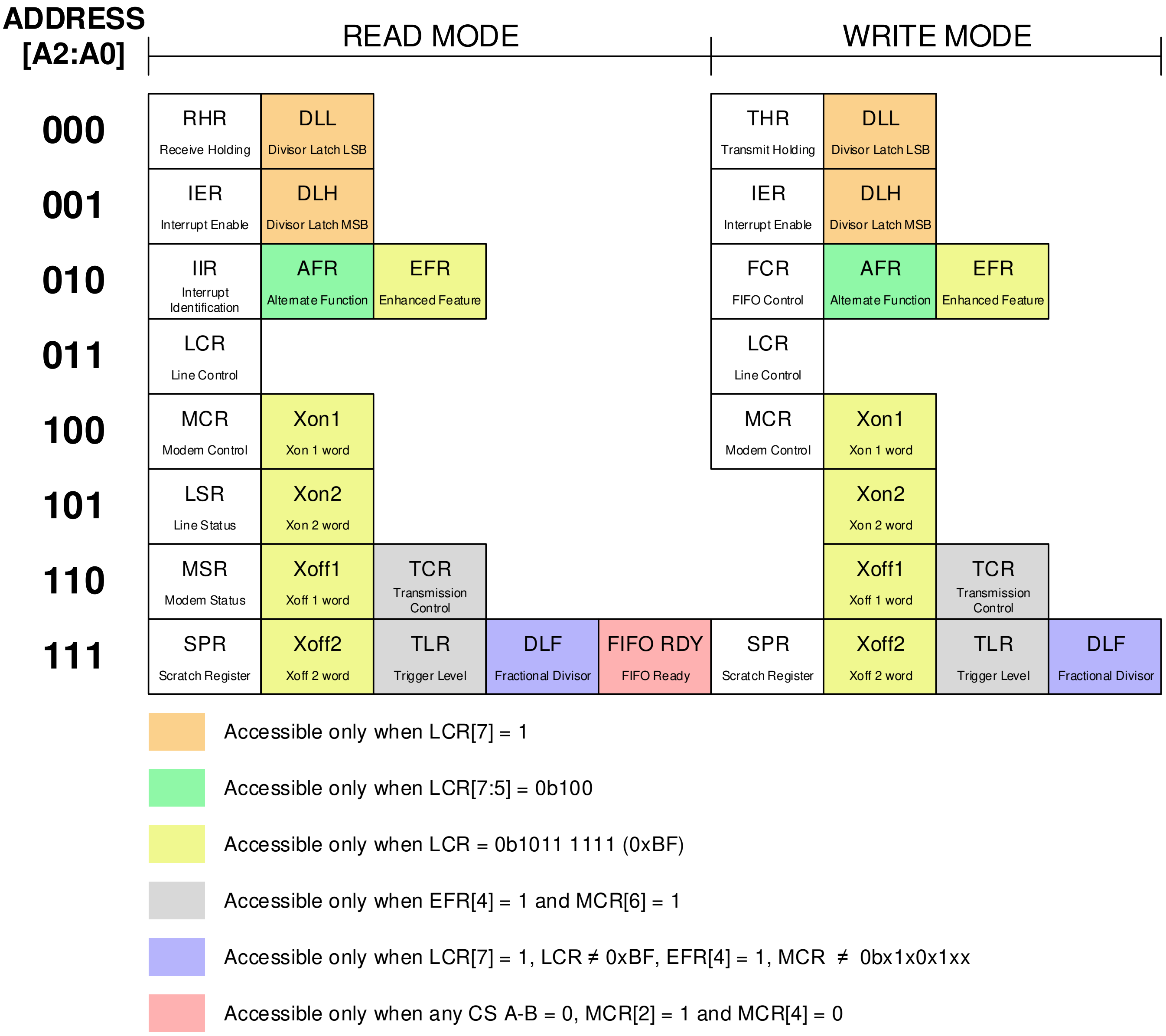
NOTE

Writing to the divisor latches, DLL and DLH, to set the baud clock, must not be done during sleep mode. Therefore, TI recommends to disable sleep mode using IER[4] before writing to DLL or DLH.

9.5 Register Maps

9.5.1 Registers Operations

Each register is selected using address lines A[0], A[1], A[2], and in some cases, bits from other registers. The programming combinations for register selection are shown in Figure 30.



ADDRESS [A2:A0]	READ MODE					WRITE MODE			
000	RHR Receive Holding	DLL Divisor Latch LSB				THR Transmit Holding	DLL Divisor Latch LSB		
001	IER Interrupt Enable	DLH Divisor Latch MSB				IER Interrupt Enable	DLH Divisor Latch MSB		
010	IIR Interrupt Identification	AFR Alternate Function	EFR Enhanced Feature			FCR FIFO Control	AFR Alternate Function	EFR Enhanced Feature	
011	LCR Line Control					LCR Line Control			
100	MCR Modem Control	Xon1 Xon 1 word				MCR Modem Control	Xon1 Xon 1 word		
101	LSR Line Status	Xon2 Xon 2 word					Xon2 Xon 2 word		
110	MSR Modem Status	Xoff1 Xoff 1 word	TCR Transmission Control				Xoff1 Xoff 1 word	TCR Transmission Control	
111	SPR Scratch Register	Xoff2 Xoff 2 word	TLR Trigger Level	DLF Fractional Divisor	FIFO RDY FIFO Ready	SPR Scratch Register	Xoff2 Xoff 2 word	TLR Trigger Level	DLF Fractional Divisor

🟧 Accessible only when LCR[7] = 1

🟩 Accessible only when LCR[7:5] = 0b100

🟨 Accessible only when LCR = 0b1011 1111 (0xBF)

⬜ Accessible only when EFR[4] = 1 and MCR[6] = 1

🟪 Accessible only when LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1, MCR ≠ 0bx1x0x1xx

🟥 Accessible only when any CS A-B = 0, MCR[2] = 1 and MCR[4] = 0

NOTE: MCR[7:5], FCR[5:4], and IER[7:4] can only be modified when EFR[4] is set.

Figure 30. Register Map – Read and Write Properties

Table 8 lists and describes the TL16C750E internal registers.

Table 8. TL16C750E Internal Registers[1] [2]

ADDRESS [A2:A0]	REGISTER	R/W [3]	ACCESS CONSIDERATION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0 0 0	RHR	R	LCR[7] = 0	bit 7 0	bit 6 0	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
	THR	W		bit 7 0	bit 6 0	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
	DLL[4]	RW	LCR[7] = 1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0 0 1	IER	RW	LCR[7] = 0	CTS# Interrupt enable[1] 0	RTS# Interrupt enable[1] 0	Xoff Interrupt enable[1] 0	Sleep mode[1] 0	Modem status interrupt 0	RX line status interrupt 0	THR empty interrupt 0	RX data available interrupt 0
	DLH[4]	RW	LCR[7] = 1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0 1 0	IIR	R	LCR[7] = 0	FCR(0) 0	FCR(0) 0	CTS# / RTS# 0	Xoff 0	Interrupt priority bit 2 0	Interrupt priority bit 1 0	Interrupt priority bit 0 0	Interrupt status 1
	FCR	W		RX trigger level 0	RX trigger level 0	TX trigger level[1] 0	TX trigger level[1] 0	DMA mode select 0	Resets TX FIFO 0	Resets RX FIFO 0	Enable FIFOs 0
	AFR[5]	RW	LCR[7:5] = 100	DLY2 0	DLY1 0	DLY0 0	RCVEN 1	485LG 0	485EN 0	IREN 0	RES 0
	EFR[6]	RW	LCR[7:0] = 10111111	Auto CTS# 0	Auto RTS# 0	Special character detect 0	Enable enhanced functions 0	S/W flow control bit 3 0	S/W flow control bit 2 0	S/W flow control bit 1 0	S/W flow control bit 0 0
0 1 1	LCR	RW	None	DLAB & EFR enable 0	Break control bit 0	Sets parity 0	Parity type select 1	Parity enable 1	No. of stop bits 1	Word length 0	Word length 1
1 0 0	MCR	RW	LCR[7:0] ≠ 10111111	1x / 4x clock[1] 0	TCR & TLR enable[1] 0	Xon any[1] 0	Enable loopback 0	INT enable 0	FIFORDY enable 0	RTS# 0	DTR# 0
	Xon1[6]	RW	LCR[7:0] = 10111111	bit 7 1	bit 6 1	bit 5 1	bit 4 1	bit 3 1	bit 2 1	bit 1 1	bit 0 1
1 0 1	LSR	R	LCR[7:0] ≠ 10111111	Error in RX FIFO 0	THR & TSR empty 1	THR empty 1	Break interrupt 0	Framing error 0	Parity error 0	Overrun error 0	Data in receiver 0
	Xon2[6]	RW	LCR[7:0] = 10111111	bit 7 1	bit 6 1	bit 5 1	bit 4 0	bit 3 1	bit 2 1	bit 1 1	bit 0 1

[1] Bits represented by the blue shaded cells can only be modified if EFR[4] is enabled, that is, if enhanced functions are enabled.
[2] For more register access information, see Figure 30.
[3] Read = R; Write = W
[4] This register is only accessible when LCR[7] = 1
[5] This register is only accessible LCR[7:5] = 100
[6] This register is only accessible when LCR = 1011 1111 (0xBF)

Table 8. TL16C750E Internal Registers[1] [2] (continued)

ADDRESS [A2:A0]	REGISTER	R/W [3]	ACCESS CONSIDERATION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1 1 0	MSR	R	LCR[7:0] ≠ 10111111 & none of the below conditions are true	CD# 1	RI# 1	DSR# 1	CTS# 1	$\overline{\text{CD\#}}$ 0	$\overline{\text{RI\#}}$ 0	$\overline{\text{DSR\#}}$ 0	$\overline{\text{CTS\#}}$ 0
	Xoff1[6]	RW	LCR[7:0] = 10111111	bit 7 1	bit 6 1	bit 5 1	bit 4 1	bit 3 1	bit 2 1	bit 1 1	bit 0 1
	TCR[7]	RW	EFR[4] = 1 & MCR[6] = 1	bit 7 0	bit 6 0	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
1 1 1	SPR	RW	LCR[7:0] ≠ 10111111 & none of the below conditions are true	bit 7 0	bit 6 0	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
	Xoff2[6]	RW	LCR[7:0] = 10111111	bit 7 1	bit 6 1	bit 5 1	bit 4 1	bit 3 1	bit 2 1	bit 1 1	bit 0 1
	TLR[7]	RW	EFR[4] = 1 & MCR[6] = 1	bit 7 0	bit 6 0	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
	DLF[8]	RW	LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1, MCR ≠ 0bx1x0 x1xx [9]	bit 7 0	bit 6 0 (Reserved, RO)	bit 5 0	bit 4 0	bit 3 0	bit 2 0	bit 1 0	bit 0 0
	FIFORdy[10]	R	MCR[4] = 0 & MCR[2] = 1	0	0	0	RX FIFO A status 0	0	0	0	TX FIFO A status 0

[7] This register is only accessible when EFR[4] = 1 and MCR[6] = 1

[8] This register is accessible when LCR[7] = 1, LCR ≠ 0xBF, EFR[4] = 1, MCR ≠ 0bx1x0 x1xx[9]

[9] A 'x' denotes a do not care for a bit value

[10] This register is accessible when any CS A-B = 0, MCR[2] = 1, and loopback MCR[4] = 0 is disabled.

9.5.2 Receiver Holding Register (RHR)

The receiver section consists of the RHR and the receiver shift register (RSR). The RHR is actually a 128-byte FIFO. The RSR receives serial data from RX terminal. The data is converted to parallel data and moved to the RHR. The receiver section is controlled by the line control register. If the FIFO is disabled, location 0 of the FIFO is used to store the characters. If overflow occurs, characters are lost. The RHR also stores the error status bits associated with each character.

9.5.3 Transmit Holding Register (THR)

The transmitter section consists of the THR and the transmitter shift register (TSR). The transmit holding register is actually a 128-byte FIFO. The THR receives data and shifts it into the TSR where it is converted to serial data and moved out on the TX terminal. If the FIFO is disabled, location 0 of the FIFO is used to store the byte. Characters are lost if overflow occurs.

9.5.4 FIFO Control Register (FCR)

This is a write-only register which is used for enabling the FIFOs, clearing the FIFOs, setting transmitter and receiver trigger levels, and selecting the type of DMA signaling. Table 9 shows FIFO control register bit settings.

Table 9. FCR Bit Settings

BIT	BIT SETTINGS
0	0 = Disable the transmit and receive FIFOs 1 = Enable the transmit and receive FIFOs
1	0 = No change 1 = Clears the receive FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.
2	0 = No change 1 = Clears the transmit FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.
3	0 = DMA mode 0 1 = DMA mode 1
5:4 (1)	Sets the trigger level for the TX FIFO: 00 – 16 spaces 01 – 32 spaces 10 – 64 spaces 11 – 120 spaces
7:6	Sets the trigger level for the RX FIFO: 00 – 1 characters 01 – 4 characters 10 – 120 characters 11 – 124 characters

(1) FCR[5−4] can be modified and enabled only when EFR[4] is set. This is because the transmit trigger level is regarded as an enhanced function.

9.5.5 Line Control Register (LCR)

This register controls the data communication format. The word length, number of stop bits, and parity type are selected by writing the appropriate bits to the LCR. Table 10 shows line control register bit settings.

Table 10. LCR Bit Settings

BIT	BIT SETTINGS
1:0	Specifies the word length to be transmitted or received 00 – 5 bits 01 – 6 bits 10 − 7 bits 11 – 8 bits
2	Specifies the number of stop bits: 0 – 1 stop bits (Word length = 5, 6, 7, 8) 1 – 1.5 stop bits (Word length = 5) 1 – 2 stop bits (Word length = 6, 7, 8) 3
3	0 = No parity 1 = A parity bit is generated during transmission and the receiver checks for received parity.
4	0 = Odd parity is generated (if LCR[3] = 1) 1 = Even parity is generated (if LCR[3] = 1)
5	Selects the forced parity format (if LCR(3) = 1) If LCR[5] = 1 and LCR[4] = 0 the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1 the parity bit is forced to 0 in the transmitted and received data.
6	Break control bit 0 = Normal operating condition 1 = Forces the transmitter output to go low to alert the communication terminal.
7	0 = Normal operating condition 1 = Divisor latch enable

9.5.6 Line Status Register (LSR)

Table 11 shows line status register bit settings.

Table 11. LSR Bit Settings

BIT	BIT SETTINGS
0	0 = No data in the receive FIFO 1 = At least one character in the RX FIFO
1	0 = No overrun error 1 = Overrun error has occurred.
2	0 = No parity error in data being read from RX FIFO 1 = Parity error in data being read from RX FIFO
3	0 = No framing error in data being read from RX FIFO 1 = Framing error occurred in data being read from RX FIFO (that is, received data did not have a valid stop bit)
4	0 = No break condition 1 = A break condition occurred and associated byte is 00 (that is, RX was low for at least one character time frame)
5	0 = Transmit hold register is not empty 1 = Transmit hold register is empty. The processor can now load up to 128 bytes of data into the THR if the TX FIFO is enabled.
6	0 = Transmitter hold and shift registers are not empty. 1 = Transmitter hold and shift registers are empty.
7	0 = Normal operation 1 = At least one parity error, framing error or break indication are stored in the receiver FIFO. Bit 7 is cleared when no errors are present in the FIFO.

When the LSR is read, LSR[4:2] reflects the error bits [BI, FE, PE] of the character at the top of the RX FIFO (next character to be read). The LSR[4:2] registers do not physically exist, as the data read from the RX FIFO is output directly onto the output data-bus, DI[4:2], when the LSR is read. Therefore, errors in a character are identified by reading the LSR and then reading the RHR.

LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO.

NOTE

Reading the LSR does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the RHR.

9.5.7 Modem Control Register (MCR)

The MCR controls the interface with the modem, data set, or peripheral device that is emulating the modem. Table 12 shows modem control register bit settings.

Table 12. MCR Bit Settings[1]

BIT	BIT SETTINGS
0	0 = Force $\overline{\text{DTR}}$ output to inactive (high) 1 = Force DTR output to active (low). In loopback controls MSR[5]
1	0 = Force $\overline{\text{RTS}}$ output to inactive (high) 1 = Force RTS output to active (low) In loopback controls MSR[4] If Auto-RTS is enabled the $\overline{\text{RTS}}$ output is controlled by hardware flow control
2	0 Disables the FIFORdy register 1 Enable the FIFORdy register In loopback controls MSR[6]
3	0 = Forces the INT output to high-impedance state 1 = Forces the INT output to the active state In loopback controls MSR[7]
4	0 = Normal operating mode 1 = Enable local loopback mode (internal) In this mode, the MCR[3:0] signals are looped back into MSR[3:0] and the TX output is looped back to the RX input internally
5	0 = Disable Xon Any function 1 = Enable Xon Any function
6	0 = No action 1 = Enable access to the TCR and TLR registers
7	0 = Divide by one clock input 1 = Divide by four clock input

[1] MCR[7:5] can be modified only when EFR[4] is set, that is, EFR[4] is a write enable.

9.5.8 Modem Status Register (MSR)

This 8-bit register provides information about the current state of the control lines from the modem, data set, or peripheral device to the processor. It also indicates when a control input from the modem changes state. Table 13 shows modem status register bit settings.

Table 13. MSR Bit Settings[1]

BIT	BIT SETTINGS
0	Indicates that $\overline{\text{CTS}}$ input (or MCR[1] in loopback) has changed state. Cleared on a read.
1	Indicates that $\overline{\text{DSR}}$ input (or MCR[0] in loopback) has changed state. Cleared on a read.
2	Indicates that $\overline{\text{RI}}$ input (or MCR[2] in loopback) has changed state from low to high. Cleared on a read.
3	Indicates that $\overline{\text{CD}}$ input (or MCR[3] in loopback) has changed state. Cleared on a read.
4	This bit is equivalent to MCR[1] during local loop-back mode. It is the complement to the $\overline{\text{CTS}}$ input.
5	This bit is equivalent to MCR[0] during local loop-back mode. It is the complement to the $\overline{\text{DSR}}$ input.
6	This bit is equivalent to MCR[2] during local loop-back mode. It is the complement to the $\overline{\text{RI}}$ input.
7	This bit is equivalent to MCR[3] during local loop-back mode. It is the complement to the $\overline{\text{CD}}$ input.

[1] The primary inputs $\overline{\text{RI}}$, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, and $\overline{\text{DSR}}$ are all active low, but their registered equivalents in the MSR and MCR (in loopback) registers are active high.

9.5.9 Interrupt Enable Register (IER)

The interrupt enable register (IER) enables each of the six types of interrupt, receiver error, RHR interrupt, THR interrupt, Xoff received, or $\overline{\text{CTS}}/\overline{\text{RTS}}$ change of state from low to high. The INT output signal is activated in response to interrupt generation. Table 14 shows interrupt enable register bit settings.

Table 14. Interrupt Enable Register (IER) Bit Settings[1]

BIT	BIT SETTINGS
0	0 = Disable the RHR interrupt 1 = Enable the RHR interrupt
1	0 = Disable the THR interrupt 1 = Enable the THR interrupt
2	0 = Disable the receiver line status interrupt 1 = Enable the receiver line status interrupt
3	0 = Disable the modem status register interrupt 1 = Enable the modem status register interrupt
4	0 = Disable sleep mode 1 = Enable sleep mode
5	0 = Disable the Xoff interrupt 1 = Enable the Xoff interrupt
6	0 = Disable the $\overline{\text{RTS}}$ interrupt 1 = Enable the $\overline{\text{RTS}}$ interrupt
7	0 = Disable the $\overline{\text{CTS}}$ interrupt 1 = Enable the $\overline{\text{CTS}}$ interrupt

[1] IER[7:4] can be modified only if EFR[4] is set, that is, EFR[4] is a write enable.
Re-enabling IER[1] causes a new interrupt, if the THR is below the threshold.

9.5.10 Interrupt Identification Register (IIR)

The IIR is a read-only 8-bit register, which provides the source of the interrupt in a prioritized manner. Table 15 shows interrupt identification register bit settings.

Table 15. IIR Bit Settings

BIT	BIT SETTINGS
0	0 = An interrupt is pending 1 = No interrupt is pending
3:1	3-Bit encoded interrupt. See Table 14
4	1 = Xoff or special character has been detected
5	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ low to high change of state
7:6	Mirror the contents of FCR[0]

The interrupt priority list is illustrated in Table 16.

Table 16. Interrupt Priority List

PRIORITY LEVEL	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	INTERRUPT SOURCE
1	0	0	0	1	1	0	Receiver line status error
2	0	0	1	1	0	0	Receiver timeout interrupt
2	0	0	0	1	0	0	RHR interrupt
3	0	0	0	0	1	0	THR interrupt
4	0	0	1	0	0	0	Modem interrupt
5	0	1	0	0	0	0	Received Xoff signal or special character
6	1	0	0	0	0	0	$\overline{\text{CTS}}$, $\overline{\text{RTS}}$ change of state from active (low) to inactive (high)

9.5.11 Enhanced Feature Register (EFR)

This 8-bit register enables or disables the enhanced features of the UART. Table 17 shows the enhanced feature register bit settings.

Table 17. EFR Bit Settings

BIT	BIT SETTINGS
3:0	Combinations of software flow control can be selected by programming bit 3 to bit 0. See Table 1.
4	Enhanced functions enable bit. 0 = Disables enhanced functions and writing to IER[7:4], FCR[5:4], MCR[7:5] 1 = Enables the enhanced function IER[7:4], FCR[5:4], and MCR[7:5] can be modified, that is, this bit is therefore a write enable
5	0 = Normal operation 1 = Special character detect. Received data is compared with Xoff-2 data. If a match occurs, the received data is transferred to FIFO and IIR[4] is set to 1 to indicate a special character has been detected.
6	$\overline{\text{RTS}}$ flow control enable bit 0 = Normal operation 1 = $\overline{\text{RTS}}$ flow control is enabled, that is, $\overline{\text{RTS}}$ pin goes high when the receiver FIFO HALT trigger level TCR[3:0] is reached, and goes low when the receiver FIFO RESTORE transmission trigger level TCR[7:4] is reached.
7	$\overline{\text{CTS}}$ flow control enable bit 0 = Normal operation 1 = $\overline{\text{CTS}}$ flow control is enabled, that is, transmission is halted when a high signal is detected on the $\overline{\text{CTS}}$ pin

9.5.12 Divisor Latches (DLL, DLH, DLF)

Two 8-bit registers store the 16-bit divisor and a 6-bit fractional divisor for generation of the baud clock in the baud rate generator. DLH, stores the most significant part of the divisor. DLL stores the least significant part of the division. DLF stores the fractional value of the divisor as x / 64 where x is the value in DLF.

Table 18. DLF Bit Values

BIT	BIT SETTINGS
7	Baud divider bit 0 (default) = Enable divide-by-16 baud divider 1 = Enable divide-by-8 baud divider
6	Reserved
5:0	6 bit fractional divider value (x / 64)

For more information on how to calculate the fractional values, see Fractional Divisor.

DLL, DLH and DLF can only be written to before sleep mode is enabled (that is, before IER[4] is set).

9.5.13 Transmission Control Register (TCR)

This 8-bit register is used to store the receive FIFO threshold levels to start or stop transmission during hardware or software flow control. Table 19 shows transmission control register bit settings.

Table 19. TCR Bit Settings

BIT	BIT SETTINGS
3:0	RCV FIFO trigger level to HALT transmission (0 to 60)
7:4	RCV FIFO trigger level to RESTORE transmission (0 to 60)

TCR trigger levels are available from 0 to 120 bytes with a granularity of 8.

TCR can be written to only when EFR[4] = 1 and MCR[6] = 1. The programmer must program the TCR such that TCR[3:0] > TCR[7:4]. There is no built-in hardware check to make sure this condition is met. Also, the TCR must be programmed with this condition before Auto-$\overline{\text{RTS}}$ or software flow control is enabled to avoid spurious operation of the device.

9.5.14 Trigger Level Register (TLR)

This 8-bit register is used to store the transmit and received FIFO trigger levels used for DMA and interrupt generation. Trigger levels from 8 to 120 can be programmed with a granularity of 8. Table 20 shows trigger level register bit settings.

Table 20. TLR Bit Settings

BIT	BIT SETTINGS
3:0	Transmit FIFO trigger levels (8 to 120), number of spaces available
7:4	RCV FIFO trigger levels (8 to 120), number of characters available

TLR can be written to only when EFR[4] = 1 and MCR[6] = 1. If TLR[3:0] or TLR[7:4] are 0, then the selectable trigger levels via the FIFO control register (FCR) are used for the transmit and receive FIFO trigger levels. Trigger levels from 8 to 120 bytes are available with a granularity of 8. The TLR should be programmed for N / 8, where N is the desired trigger level.

9.5.15 FIFO Ready Register

The FIFO ready register provides realtime status of the transmit and receive FIFOs. Table 21 shows the FIFO ready register bit settings. The trigger level mentioned in Table 21 refers to the setting in either FCR (when TLR value is 0), or TLR (when it has a nonzero value).

Table 21. FIFO Ready Register

BIT	BIT SETTINGS
0	0 = There are fewer than a TX trigger level number of spaces available in the TX FIFO. 1 = There are at least a TX trigger level number of spaces available in the TX FIFO.
3:1	Unused, always 0.
4	0 = There are fewer than a RX trigger level number of characters in the RX FIFO. 1 = The RX FIFO has more than a RX trigger level number of characters available for reading or a timeout condition has occurred.
7:5	Unused, always 0

The FIFORdy register is a read only register and can be accessed when the UART is selected. $\overline{\text{CS}}$ = 0, MCR[2] (FIFORdy Enable) is a logic 1, and loopback is disabled. Its address is 111.

9.5.16 Alternate Function Register (AFR)

The AFR is used to enable some extra functionality beyond the capabilities of the original TL16C750. The first addition is the IrDA mode, which supports Standard IrDA (SIR) mode with baud rates from 2400 to 115.2 kbps. The third addition is support for RS-485 bus drivers or transceivers by providing an output pin ($\overline{\text{DTR}}$), which is timed to keep the RS-485 driver enabled as long as transmit data is pending.

The AFR is located at A[2:0] = 010 when LCR[7:5] = 100.

Table 22. AFR Bit Settings

BIT	BIT SETTINGS
0	Reserved bit. Does not do anything
1	IREN enables the IrDA SIR mode. This mode is only specified to 115.2 bps; TI does not recommend the use of this mode at higher speeds.
2	485EN enables the half duplex RS-485 mode and causes the $\overline{\text{DTR}}$ output to be set high whenever there is any data in the THR or TSR and to be held high until the delay set by DLY2:0 has expired, at which time it is set low. The $\overline{\text{DTR}}$ output is intended to drive the enabled input of an RS-485 driver. When this bit is set, the transmitter interrupts are held off until the TSR is empty, unless 485LG is set.
3	485LG is set when the 485EN is set. This bit indicates that a relatively large data block is being set, requiring more than a single load of the xmt fifo. In this case, the transmitter interrupts occur as in the standard RS-232 mode, either when the xmt fifo contents drop below the xmt threshold or when the xmt fifo is empty.
4	RCVEN is valid only when 485EN or IREN is set, and allows the serial receiver to listen in or snoop on the RS-485 traffic or IrDA traffic. RS-485 mode is generally considered half duplex, and usually a node is either driving or receiving, but there can be cases when it is advantageous to verify what you are sending. This can be used to detect collisions or as part of an arbitration mechanism on the bus. When both RCVEN and 485EN are set, the receiver stores any data presented on RX, if any. Note that implies that the external RS-485 receiver is enabled. Whenever 485EN is cleared, the serial receiver is enabled for normal full duplex RS-232 traffic. If RCVEN is cleared while 485EN is set, the receiver is disabled while transmitting. SIR is also considered half duplex. Often the light energy from the transmitting LED is coupled back into the receiving PIN diode, which creates an input data stream that is not of interest to the host. Disabling the receiver (clearing RCVEN) prevents this reception, and eliminates the task of unloading the data. On the other hand, for diagnostic or other purposes, it may be useful to observe this data stream. For example, a mirror could be used to intentionally couple the output LED to the input PIN. For these cases, RCVEN could be set to enable the receiver. NOTE: When RCVEN is cleared (set to 0), the character timeout interrupt is not available, even in RS-232 mode. This can be useful when checking code for valid threshold interrupts, as the timeout interrupt does not override the threshold interrupt.
7:5	DLY2 to DLY0 sets a delay after the last stop bit of the last data byte being set before the $\overline{\text{DTR}}$ is set low, to allow for long cable runs. The delay is in number of bit times and is enabled by 485EN. The delay starts only when both the xmt serial shift register (TSR) is empty and the xmt fifo (THR) is empty, and if started, is cleared by any data being written to the THR.

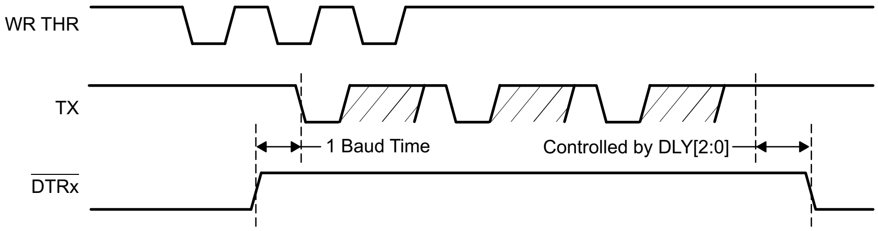
Table 23. LOOP and RCVEN Functionality

LOOP MODE	RCVEN	AFR	MODE	DESCRIPTION
LOOP mode off, MCR4 = 0, RX, TX active	RCVEN = 1	AFR = 10	RS-232	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
		AFR = 14	RS-485	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
		AFR = 12	IrDA	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
	RCVEN = 0	AFR = 00	RS-232	Receive threshold and error detection interrupts available Data stored in receive FIFO
		AFR = 04	RS-485	No data stored in receive FIFO, hence no interrupts available
		AFR = 02	IrDA	No data stored in receive FIFO, hence no interrupts available
LOOP mode on, MCR4 = 1, RX, TX inactive	RCVEN = 1	AFR = 10	RS-232	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
		AFR = 14	RS-485	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
		AFR = 12	IrDA	Receive threshold, timeout, and error detection interrupts available Data stored in receive FIFO
	RCVEN = 0	AFR = 00	RS-232	Receive threshold and error detection interrupts available Data stored in receive FIFO
		AFR = 04	RS-485	Receive threshold and error detection interrupts available Data stored in receive FIFO
		AFR = 02	IrDA	Receive threshold and error detection interrupts available Data stored in receive FIFO

9.5.17 RS-485 Mode

The RS-485 mode is intended to simplify the interface between the UART and an RS-485 driver or transceiver. When enabled by setting 485EN, the $\overline{\text{DTR}}$ output goes high one bit time before the first stop bit of the first data byte being sent, and remains high as long as there is pending data in the TSR or THR (xmt fifo). After both are empty (after the last stop bit of the last data byte), the $\overline{\text{DTR}}$ output stays high for a programmable delay of 0 to 15 bit times, as set by DLY[2:0]. This helps preserve data integrity over long signal lines. This is illustrated in the following.

Often RS-485 packets are relatively short and the entire packet can fit within the 128 byte xmt fifo. In this case, it goes empty when the TSR goes empty. But in cases where a larger block needs to be sent, it is advantageous to reload the xmt fifo as soon as it is depleted. Otherwise, the transmission stalls while waiting for the xmt fifo to be reloaded, which varies with processor load. In this case, it is best to also set 485LG (large block), which causes the transmit interrupt to occur wither when the THR becomes empty (if the xmt fifo level was not above the threshold), or when the xmt fifo threshold is crossed. The reloading of the xmt fifo occurs while some data is being shifted out, eliminating fifo underrun. If desired, when the last bytes of a current transmission are being loaded in the xmt fifo, 485LG can be cleared before the load and the transmit interrupt occurs on the TSR going empty.



A. Waveforms are not shown to scale, as the WR THR pulses typically are less than 100 ns, where the TX waveform varies with baud rate but is typically in the microsecond range.

Figure 31. $\overline{\text{DTR}}$x and Transmit Data Relationship

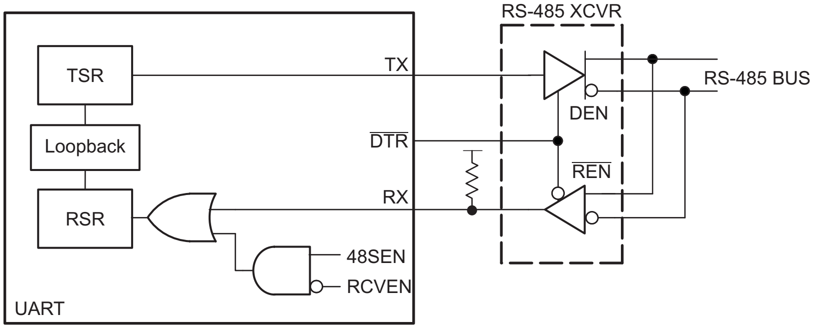


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Figure 32. RS-485 Application Example 1

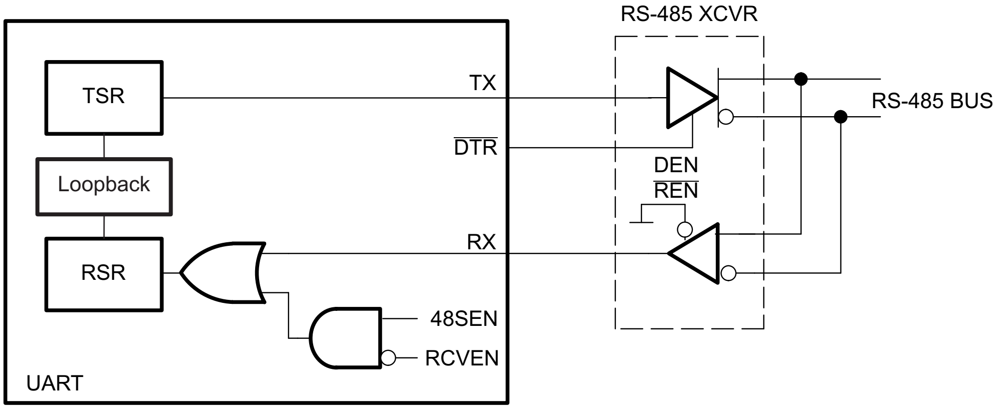

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Figure 33. RS-485 Application Example 2

9.5.18 IrDA Overview

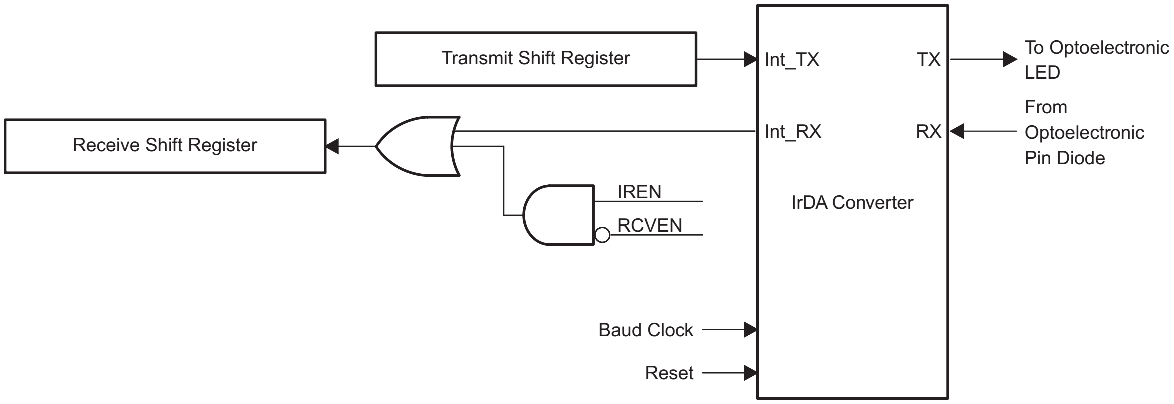

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Figure 34. IrDA Mode

The IrDA defines several protocols for sending and receiving serial infrared data, including rates of 115.2 kbps, 0.576 Mbps, 1.152 Mbps, and 4 Mbps. The low rate of 115.2 kbps was specified first and the others must maintain downward compatibility with it. At the 115.2 kbps rate, the protocol implemented in the hardware is fairly simple. It primarily defines a serial infrared data word to be surrounded by a start bit equal to 0 and a stop bit equal to 1. Individual bits are encoded or decoded the same whether they are start, data, or stop bits. The IrDA engine in the TL16C750E device only evaluates single bits and follows the 115.2-kbps protocol. The 115.2-kbps rate is a maximum rate. When both ends of the transfer are setup to a lower but matching speed, the protocol still works. The clock used to code or sample the data is 16 times the baud rate, or 1.843-MHz maximum. To code a 1, no pulse is sent or received for 1-bit time period, or 16 clock cycles. To code a 0, one pulse is sent or received within a 1-bit time period, or 16 clock cycles. The pulse must be at least 1.6-μs wide and 3 clock cycles long at 1.843 MHz. At lower baud rates the pulse can be 1.6 μs wide or as long as 3 clock cycles. The transmitter output, TX, is intended to drive a LED circuit to generate an infrared pulse. The LED circuits work on positive pulses. A terminal circuit is expected to create the receiver input, RX. Most, but not all, PIN circuits have inversion and generate negative pulses from the detected infrared light. Their output is normally high. The TL16C750E device can decode either negative or positive pulses on RX.

9.5.19 IrDA Encoder Function

Serial data from a UART is encoded to transmit data to the optoelectronics. While the serial data input to this block (Int_TX) is high, the output (TX) is always low, and the counter used to form a pulse on TX is continuously cleared. After Int_TX resets to 0, TX rises on the falling edge of the 7th 16XCLK. On the falling edge of the 10th 16XCLK pulse, TX falls, creating a 3-clock-wide pulse. While Int_TX stays low, a pulse is transmitted during the seventh to tenth clocks of each 16-clock bit cycle.

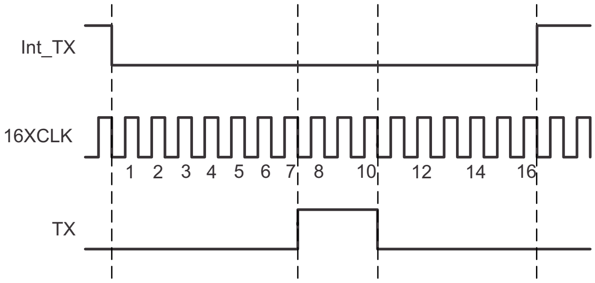


Figure 35. IrDA-SIR Encoding Scheme – Detailed Timing Diagram

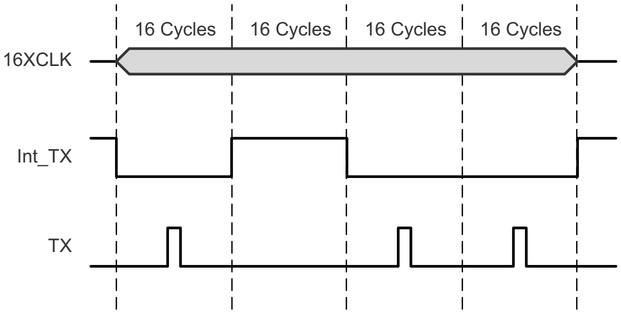


Figure 36. Encoding Scheme – Macro View

After reset, Int_RX is high and the 4-bit counter is cleared. When a falling edge is detected on RX, Int_RX falls on the next rising edge of 16XCLK with sufficient setup time. Int_RX stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (falling edges) are detected on RX, Int_RX remains high.

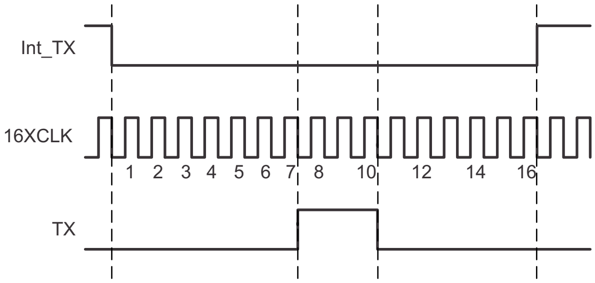


Figure 37. IrDA-SIR Decoding Scheme – Detailed Timing Diagram

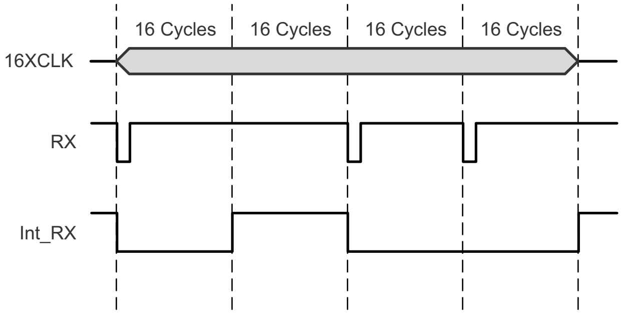


Figure 38. IrDA-SIR Decoding Scheme – Macro View

It is possible for jitter or slight frequency differences to cause the next falling edge on RX to be missed for one 16XCLK cycle. In that case, a 1-clock-wide pulse appears on Int_RX between consecutive 0s. It is important for the UART to strobe Int_RX in the middle of the bit time to avoid latching this 1-clock-wide pulse. The TL16C750E UART already strobes incoming serial data at the proper time. Otherwise, note that data is required to be framed by a leading 0 and a trailing 1. The falling edge of that first 0 on Int_RX synchronizes the read strobe. The strobe occurs on the 8th 16XCLK pulse after the Int_RX falling edge and once every 16 cycles thereafter until the stop bit occurs.

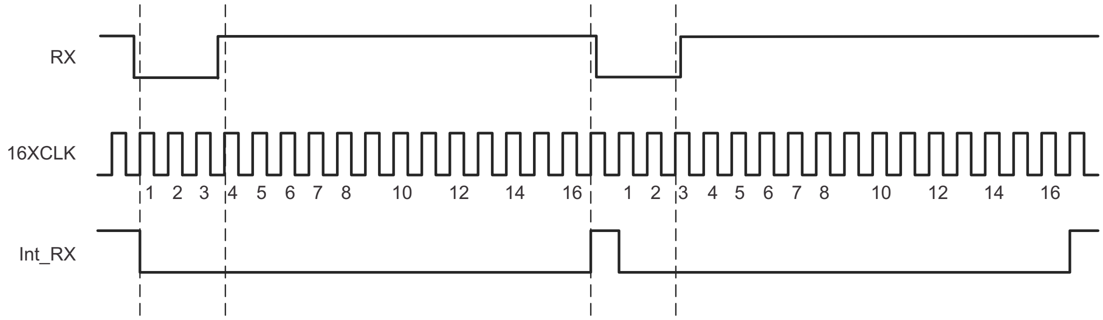


Figure 39. Timing Causing 1-Clock-Wide Pulse Between Consecutive Ones

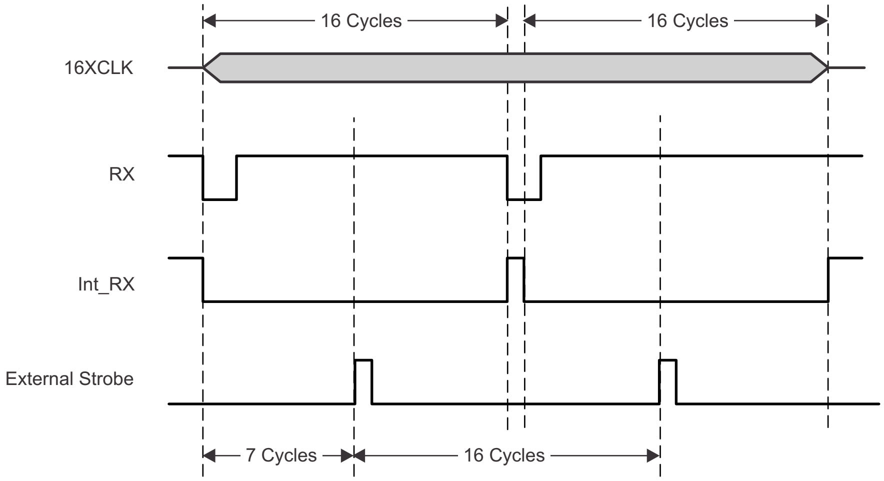


Figure 40. Recommended Strobing for Decoded Data

The TL16C750E device can decode positive pulses on RX. The timing is different, but the variation is invisible to the UART. The decoder, which works from the falling edge, now recognizes a 0 on the trailing edge of the pulse rather than on the leading edge. As long as the pulse duration is fairly constant, as defined by the specification, the trailing edges should also be 16 clock cycles apart and data can readily be decoded. The 0 appears on Int_RX after the pulse rather than at the start of it.

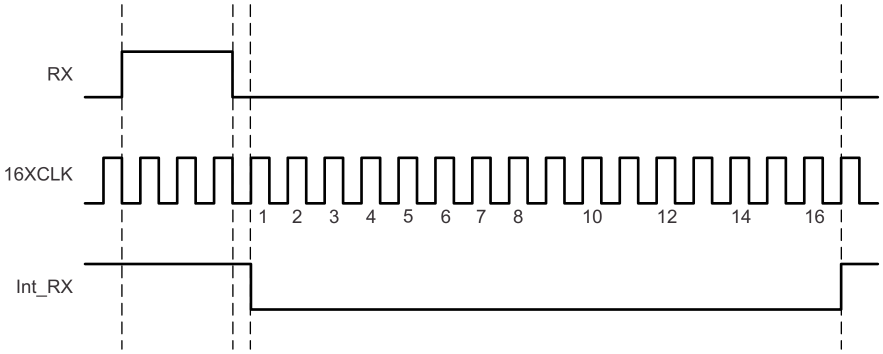


Figure 41. Positive RX Pulse Decode – Detailed View

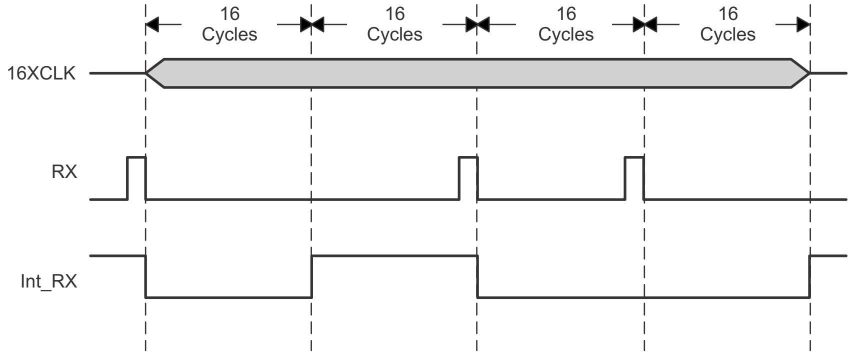


Figure 42. Positive RX Pulse Decode – Macro View

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The typical implementation is to use the TL16C750E as a RS-232 interface, which is intended to operate with a 5-V microprocessor.

10.2 Typical Application

The typical application is to communicate over UART, either through a RS-232 transceiver, or directly. The general initialization sequence is recommended as following:

1. Set the desired baud rate with DLL and DLH (or with fractional baud rate if required)
2. Set the desired word length and other settings in the LCR register.
3. Reset the FIFOs with the FCR registers

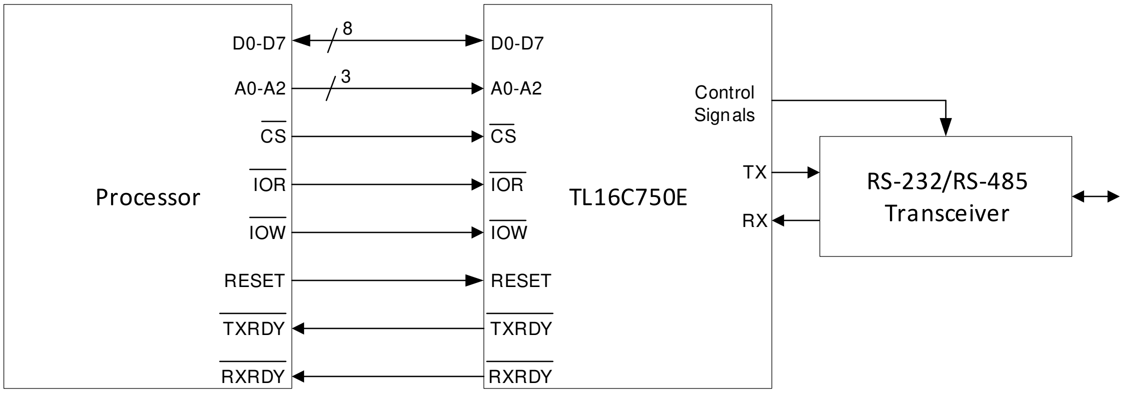


Figure 43. Typical Application

10.2.1 Design Requirements

For this example, we'll assume a basic 9600 baud UART communication. This is one of the most common and basic UART configurations.

Table 24. Example design considerations

Constraint	Value
Crystal oscillator speed	24 MHz
Desired baud rate	9600 baud
Parity	None
Data bits	8 bits
Stop bits	1 bit

10.2.2 Detailed Design Procedure

The procedure to setup the part for transmission involves only a few register writes. Each step of the process is outlined

10.2.2.1 Set the desired baud rate

As per Table 24, the desired baud rate is 9600 with an input clock of 24 MHz. The math required to calculate the register values is outlined in Programmable Baud Rate Generator with Fractional Divisor and Fractional Divisor. Since the device by default uses a 16x over sample setting, the math is 24E9 / (16 * 9600) = 156.25. This shows that the fractional baud rate feature is required to achieve 9600 baud. Since the fractional baud rate gives x/64 resolution, 0.25 * 64 = 16. The below values are the divisor values to be used in the registers.

Table 25. 9600 baud divisor values

Register	Description	Value
DLH	MSB of the divisor	0x00
DLL	LSB of the divisor	0x9C
DLF	Fractional (1/64) divisor	0x10

Since these registers have access considerations in order to write to them (see Table 8), a few extra writes are required to enable the writes to the desired registers.

Table 26. Register writes to configure baud rate

Step	Description	Register & Access Type	Value
1	Enable access to EFR (enhanced function) register	LCR (0b011) [W]	0xBF
2	Enable the enhanced functionality (fractional baud rate)	EFR (0b010) [W]	0x10
3	Enable extra feature registers and 8 bits/no parity/1 stop bit	LCR (0b011) [W]	0x93
4	Write the MSB of the divisor	DLH (0b001) [W]	0x00
5	Write to the LSB of the divisor	DLL (0b000) [W]	0x9C
6	Write to the fractional divisor	DLF (0b111) [W]	0x10
7	Change LCR back to normal mode	LCR (0b011) [W]	0x13

10.2.2.2 Reset the fifos

Since the baud rate and UART settings are configured in the previous section, configuration is complete and the FIFOs are ready to be reset for use.

Table 27. Register writes to reset FIFOs

Step	Description	Register & Access Type	Value
1	Reset FIFOs	FCR (0b010) [W]	0x06
2	Enable the FIFOs	FCR (0b010) [W]	0x01

10.2.2.3 Sending data on the bus

Once configuration is complete, the part is ready for data transmission. For the example the data 0xAA is written to the bus. This is quite simple to do. Writing to THR (0b000) automatically shifts the written data into an internal FIFO (since FIFOs are enabled) and then begins being shifted out onto the UART bus.

Table 28. Register writes to writing data onto the bus

Step	Description	Register & Access Type	Value
1	Write data onto bus	THR (0b000) [W]	0xAA

10.2.3 Application Curves

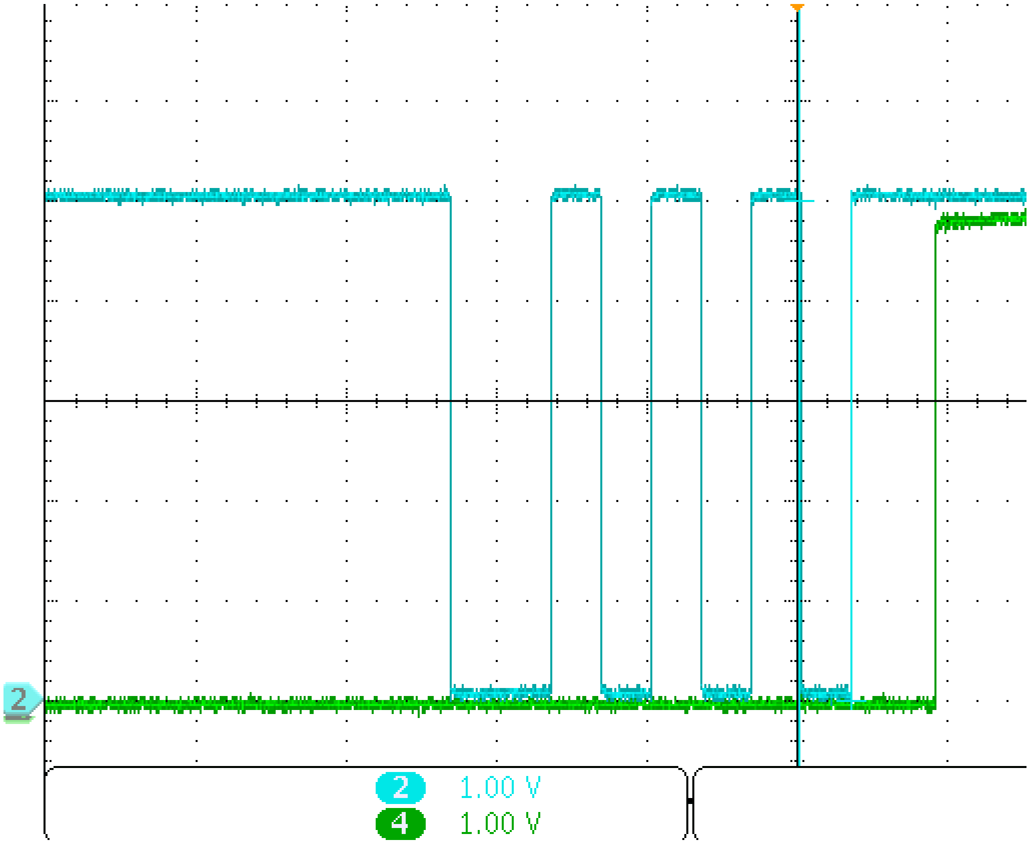


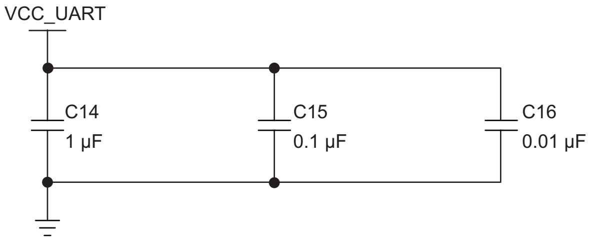
Figure 44. Waveform showing 0xAA waveform

11 Power Supply Recommendations

The power supply must provide a constant voltage with a 10% maximum variation of the nominal value and has to be able to provide at least the maximum current consumption of the device for the selected nominal voltage only for the UART device:

- V_{CC} = 1.8 V
- V_{CC} = 2.5 V
- V_{CC} = 3.3 V
- V_{CC} = 5 V

The VCC pin must have a 1-µF bypass capacitor placed as close as possible to this pin. Also, TI recommends to include two extra capacitors in parallel, which should also be placed as close as possible to the VCC pin. The suggested values for these extra capacitors are 0.1 µF and 0.01 µF, respectively.



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Place as close as possible to the VCC pin of the UART.

Figure 45. Recommended Bypass Capacitors Array

12 Layout

12.1 Layout Guidelines

Traces, Vias, and Other PCB Components: A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 28).
- Separate high-speed signals (for example, clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other

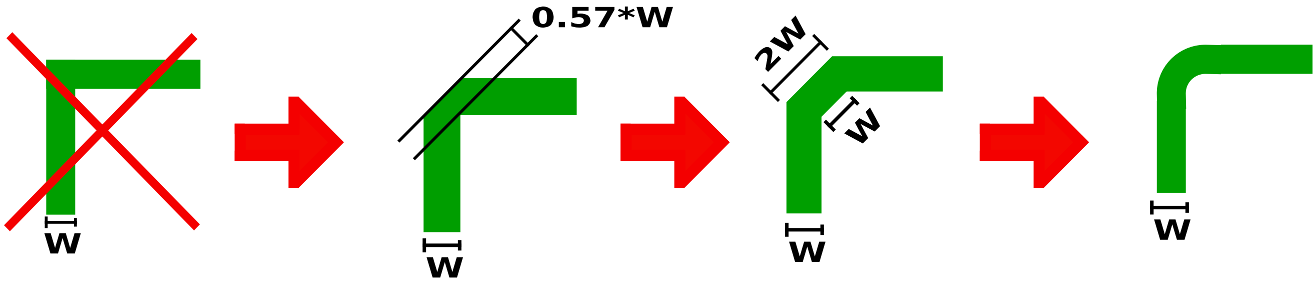

Figure 46. Layout Do's and Don'ts

12.2 Layout Examples

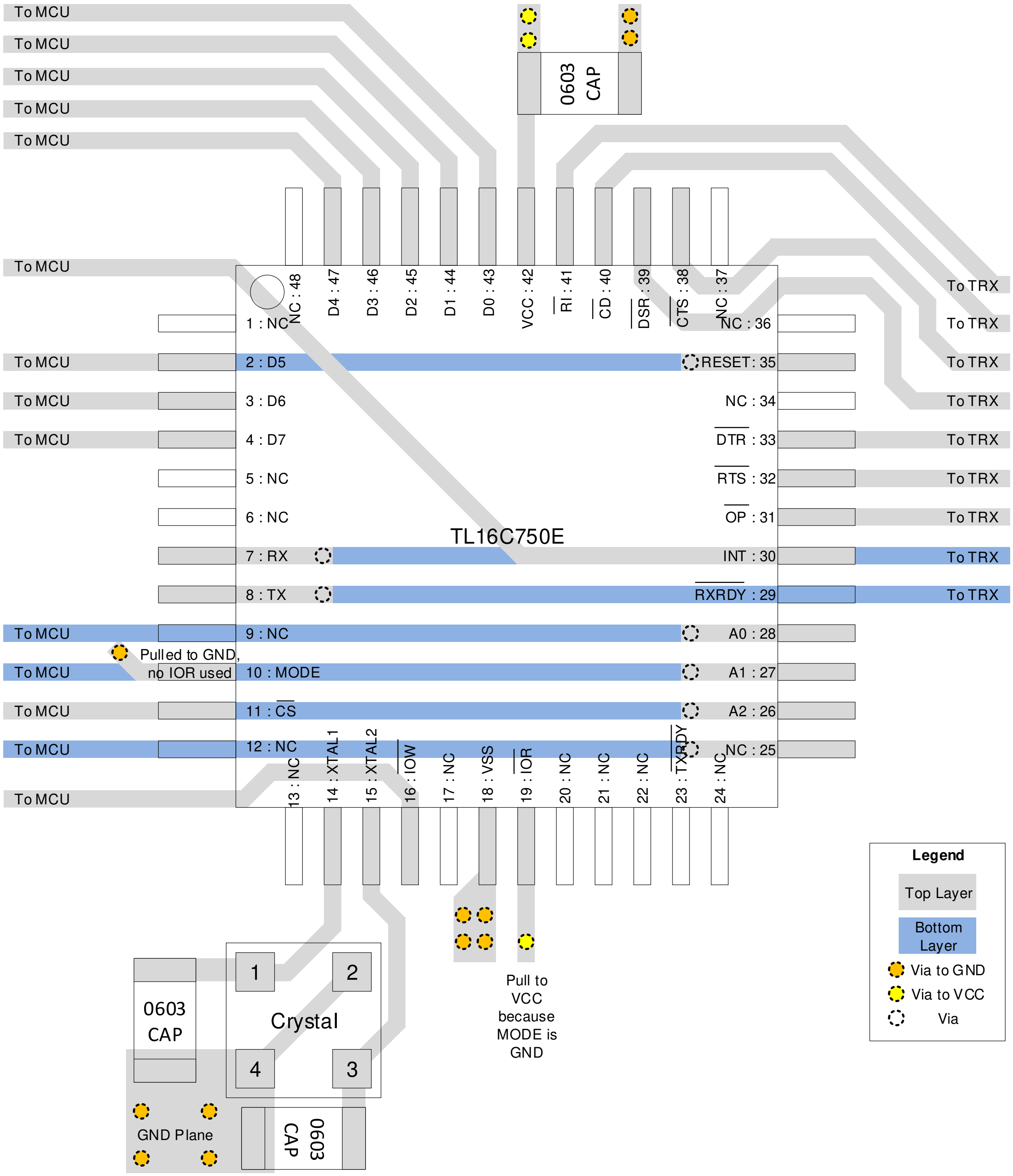

Figure 47. Typical UART Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

-
-

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL16C750EPFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TL16C750E	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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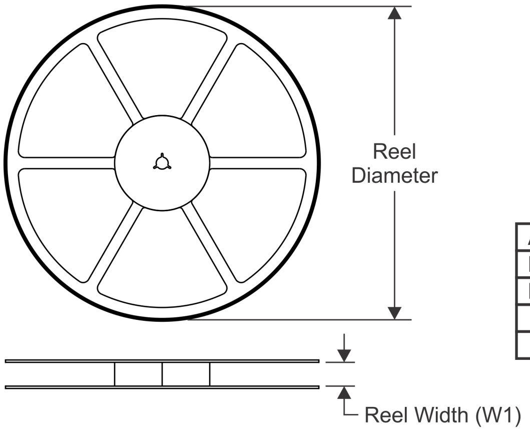
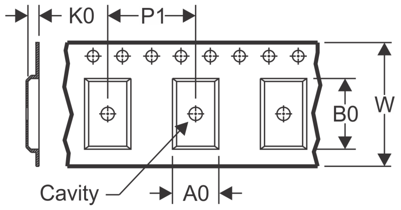
TAPE AND REEL INFORMATION

REEL DIMENSIONS

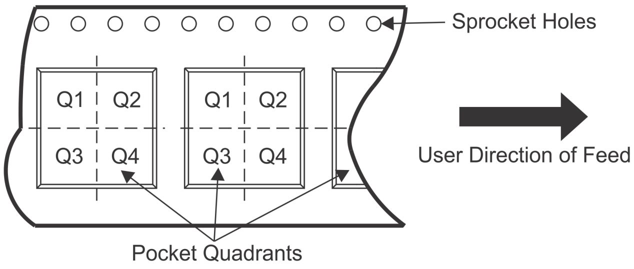


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

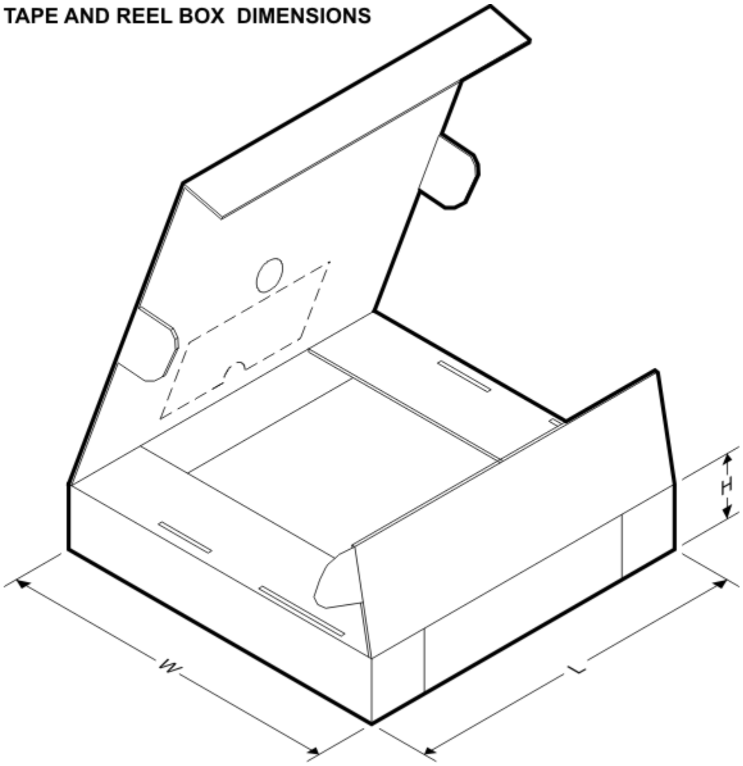
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL16C750EPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

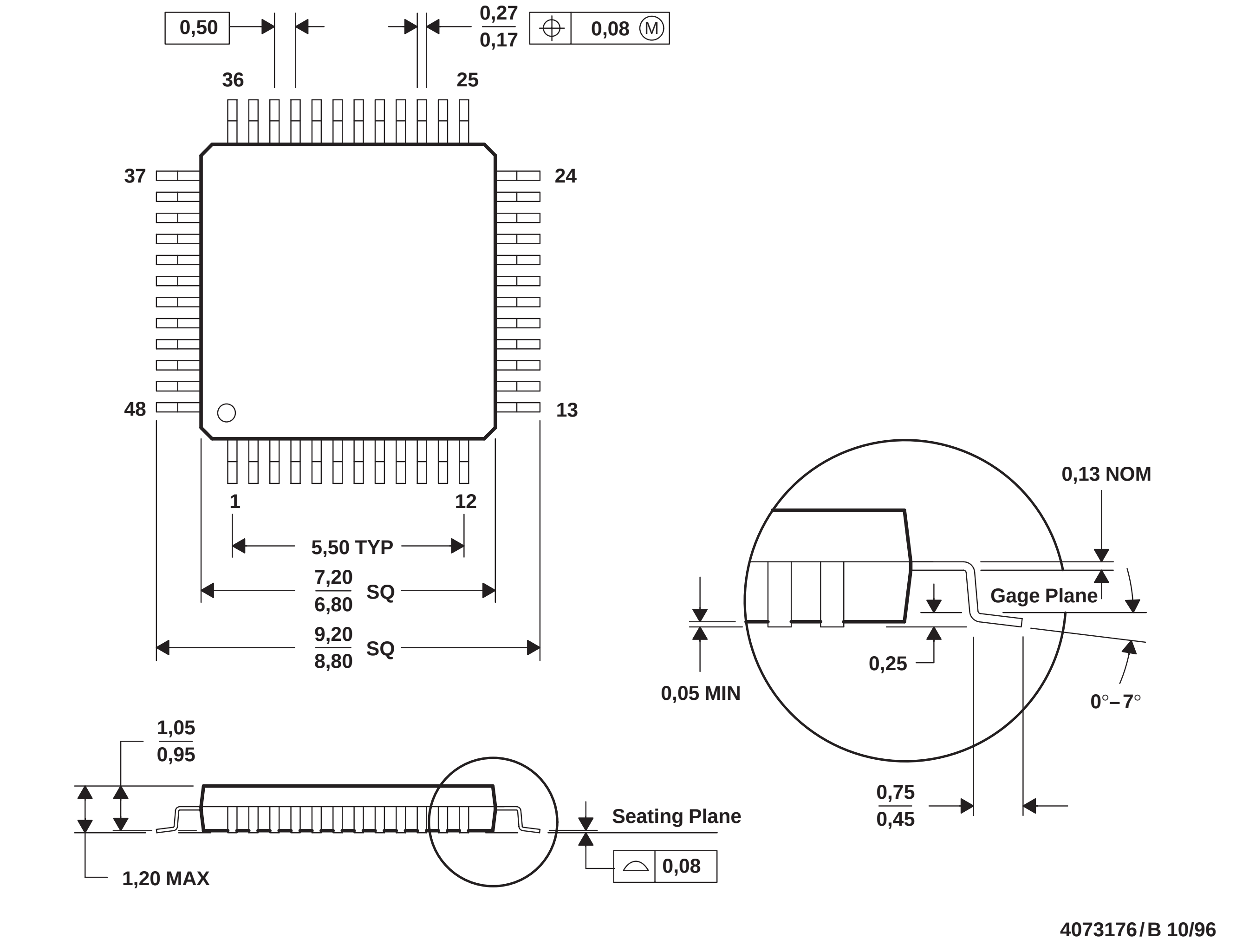
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

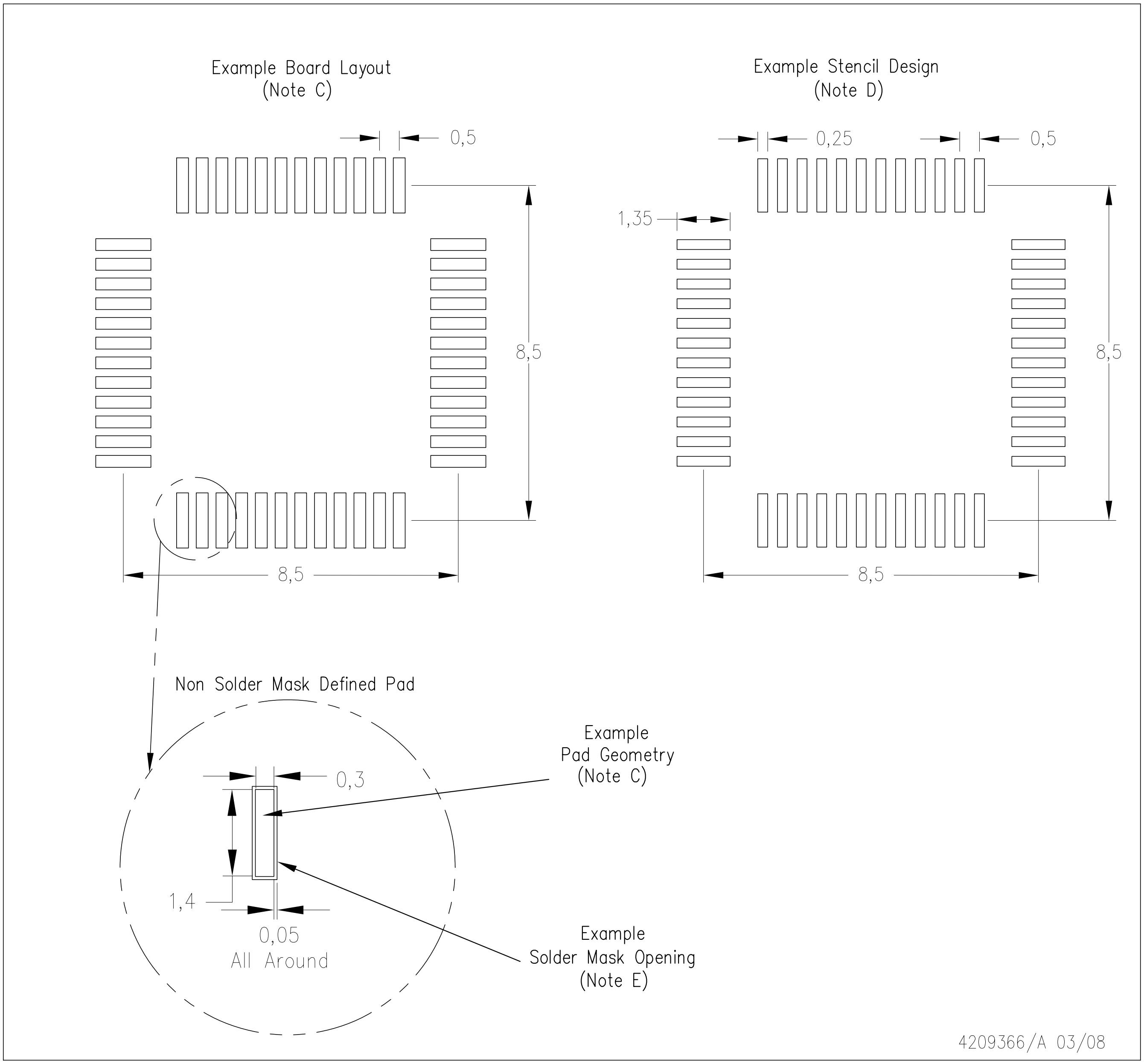
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL16C750EPFBR	TQFP	PFB	48	1000	336.6	336.6	31.8

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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