

# ADSxx50 Dual, 750-kSPS, 16-, 14-, and 12-Bit, Simultaneous-Sampling, Analog-to-Digital Converters

## 1 Features

- 16-, 14-, and 12-Bit Pin-Compatible Family
- Simultaneously Samples Two Channels
- Pseudo-Differential Analog Inputs
- Fast Throughput: 750 kSPS
- Excellent DC Performance:
  - Linearity:
    - ADS8350: 16-Bit NMC DNL,  $\pm 2.5$  LSB, Max INL
    - ADS7850: 14-Bit NMC DNL,  $\pm 1.5$  LSB, Max INL
    - ADS7250: 12-Bit NMC DNL,  $\pm 1$  LSB, Max INL
- Excellent AC Performance:
  - ADS8350: 85-dB SNR,  $-96$ -dB THD
  - ADS7850: 81-dB SNR,  $-90$ -dB THD
  - ADS7250: 73-dB SNR,  $-88$ -dB THD
- Simple Serial Interface
- Fully-Specified Over Extended Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Small Footprint: WQFN-16 (3 mm  $\times$  3 mm)

## 2 Applications

- Motor Control: Position Measurement Using SinCos Encoders
- Optical Networking: EDFA Gain Control Loop
- Protection Relays
- Power Quality Measurement
- Three-Phase Power Controls
- Programmable Logic Controllers
- Industrial Automation

## 3 Description

The ADS8350, ADS7850, and ADS7250 devices belong to a family of pin-compatible, dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs) that support pseudo-differential analog inputs. All devices support a simple serial interface that can operate over a wide power-supply range, enabling easy communication with a large variety of host controllers.

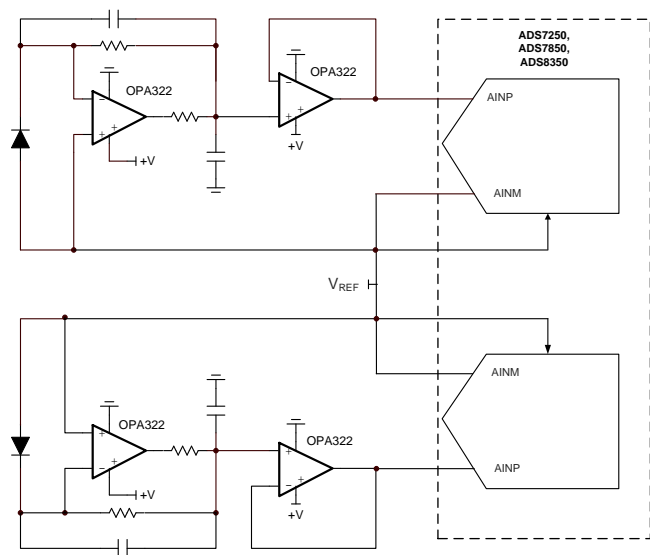
All devices are fully specified over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) and are available in a pin-compatible, WQFN-16 (3 mm  $\times$  3 mm) package.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS7250	WQFN (16)	3.00 mm $\times$ 3.00 mm
ADS7850		
ADS8350		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Functional Block Diagram**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

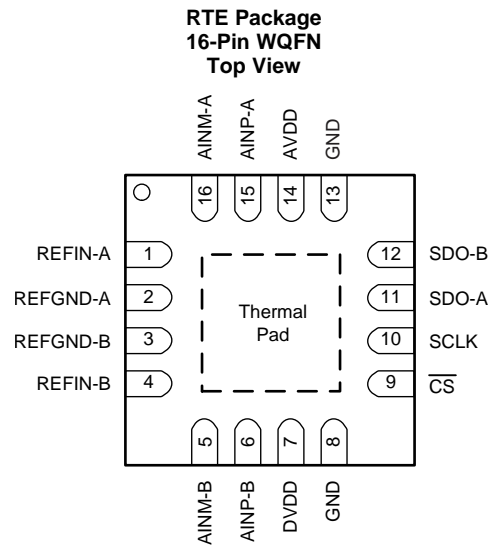
Changes from Revision C (June 2014) to Revision D	Page
• Changed <i>ESD Ratings</i> title, updated to current format, moved <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table ..... 4	4
• Changed <i>Timing Characteristics</i> table: split table into <i>Timing Requirements</i> and <i>Switching Characteristics</i> ..... 9	9
• Deleted $t_{SU\_DOCK}$ and $t_{HT\_CKDO}$ parameters, replaced with $t_{D\_CKDO}$ parameter ..... 9	9
• Changed <i>Timing Diagram</i> figure ..... 9	9

Changes from Revision B (April 2014) to Revision C	Page
• Changed Device Information table to current standards ..... 1	1
• Corrected pseudo-differential input and reference connections in the functional block diagram ..... 1	1
• Changed Handling Ratings table to current standards ..... 4	4

Changes from Revision A (January 2014) to Revision B	Page
• Changed format to meet latest data sheet standards; added <i>Layout</i> section, moved existing sections ..... 1	1
• Deleted Ordering Information section ..... 3	3

Changes from Original (May 2013) to Revision A	Page
• Released to production ..... 1	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINM-A	16	Analog input	Negative analog input, ADC_A
AINM-B	5	Analog input	Negative analog input, ADC_B
AINP-A	15	Analog input	Positive analog input, ADC_A
AINP-B	6	Analog input	Positive analog input, ADC_B
AVDD	14	Supply	ADC supply voltage
$\overline{CS}$	9	Digital input	Chip-select signal; active low
DVDD	7	Supply	Digital I/O supply
GND	8, 13	Supply	Device ground
REFGND-A	2	Supply	Reference ground potential, ADC_A
REFGND-B	3	Supply	Reference ground potential, ADC_B
REFIN-A	1	Analog input	Reference voltage input, ADC_A
REFIN-B	4	Analog input	Reference voltage input, ADC_B
SCLK	10	Digital input	Serial communication clock
SDO-A	11	Digital output	Data output for serial communication, ADC_A
SDO-B	12	Digital output	Data output for serial communication, ADC_B
Thermal pad		Supply	Exposed thermal pad. TI recommends connecting the thermal pad to the printed circuit board (PCB) ground.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	AVDD to GND	-0.3	7	V
	DVDD to GND	-0.3	7	
Analog input voltage	AINP_x to REFGND_x	REFGND_x - 0.3	AVDD + 0.3	V
	AINM_x to REFGND_x	REFGND_x - 0.3	AVDD + 0.3	
	REFIN_x to REFGND_x	REFGND_x - 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS}$ , SCLK to GND	GND - 0.3	DVDD + 0.3	V
Ground voltage difference	REFGND_x - GND		0.3	V
Input current	Any pin except supply pins		±10	mA
Maximum virtual junction temperature, T <sub>J</sub>			150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		5		V
DVDD	Digital power supply		3.3		V

### 6.4 Thermal Information

THERMAL METRIC		ADS7250, ADS7850, ADS8350		UNIT
		RTE (WQFN)		
		16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	33.3		°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	29.5		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.3		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.4		°C/W
R <sub>θJcbot</sub>	Junction-to-case (bottom) thermal resistance	0.9		°C/W

## 6.5 Electrical Characteristics: All Devices

minimum and maximum specifications are at  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $\text{AVDD} = 5\text{ V}$ ,  $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$ , and  $t_{\text{DATA}} = 750\text{ kSPS}$  (unless otherwise noted); typical values are at  $T_A = 25^{\circ}\text{C}$ ,  $\text{AVDD} = 5\text{ V}$ , and  $\text{DVDD} = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
FSR	Full-scale input range, (AINP_x – AINM_x)	$\text{AVDD} \geq 2 \times V_{\text{REF}}^{(1)}$ , $\text{AINM}_x = V_{\text{REF}}$	$-V_{\text{REF}}$		$V_{\text{REF}}$	V
$V_{\text{INP}}$	Absolute input voltage, (AINP_x to REFGND)	$\text{AVDD} \geq 2 \times V_{\text{REF}}^{(1)}$ , $\text{AINM}_x = V_{\text{REF}}$	0		$2 \times V_{\text{REF}}$	V
$V_{\text{INM}}$	Absolute input voltage, (AINM_x to REFGND)		$V_{\text{REF}} - 0.1$	$V_{\text{REF}}$	$V_{\text{REF}} + 0.1$	V
$C_{\text{IN}}$	Input capacitance	In sample mode		40		pF
		In hold mode		4		
$I_{\text{IN}}$	Input leakage current			1.5		nA
<b>SAMPLING DYNAMICS</b>						
$f_{\text{DATA}}$	Data rate				750	kSPS
$t_{\text{A}}$	Aperture delay			8		ns
	$t_{\text{A}}$ match	ADC_A to ADC_B		40		ps
	Aperture jitter			10		ps
$f_{\text{CLK}}$	Clock frequency				24	MHz
<b>VOLTAGE REFERENCE INPUT</b>						
$V_{\text{REF}}$	Reference input voltage		2.25	2.5	$\text{AVDD} / 2^{(1)}$	V
$I_{\text{REF}}$	Reference input current			300		$\mu\text{A}$
	Reference leakage current				1	$\mu\text{A}$
$C_{\text{REF}}$	External ceramic reference capacitance			10		$\mu\text{F}$
<b>DIGITAL INPUTS<sup>(2)</sup></b>						
$V_{\text{IH}}$	Input voltage, high		0.7 DVDD		$\text{DVDD} + 0.3$	V
$V_{\text{IL}}$	Input voltage, low		-0.3		0.3 DVDD	V
<b>DIGITAL OUTPUTS<sup>(2)</sup></b>						
$V_{\text{OH}}$	Output voltage, high	$I_{\text{OH}} = 500\text{-}\mu\text{A}$ source	0.8 DVDD		DVDD	V
$V_{\text{OL}}$	Output voltage, low	$I_{\text{OH}} = 500\text{-}\mu\text{A}$ sink	0		0.2 DVDD	V
<b>POWER SUPPLY</b>						
AVDD	Analog supply voltage, AVDD to GND		4.5 <sup>(1)</sup>	5.0	5.5	V
DVDD	Digital supply voltage, DVDD to GND		1.65		5.5	V
$I_{\text{A-DYNA}}$	Analog supply current, during conversion	$\text{AVDD} = 5\text{ V}$ , throughput = max		8	9	mA
$I_{\text{A-STAT}}$	Analog supply current, no conversion	$\text{AVDD} = 5\text{ V}$ , static		5	7	mA
$I_{\text{DVDD}}$	Digital supply current	$\text{DVDD} = 3.3\text{ V}$		0.25		mA
$P_{\text{D-DYNA}}$	Power dissipation	$\text{AVDD} = 5\text{ V}$ , throughput = max		40	45	mW
$P_{\text{D-STAT}}$		$\text{AVDD} = 5\text{ V}$ , static		25	35	

(1) The AVDD supply voltage defines the permissible voltage swing on the analog input pins. To use the maximum dynamic range of the analog input pins,  $V_{\text{REFIN}_x}$  and AVDD must be in the respective permissible range with  $\text{AVDD} \geq 2 \times V_{\text{REFIN}_x}$ .

(2) Specified by design; not production tested.

## 6.6 Electrical Characteristics: ADS7250

minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$ , and  $t_{\text{DATA}} = 750\text{ kSPS}$  (unless otherwise noted); typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			12			Bits
<b>DC ACCURACY</b>						
INL	Integral nonlinearity		-1	$\pm 0.5$	1	LSB
DNL	Differential nonlinearity		-0.99	$\pm 0.4$	1	LSB
$V_{\text{OS}}$	Input offset error		-2	$\pm 0.75$	2	mV
	$V_{\text{OS}}$ match	ADC_A to ADC_B	-2	$\pm 0.75$	2	mV
$dV_{\text{OS}}/dT$	Input offset thermal drift			1		$\mu\text{V}/^\circ\text{C}$
$G_{\text{ERR}}$	Gain error	Referenced to voltage at REFIN_x	-0.1%	$\pm 0.05\%$	0.1%	
	$G_{\text{ERR}}$ match	ADC_A to ADC_B	-0.1%	$\pm 0.05\%$	0.1%	
$G_{\text{ERR}}/dT$	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
<b>AC ACCURACY</b>						
SINAD	Signal-to-noise + distortion	-0.5 dBFS at 20-kHz input	71.5	72.9		dB
		-0.5 dBFS at 100-kHz input		72.9		
		-0.5 dBFS at 250-kHz input		72.5		
SNR	Signal-to-noise ratio	-0.5 dBFS at 20-kHz input	72	73		dB
		-0.5 dBFS at 100-kHz input		73		
		-0.5 dBFS at 250-kHz input		73		
THD	Total harmonic distortion	-0.5 dBFS at 20-kHz input		-90		dB
		-0.5 dBFS at 100-kHz input		-90		
		-0.5 dBFS at 250-kHz input		-82		
SFDR	Spurious-free dynamic range	-0.5 dBFS at 20-kHz input		90		dB
		-0.5 dBFS at 100-kHz input		90		
		-0.5 dBFS at 250-kHz input		82		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$ , $f_{\text{NOISE}} = 25\text{ kHz}$		-85		dB
$BW_{(\text{FP})}$	Full-power bandwidth	At -3 dB		25		MHz
		At -0.1 dB		5		

## 6.7 Electrical Characteristics: ADS7850

minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$ , and  $t_{\text{DATA}} = 750\text{ kSPS}$  (unless otherwise noted); typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			14			Bits
<b>DC ACCURACY</b>						
INL	Integral nonlinearity		-1.5	$\pm 0.8$	1.5	LSB
DNL	Differential nonlinearity		-0.99	$\pm 0.7$	1	LSB
$V_{\text{OS}}$	Input offset error		-1	$\pm 0.25$	1	mV
	$V_{\text{OS}}$ match	ADC_A to ADC_B	-1	$\pm 0.25$	1	mV
$dV_{\text{OS}}/dT$	Input offset thermal drift			1		$\mu\text{V}/^\circ\text{C}$
$G_{\text{ERR}}$	Gain error	Referenced to voltage at REFIN_x	-0.1%	$\pm 0.05\%$	0.1%	
	$G_{\text{ERR}}$ match	ADC_A to ADC_B	-0.1%	$\pm 0.05\%$	0.1%	
$G_{\text{ERR}}/dT$	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
<b>AC ACCURACY</b>						
SINAD	Signal-to-noise + distortion	-0.5 dBFS at 20-kHz input	79	81		dB
		-0.5 dBFS at 100-kHz input		81		
		-0.5 dBFS at 250-kHz input		79.9		
SNR	Signal-to-noise ratio	-0.5 dBFS at 20-kHz input	79.5	81.5		dB
		-0.5 dBFS at 100-kHz input		81.5		
		-0.5 dBFS at 250-kHz input		81		
THD	Total harmonic distortion	-0.5 dBFS at 20-kHz input		-90		dB
		-0.5 dBFS at 100-kHz input		-90		
		-0.5 dBFS at 250-kHz input		-86		
SFDR	Spurious-free dynamic range	-0.5 dBFS at 20-kHz input		90		dB
		-0.5 dBFS at 100-kHz input		90		
		-0.5 dBFS at 250-kHz input		86		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$ , $f_{\text{NOISE}} = 25\text{ kHz}$		-90		dB
$BW_{(\text{FP})}$	Full-power bandwidth	At -3 dB		25		MHz
		At -0.1 dB		5		

## 6.8 Electrical Characteristics: ADS8350

minimum and maximum specifications are at  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$ , and  $t_{\text{DATA}} = 750\text{ kSPS}$  (unless otherwise noted); typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ , and  $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RESOLUTION</b>						
Resolution			16			Bits
<b>DC ACCURACY</b>						
INL	Integral nonlinearity		-2.5	$\pm 1$	2.5	LSB
DNL	Differential nonlinearity		-0.99	$\pm 0.7$	2	LSB
$V_{\text{OS}}$	Input offset error		-1	$\pm 0.25$	1	mV
	$V_{\text{OS}}$ match	ADC_A to ADC_B	-1	$\pm 0.25$	1	mV
$dV_{\text{OS}}/dT$	Input offset thermal drift			1		$\mu\text{V}/^\circ\text{C}$
$G_{\text{ERR}}$	Gain error	Referenced to voltage at REFIN_x	-0.1%	$\pm 0.05\%$	0.1%	
	$G_{\text{ERR}}$ match	ADC_A to ADC_B	-0.1%	$\pm 0.05\%$	0.1%	
$G_{\text{ERR}}/dT$	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
<b>AC ACCURACY</b>						
SINAD	Signal-to-noise + distortion	-0.5 dBFS at 20-kHz input	83.5	84.7		dB
		-0.5 dBFS at 100-kHz input		83.7		
		-0.5 dBFS at 250-kHz input		83		
SNR	Signal-to-noise ratio	-0.5 dBFS at 20-kHz input	84	85		dB
		-0.5 dBFS at 100-kHz input		84.8		
		-0.5 dBFS at 250-kHz input		84		
THD	Total harmonic distortion	-0.5 dBFS at 20-kHz input		-96		dB
		-0.5 dBFS at 100-kHz input		-90		
		-0.5 dBFS at 250-kHz input		-90		
SFDR	Spurious-free dynamic range	-0.5 dBFS at 20-kHz input		96		dB
		-0.5 dBFS at 100-kHz input		90		
		-0.5 dBFS at 250-kHz input		90		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$ , $f_{\text{NOISE}} = 25\text{ kHz}$		-90		dB
$BW_{(\text{FP})}$	Full-power bandwidth	At -3 dB		25		MHz
		At -0.1 dB		5		



### 6.9 Timing Requirements

		MIN	NOM	MAX	UNIT
$f_{\text{THROUGHPUT}}$	Sample taken to data read	$f_{\text{CLK}} = \text{max}$		750	kSPS
		$f_{\text{CLK}} = \text{max}$	1.33		$\mu\text{s}$
$f_{\text{CLK}}$	CLOCK frequency			24	MHz
$t_{\text{CLK}}$	CLOCK period			41.66	ns
$t_{\text{PH\_CK}}$	CLOCK high time	0.4		0.6	$t_{\text{CLK}}$
$t_{\text{PL\_CK}}$	CLOCK low time	0.4		0.6	$t_{\text{CLK}}$
$t_{\text{ACQ}}$	Acquisition time	ADS8350, $f_{\text{CLK}} = \text{max}$	120		ns
		ADS7850, $f_{\text{CLK}} = \text{max}$	100		
		ADS7250, $f_{\text{CLK}} = \text{max}$	70		
$t_{\text{PH\_CS}}$	$\overline{\text{CS}}$ high time	20			ns
$t_{\text{PH\_CS\_SHRT}}$	$\overline{\text{CS}}$ high time after frame abort	ADS8350	120		ns
		ADS7850	100		
		ADS7250	70		
$t_{\text{D\_CKCS}}$	Delay time from last SCLK falling to $\overline{\text{CS}}$ rising	15			ns
$t_{\text{SU\_CSCK}}$	Setup time from $\overline{\text{CS}}$ falling to SCLK falling	15			ns

### 6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{CONV}}$	Conversion time			590	ns
$t_{\text{DV\_CSDO}}$	Delay time from $\overline{\text{CS}}$ falling to data enable			12	ns
$t_{\text{DZ\_CSDO}}$	Delay time from $\overline{\text{CS}}$ rising to DOUT going to 3-state			10	ns
$t_{\text{D\_CKDO}}$	Delay time from SCLK falling to (next) data valid on SDO	3		20	ns

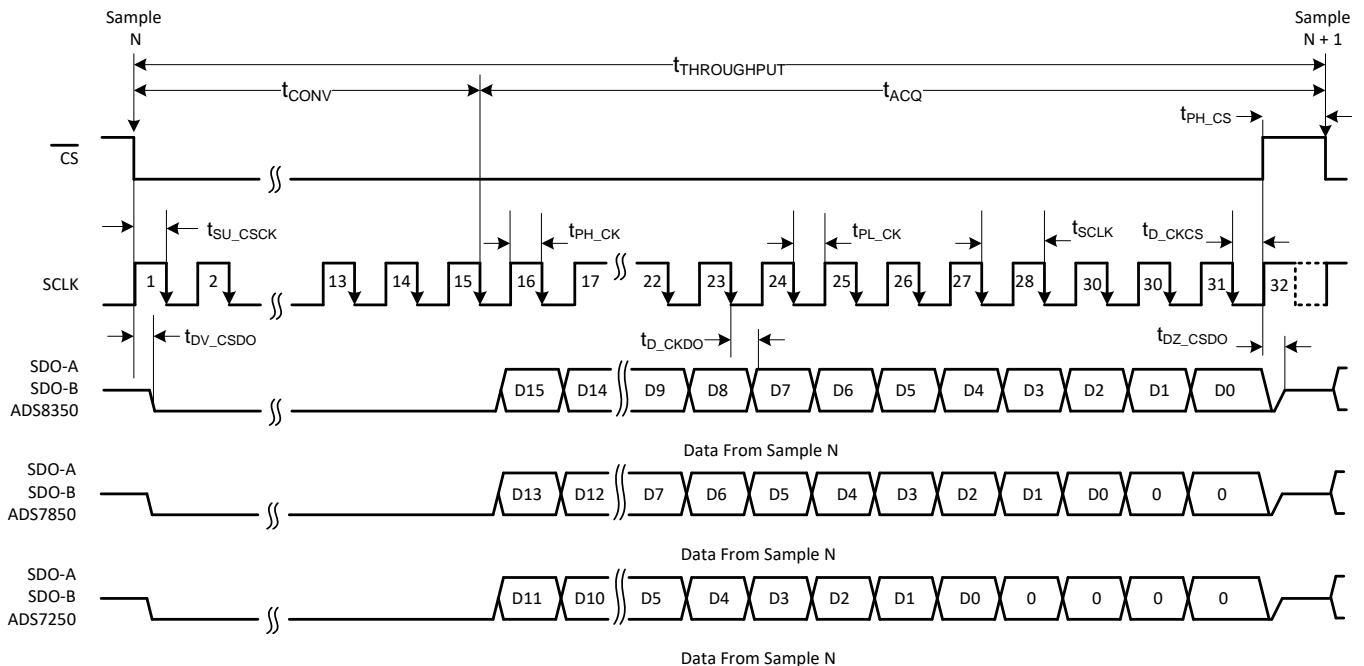
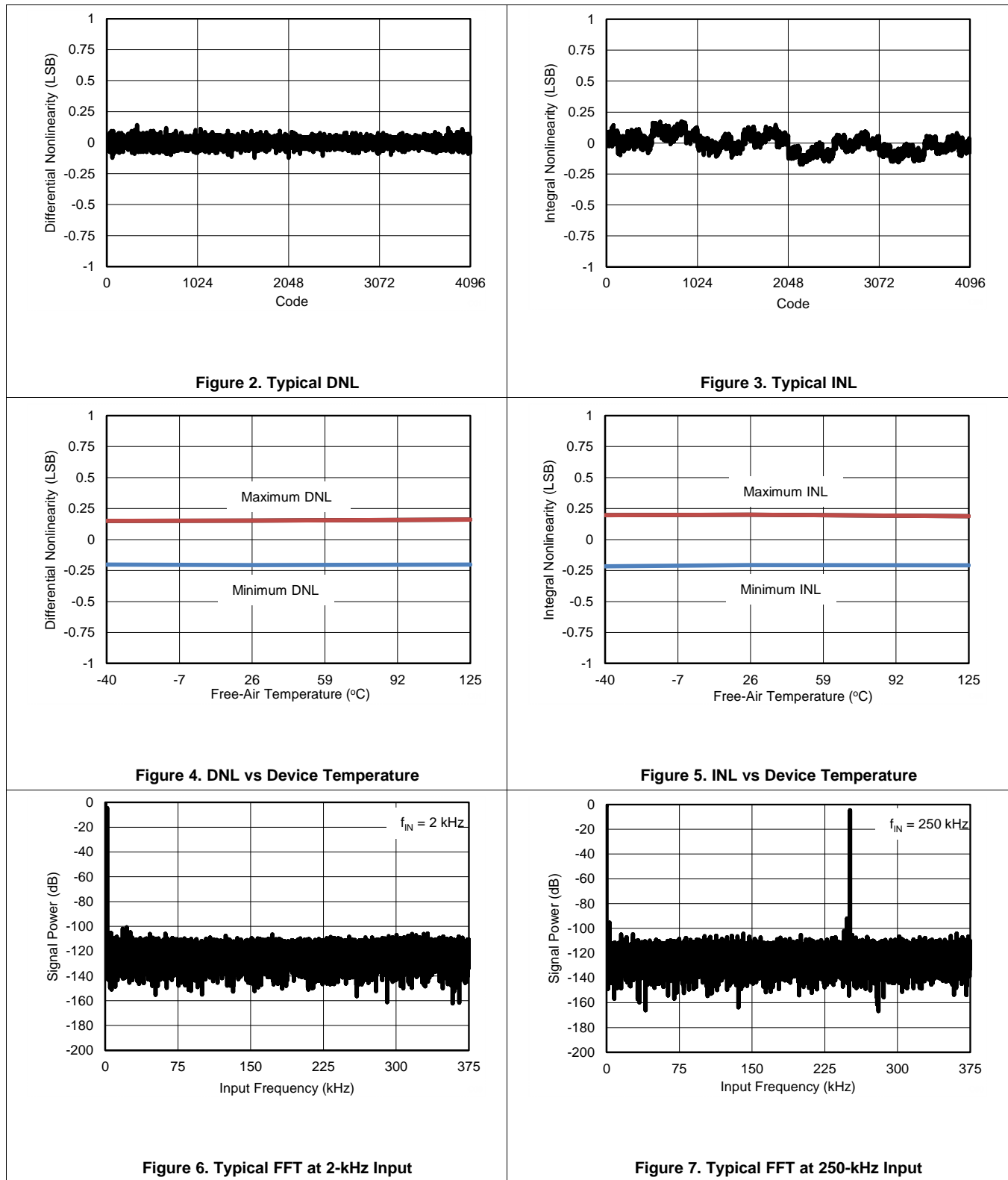


Figure 1. Timing Diagram

### 6.11 Typical Characteristics: ADS7250

at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = 5\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)



Typical Characteristics: ADS7250 (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)

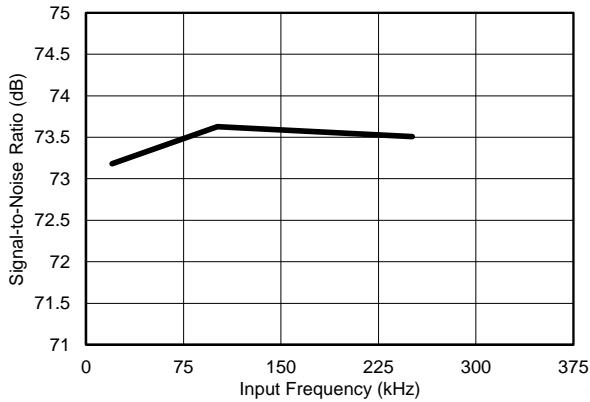


Figure 8. SNR vs Input Frequency

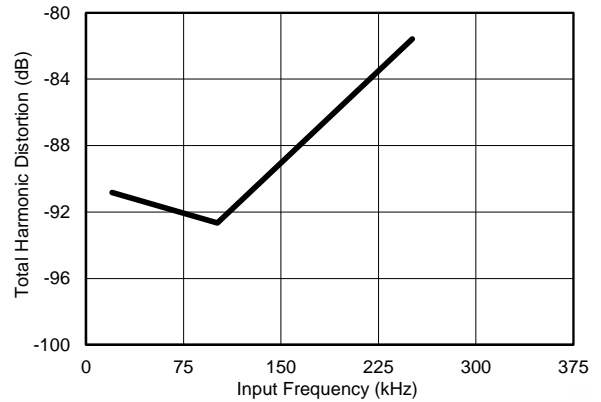


Figure 9. THD vs Input Frequency

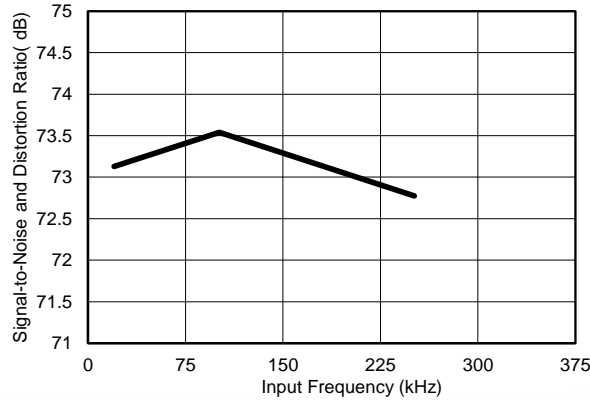


Figure 10. SINAD vs Input Frequency

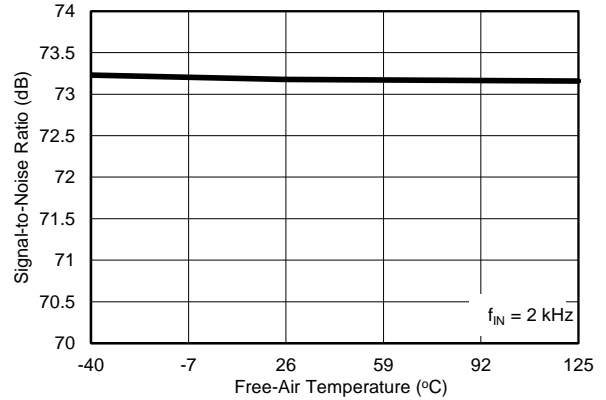


Figure 11. SNR vs Device Temperature

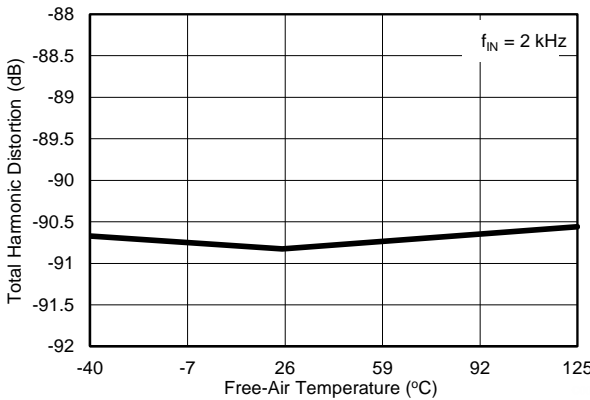


Figure 12. THD vs Device Temperature

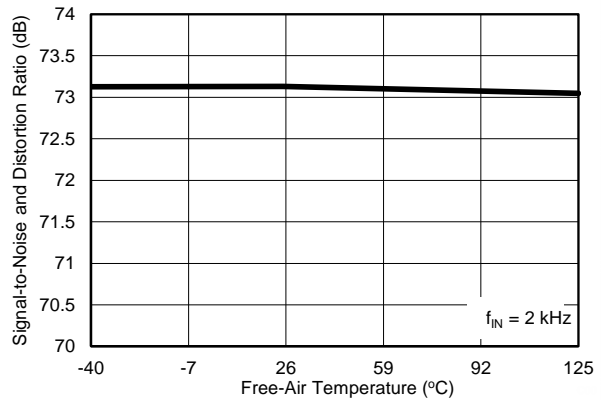
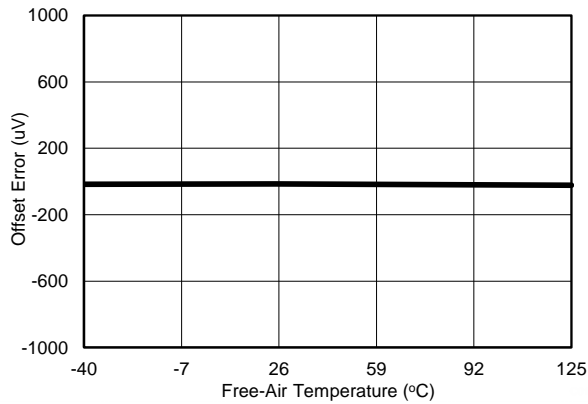


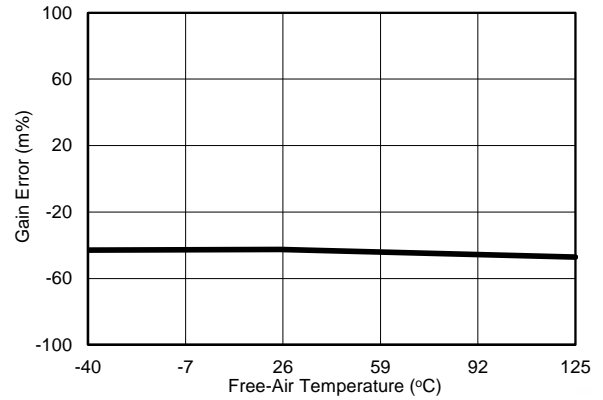
Figure 13. SINAD vs Device Temperature

**Typical Characteristics: ADS7250 (continued)**

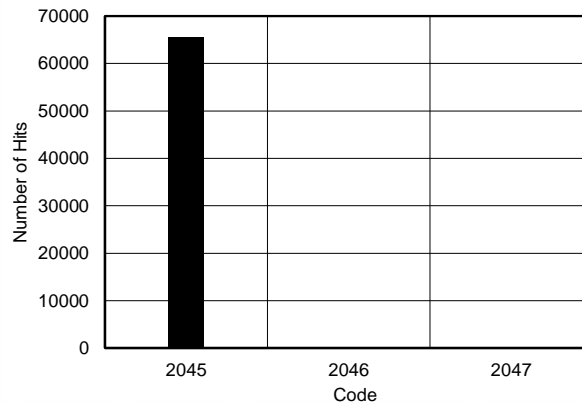
at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)



**Figure 14. Offset Error vs Device Temperature**



**Figure 15. Gain Error vs Device Temperature**



**Figure 16. DC Histogram**

## 6.12 Typical Characteristics: ADS7850

at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = 5\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)

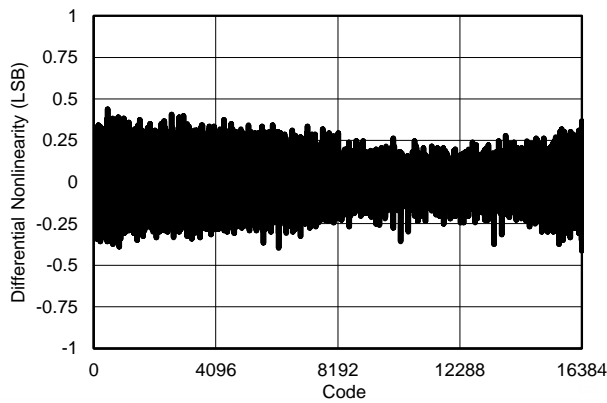


Figure 17. Typical DNL

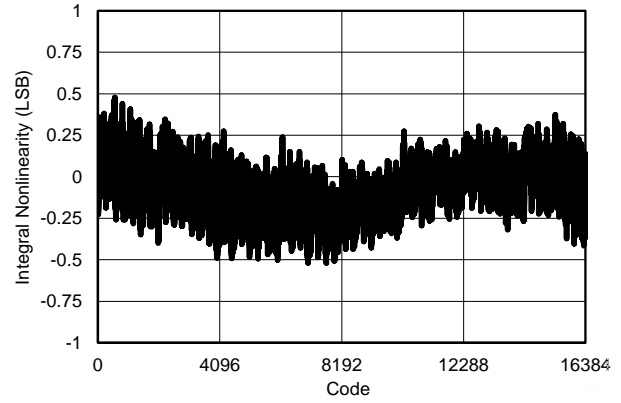


Figure 18. Typical INL

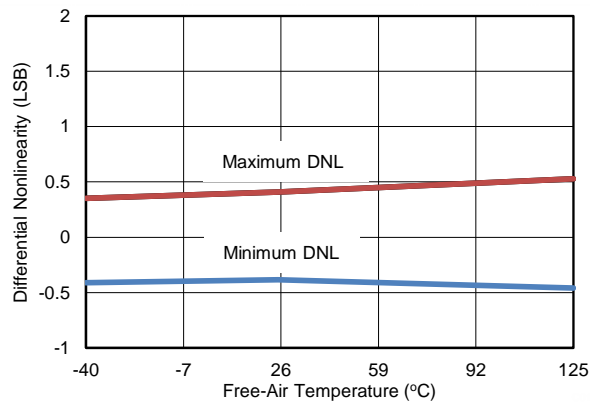


Figure 19. DNL vs Device Temperature

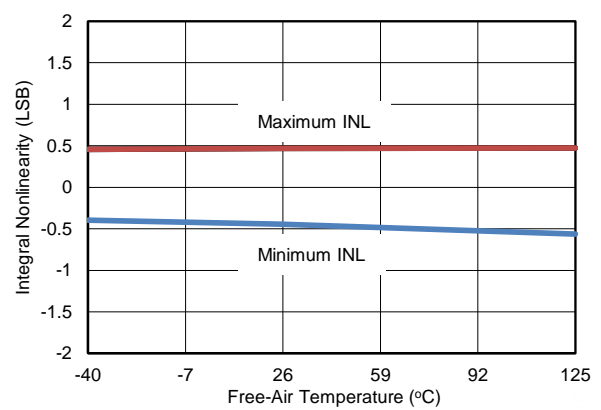


Figure 20. INL vs Device Temperature

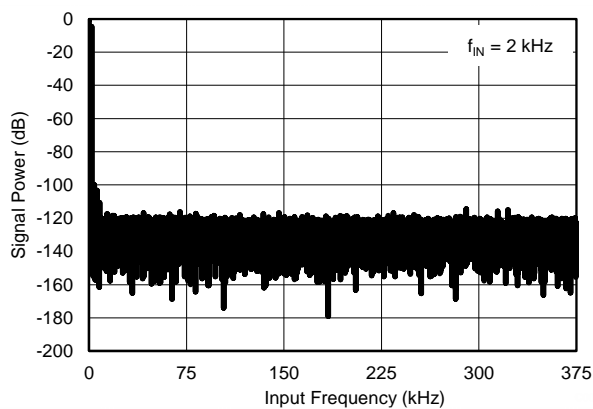


Figure 21. Typical FFT at 2-kHz Input

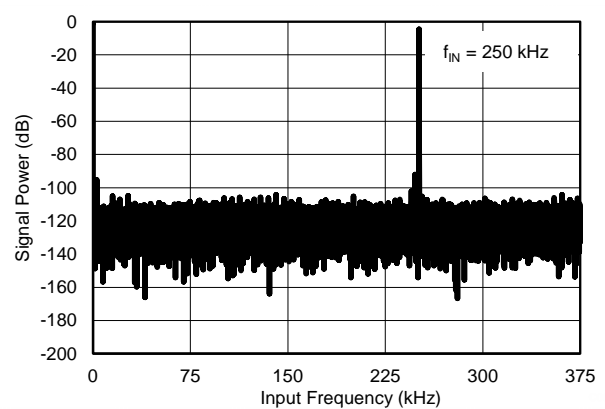


Figure 22. Typical FFT at 250-kHz Input

**Typical Characteristics: ADS7850 (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)

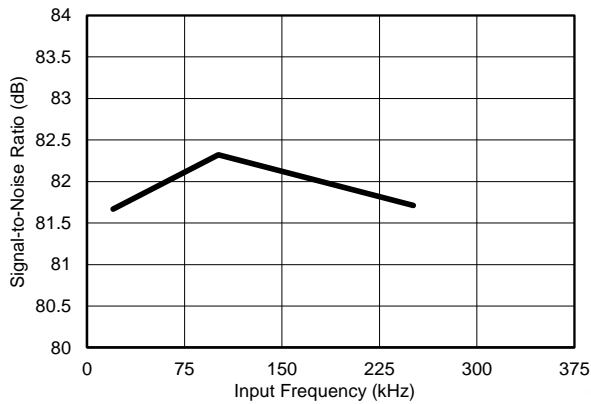


Figure 23. SNR vs Input Frequency

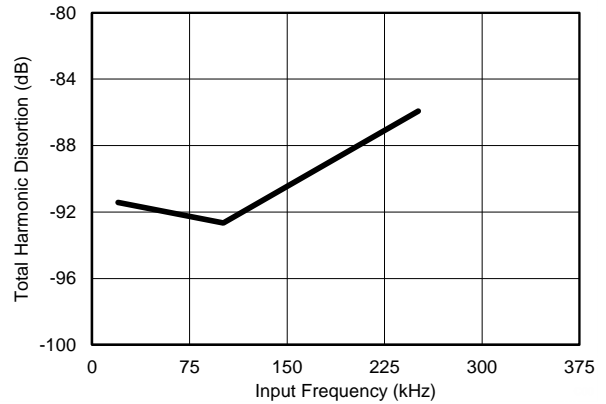


Figure 24. THD vs Input Frequency

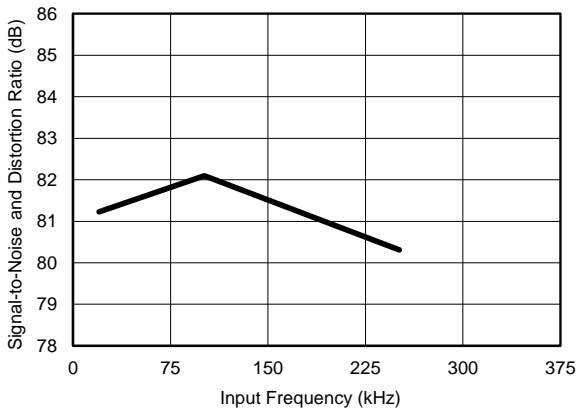


Figure 25. SINAD vs Input Frequency

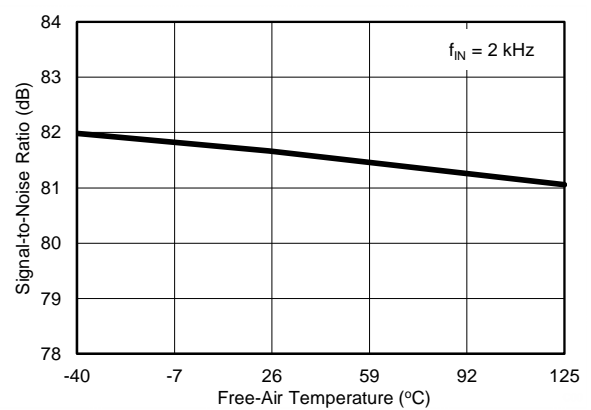


Figure 26. SNR vs Device Temperature

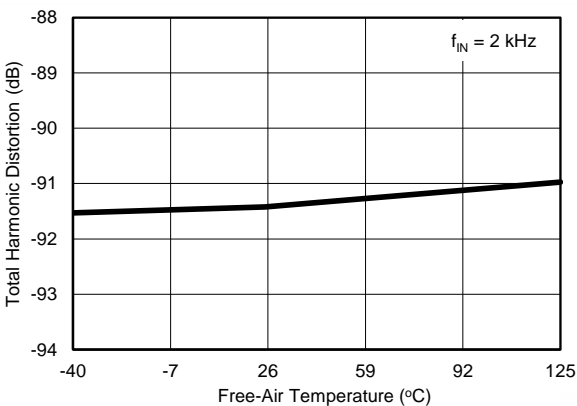


Figure 27. THD vs Device Temperature

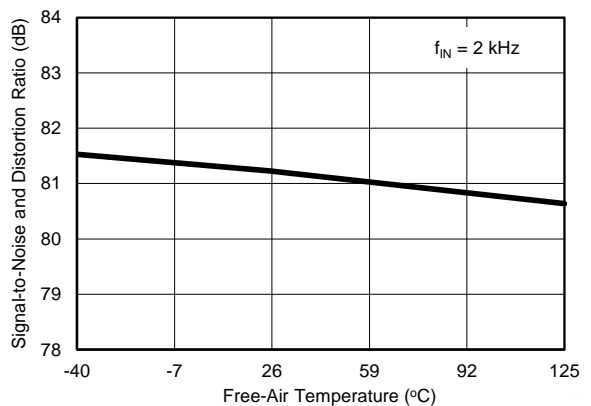
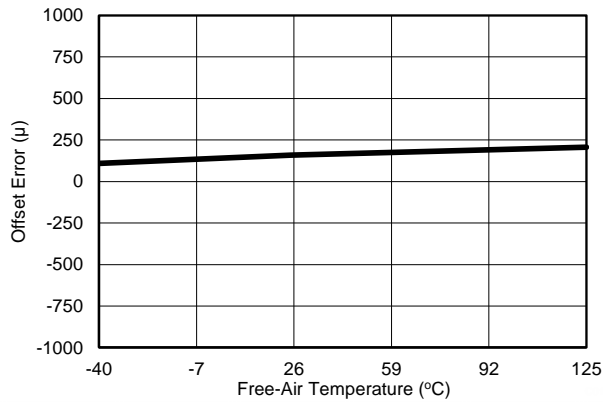


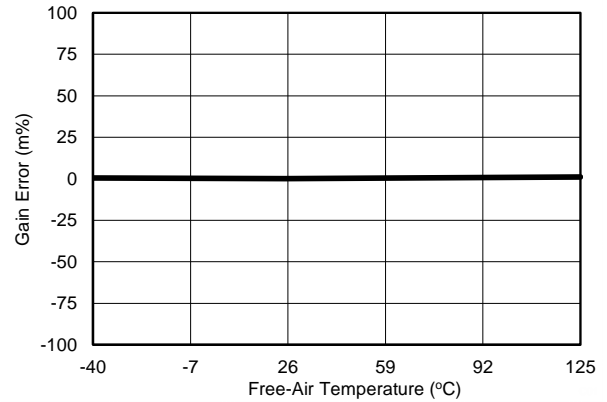
Figure 28. SINAD vs Device Temperature

**Typical Characteristics: ADS7850 (continued)**

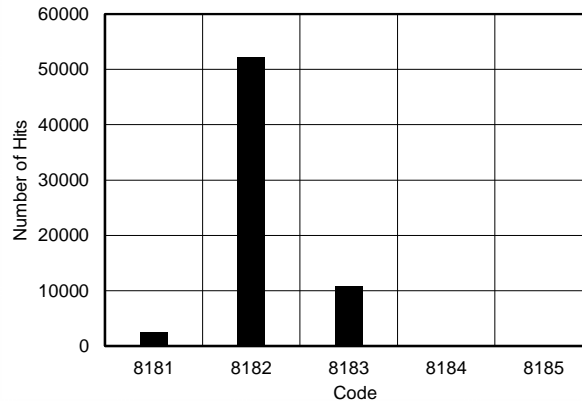
at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)



**Figure 29. Offset Error vs Device Temperature**



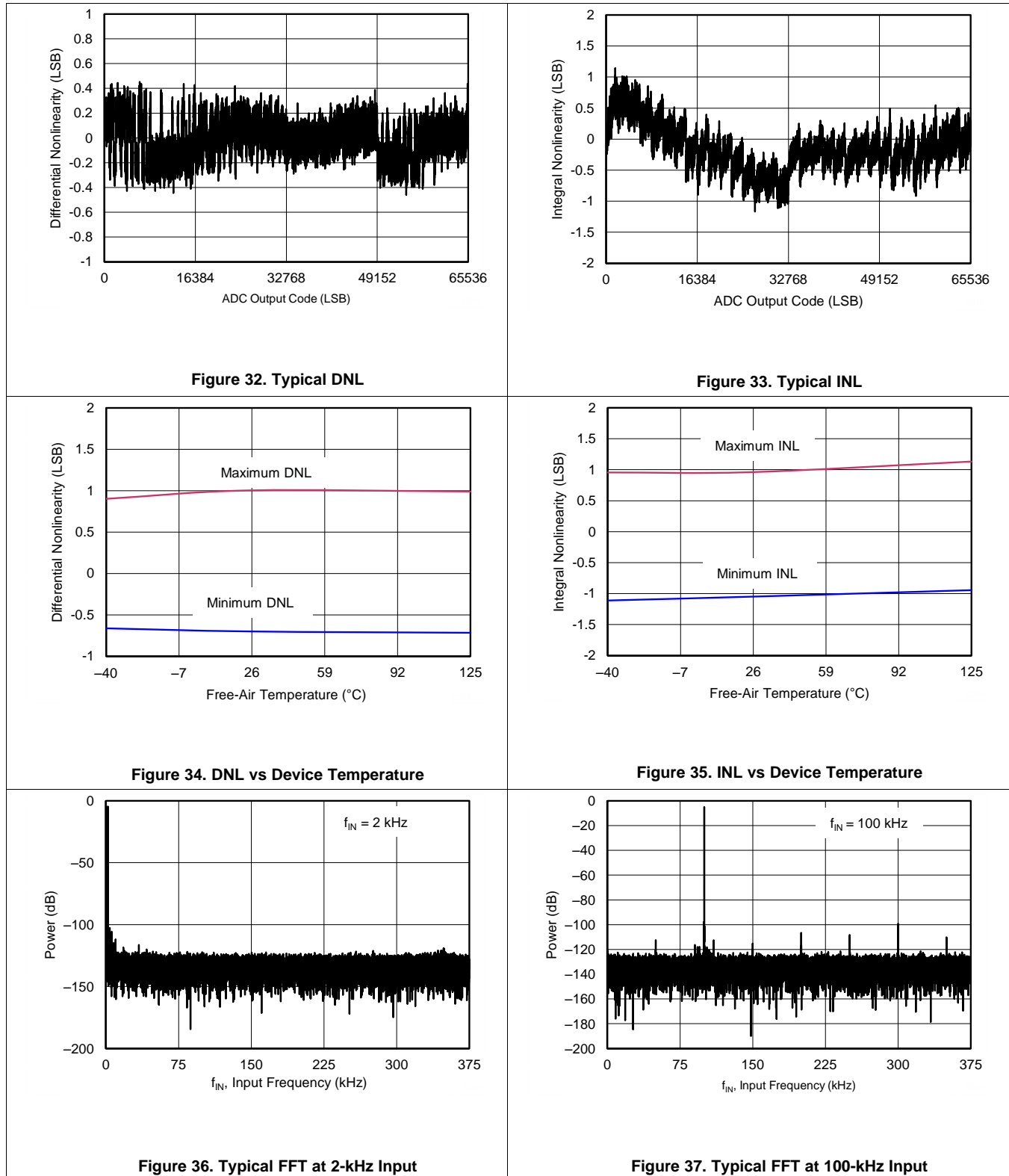
**Figure 30. Gain Error vs Device Temperature**



**Figure 31. DC Histogram**

### 6.13 Typical Characteristics: ADS8350

at  $T_A = 25^\circ\text{C}$ ,  $AV_{DD} = 5\text{ V}$ ,  $DV_{DD} = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)





Typical Characteristics: ADS8350 (continued)

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)

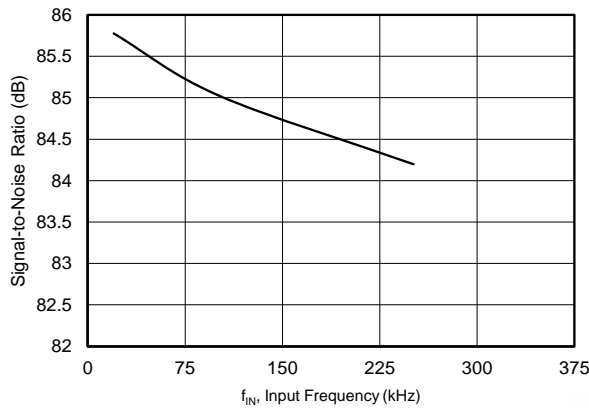


Figure 38. SNR vs Input Frequency

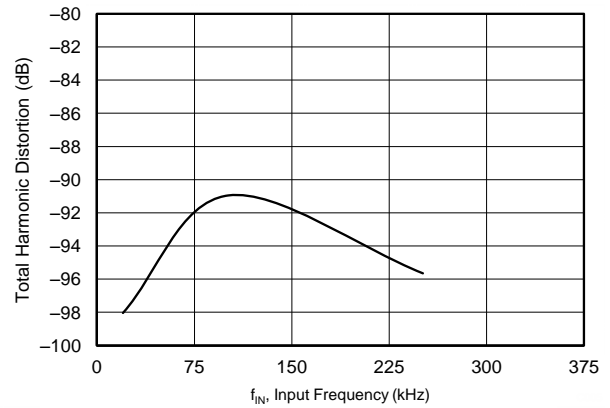


Figure 39. THD vs Input Frequency

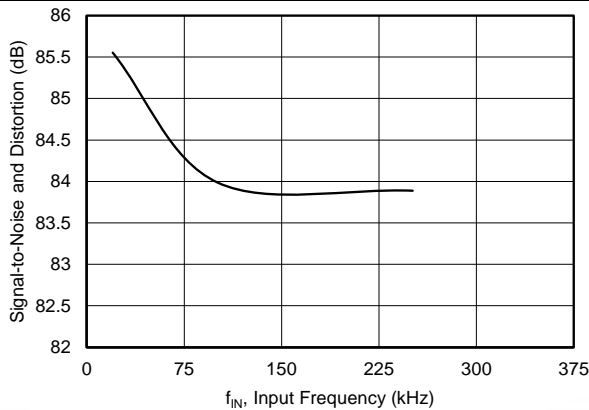


Figure 40. SINAD vs Input Frequency

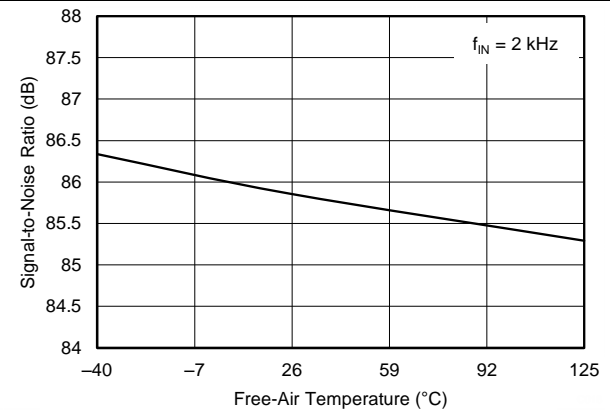


Figure 41. SNR vs Device Temperature

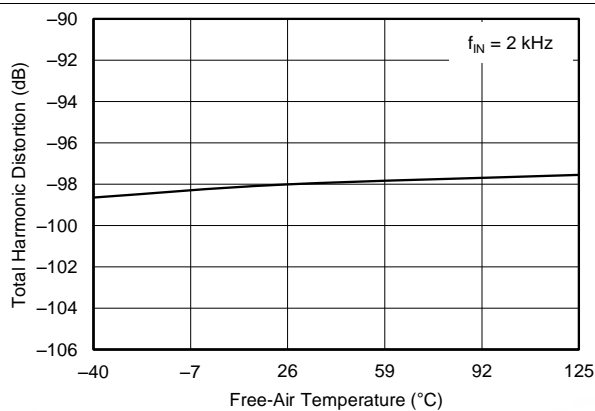


Figure 42. THD vs Device Temperature

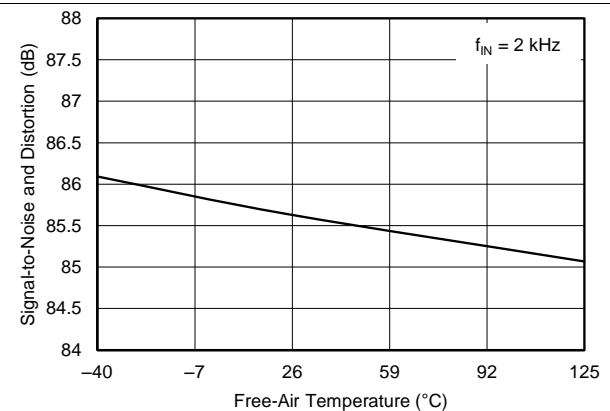
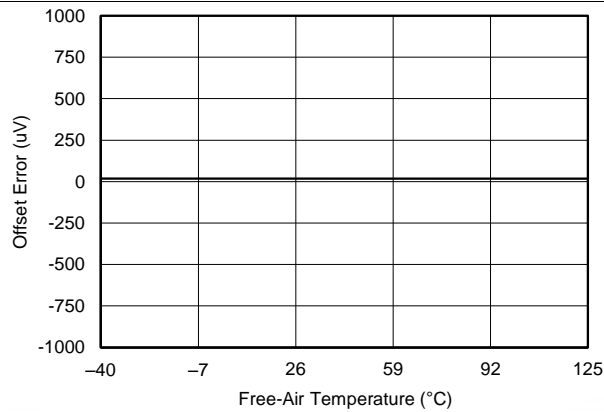


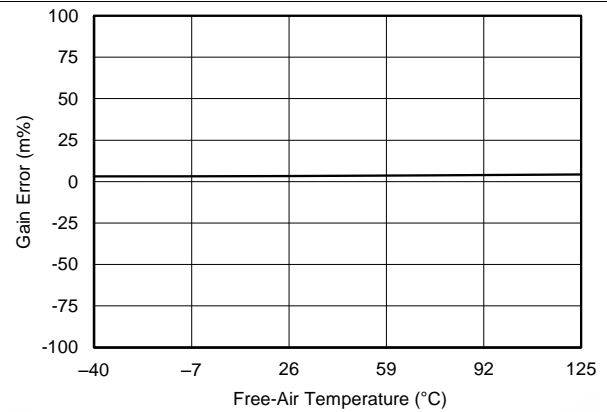
Figure 43. SINAD vs Device Temperature

**Typical Characteristics: ADS8350 (continued)**

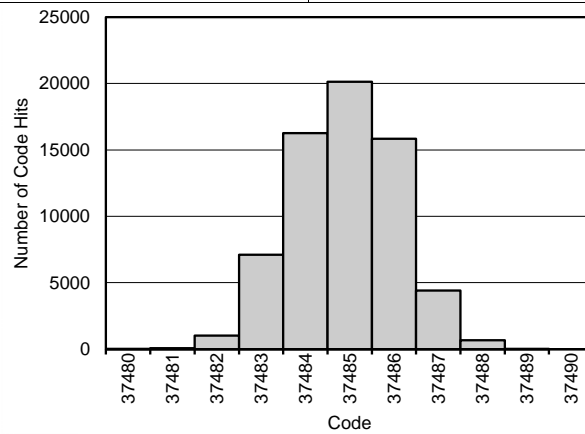
at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)



**Figure 44. Offset Error vs Device Temperature**



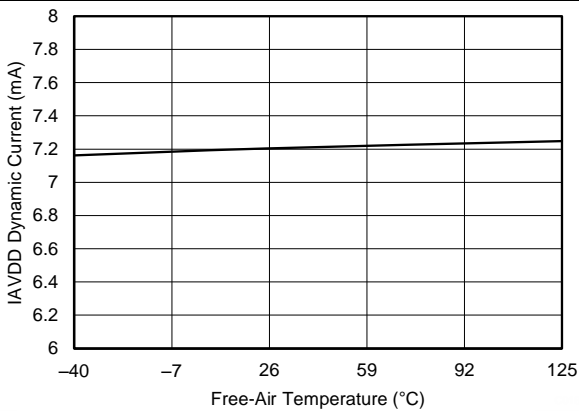
**Figure 45. Gain Error vs Device Temperature**



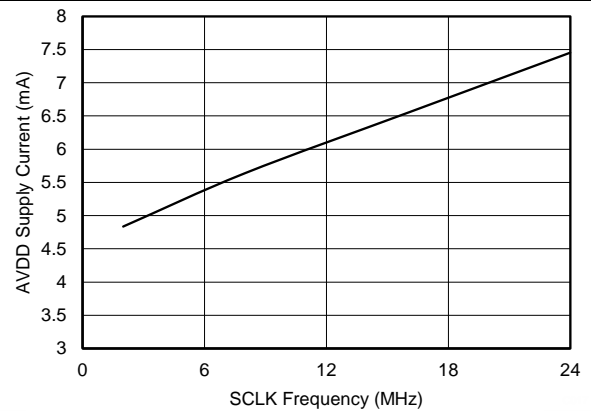
**Figure 46. DC Histogram**

### 6.14 Typical Characteristics: All Devices

at  $T_A = 25^\circ\text{C}$ ,  $AVDD = 5\text{ V}$ ,  $DVDD = 3.3\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$ , and  $f_{DATA} = 750\text{ kSPS}$  (unless otherwise noted)



**Figure 47. Dynamic Current vs Device Temperature**



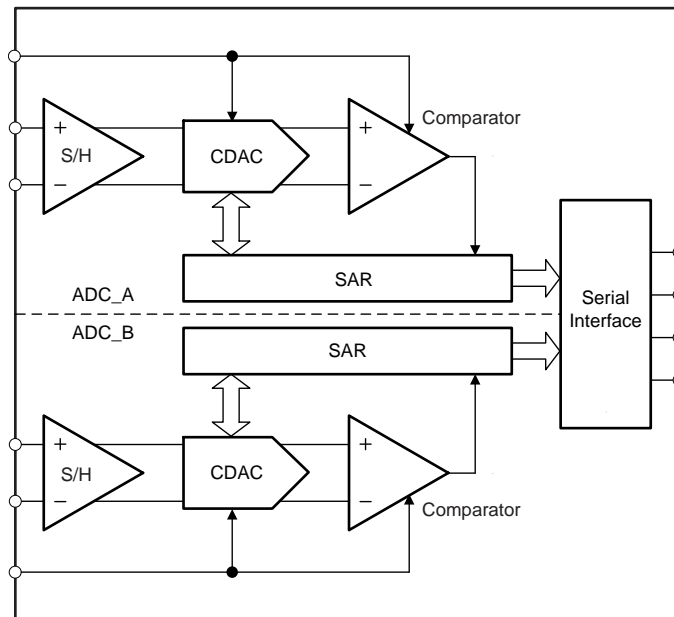
**Figure 48. Supply Current vs SCLK Frequency**

## 7 Detailed Description

### 7.1 Overview

The ADS8350, ADS7850, and ADS7250 belong to a family of dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The devices support pseudo-differential input signals with the input common-mode equal to the reference voltage and the full-scale input range equal to twice the reference voltage. The devices provide a simple serial interface to the host controller and operate over a wide range of digital power supplies.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Reference

Each device has two simultaneous-sampling ADCs (ADC\_A and ADC\_B). ADC\_A operates with reference voltage  $V_{REFIN\_A}$  and ADC\_B operates with reference voltage  $V_{REFIN\_B}$ . These reference voltages must be provided on the REFIN\_A and REFIN\_B pins, respectively. REFIN\_A and REFIN\_B may be set to different values as per the application requirement.

As shown in Figure 49, decouple the REFIN\_A and REFIN\_B pins with the REFGND\_A and REFGND\_B pins, respectively, with individual 10- $\mu$ F decoupling capacitors.

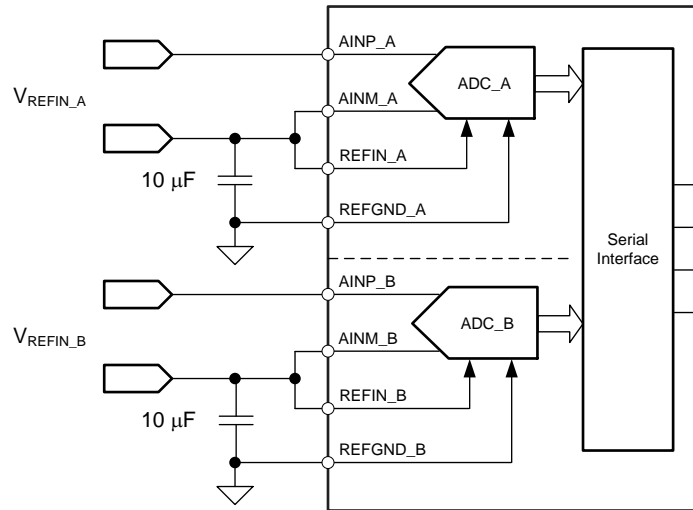


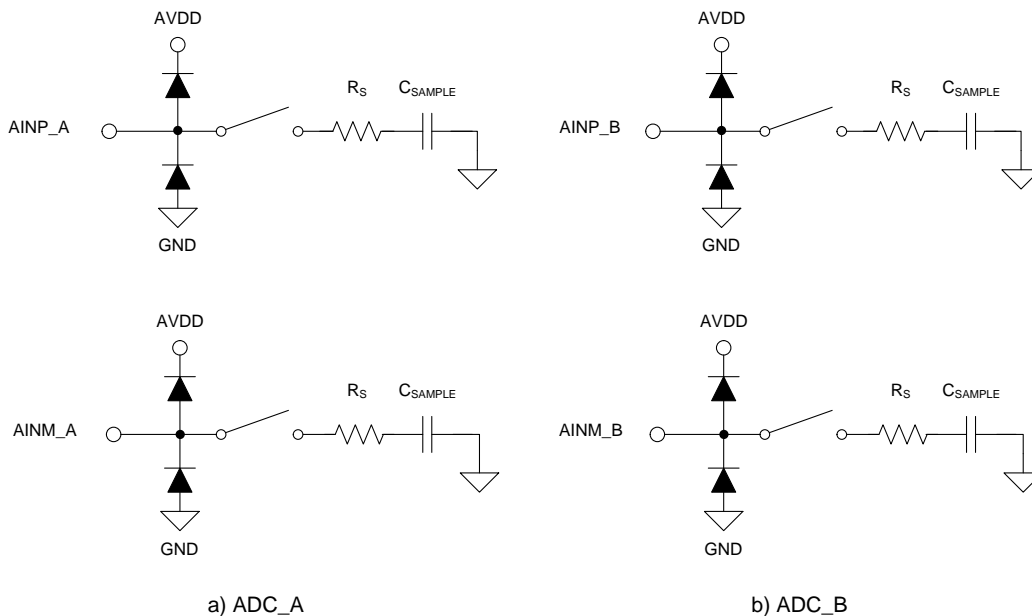
Figure 49. Reference Block Diagram

## Feature Description (continued)

### 7.3.2 Analog Input

The devices support pseudo-differential analog input signals. These inputs are sampled and converted simultaneously by the two ADCs (ADC\_A and ADC\_B). ADC\_A samples and converts ( $V_{AINP\_A} - V_{AINM\_A}$ ), and ADC\_B samples and converts ( $V_{AINP\_B} - V_{AINM\_B}$ ).

Figure 50a and Figure 50b show equivalent circuits for the ADC\_A and ADC\_B analog input pins, respectively.  $R_S$  (typically 50  $\Omega$ ) represents the on-state sampling switch resistance, and  $C_{SAMPLE}$  represents the device sampling capacitor (typically 40 pF).



**Figure 50. Equivalent Circuit for Analog Input Pins**

#### 7.3.2.1 Analog Input Full-Scale Range

The analog input full-scale range (FSR) for ADC\_A and ADC\_B is twice the reference voltage provided to the particular ADC. By providing different reference voltages ( $V_{REFIN\_A}$  and  $V_{REFIN\_B}$ ), ADC\_A and ADC\_B can have different full-scale input ranges. Therefore, the FSR for ADC\_A and ADC\_B can be determined by Equation 1 and Equation 2, respectively:

$$FSR\_ADC\_A = 2 \times V_{REFIN\_A} \quad (1)$$

$$V_{AINP\_A} = 0 \text{ to } 2 \times V_{REFIN\_A}$$

$$V_{AINM\_A} = V_{REFIN\_A}$$

The REFIN\_A and AINM\_A pins must be shorted and connected to the external reference voltage,  $V_{REFIN\_A}$ .

$$FSR\_ADC\_B = 2 \times V_{REFIN\_B} \quad (2)$$

$$V_{AINP\_B} = 0 \text{ to } 2 \times V_{REFIN\_B}$$

$$V_{AINM\_B} = V_{REFIN\_B}$$

The REFIN\_B and AINM\_B pins must be shorted and connected to the external reference voltage,  $V_{REFIN\_B}$ .

To use the full dynamic input range on the analog input pins, AVDD must be as shown in Equation 3, Equation 4, and Equation 5:

$$AVDD \geq 2 \times V_{REFIN\_A} \quad (3)$$

$$AVDD \geq 2 \times V_{REFIN\_B} \quad (4)$$

$$4.5 \text{ V} \leq AVDD \leq 5.5 \text{ V} \quad (5)$$

## Feature Description (continued)

### 7.3.3 ADC Transfer Function

The device output is in binary twos complement format. Device resolution is calculated by [Equation 6](#):

$$1 \text{ LSB} = (\text{FSR\_ADC\_x}) / (2^N)$$

where:

- $\text{FSR\_ADC\_x} = 2 \times V_{\text{REFIN\_x}}$  and
- N is the resolution of the ADC : N = 16 for the ADS8350, N = 14 for the ADS7850, and N = 12 for the ADS7250

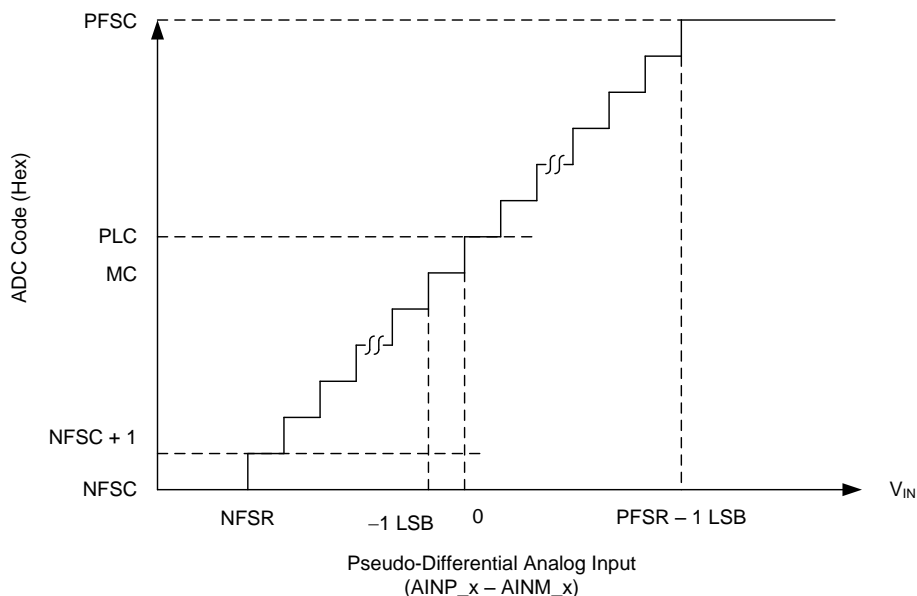
(6)

[Table 1](#) shows the different input voltages and the corresponding device output codes.

**Table 1. Transfer Characteristics**

INPUT VOLTAGE (AINM_x)	INPUT VOLTAGE (AINP_x)	PSEUDO-DIFFERENTIAL INPUT TO ADC (AINP_x - AINM_x)		OUTPUT CODE (HEX)			
				CODE	ADS7250	ADS7850	ADS8350
$V_{\text{REFIN\_x}}$	0	$-V_{\text{REFIN\_x}}$	NFSR	NFSC	800	2000	8000
	1 LSB	$-V_{\text{REFIN\_x}} + 1 \text{ LSB}$	$\text{NFSR} + 1 \text{ LSB}$	$\text{NFSC} + 1$	801	2001	8001
	$V_{\text{REFIN\_x}} - 1 \text{ LSB}$	-1 LSB	-1 LSB	MC	FFF	3FFF	FFFF
	$V_{\text{REFIN\_x}}$	0	0	PLC	000	0000	0000
	$2 \times V_{\text{REFIN\_x}} - 1 \text{ LSB}$	$V_{\text{REFIN\_x}} - 1 \text{ LSB}$	$\text{PFSR} - 1 \text{ LSB}$	PFSC	7FF	1FFF	7FFF

[Figure 51](#) shows the ideal transfer characteristics for the device.

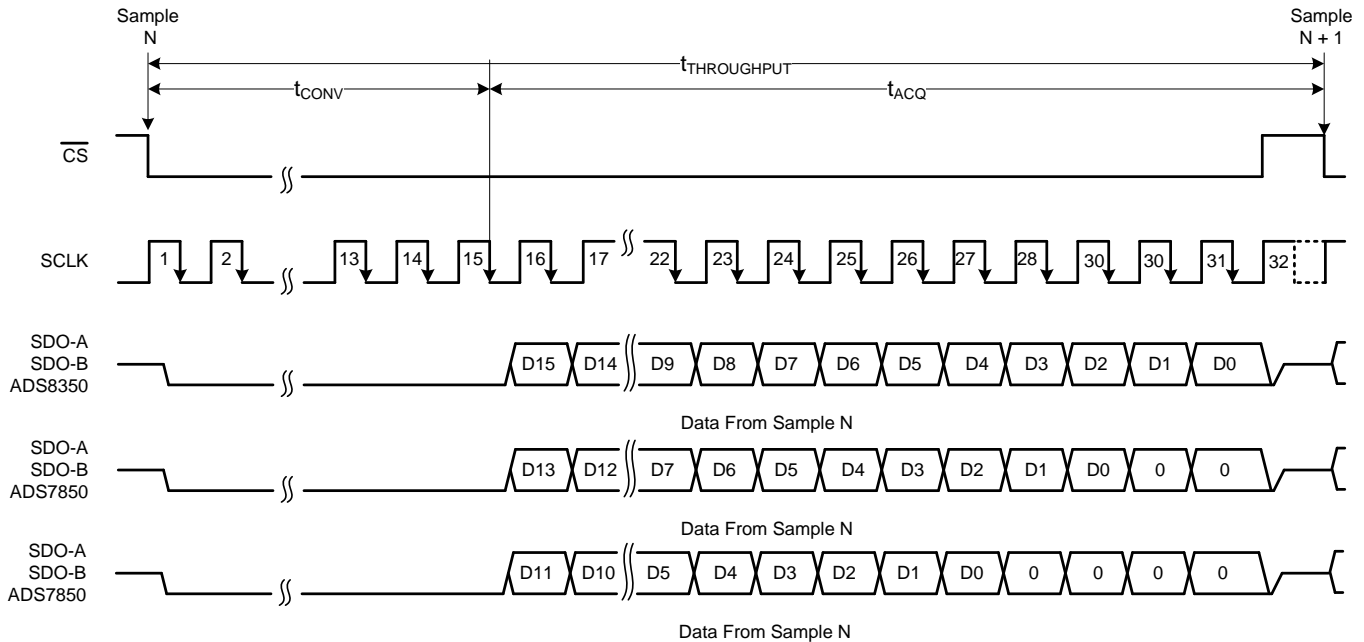


**Figure 51. Ideal Transfer Characteristics**

## 7.4 Device Functional Modes

### 7.4.1 Serial Interface

The devices support a simple, SPI-compatible serial interface to the external digital host. The  $\overline{CS}$  signal defines one conversion and serial transfer frame. A frame starts with a  $\overline{CS}$  falling edge and ends with a  $\overline{CS}$  rising edge. The SDO\_A and SDO\_B pins output the ADC\_A and ADC\_B conversion results, respectively. Figure 52 shows a detailed timing diagram for these devices.



**Figure 52. Serial Interface Timing Diagram**

A  $\overline{CS}$  falling edge brings the serial data bus out of 3-state and also outputs a '0' on the SDO\_A and SDO\_B pins. The device converts the sampled analog input during the next 14 clocks. SDO\_A and SDO\_B read '0' during this period. The sample-and-hold circuit goes back into sample mode on the 15th SCLK falling edge and the MSBs of ADC\_A and ADC\_B are output on SDO\_A and SDO\_B, respectively. The subsequent clock edges are used to shift out the conversion result using the serial interface, as shown in Table 2. Output data are in binary two's complement format. A  $\overline{CS}$  rising edge ends the frame and puts the serial bus into 3-state.

**Table 2. Data Launch Edge**

DEVICE	PIN	LAUNCH EDGE													
		$\overline{CS} \downarrow$	SCLK											$\overline{CS} \uparrow$	
			$\downarrow 1$	...	$\downarrow 14$	$\downarrow 15$	...	$\downarrow 26$	$\downarrow 27$	$\downarrow 28$	$\downarrow 29$	$\downarrow 30$	$\downarrow 31$		...
ADS8350	SDO-A	0	0	...	0	D15_A	...	D4_A	D3_A	D2_A	D1_A	D0_A	0	...	Hi-Z
	SDO-B	0	0	...	0	D15_B	...	D4_B	D3_B	D2_B	D1_B	D0_B	0	...	Hi-Z
ADS7850	SDO-A	0	0	...	0	D13_A	...	D2_A	D1_A	D0_A	0	0	0	...	Hi-Z
	SDO-B	0	0	...	0	D13_B	...	D2_B	D1_B	D0_B	0	0	0	...	Hi-Z
ADS7250	SDO-A	0	0	...	0	D11_A	...	D0_A	0	0	0	0	0	...	Hi-Z
	SDO-B	0	0	...	0	D11_B	...	D0_B	0	0	0	0	0	...	Hi-Z



### 7.4.2 Short-Cycling, Frame Abort, and Reconversion Feature

Referring to Table 2, the ADS8350 requires a minimum of 31 SCLK falling edges between the beginning and end of the frame to complete the 16-bit data transfer, the ADS7850 requires a minimum of 29 SCLK falling edges between the beginning and end of the frame to complete the 14-bit data transfer, and the ADS7250 requires a minimum of 27 SCLK falling edges between the beginning and end of the frame to complete the 12-bit data transfer. However,  $\overline{\text{CS}}$  can be brought high at any time during the frame to abort the frame or to *short-cycle* the converter.

As shown in Figure 53, if  $\overline{\text{CS}}$  is brought high before the 15th SCLK falling edge, the device aborts the conversion and starts sampling the new analog input signal.

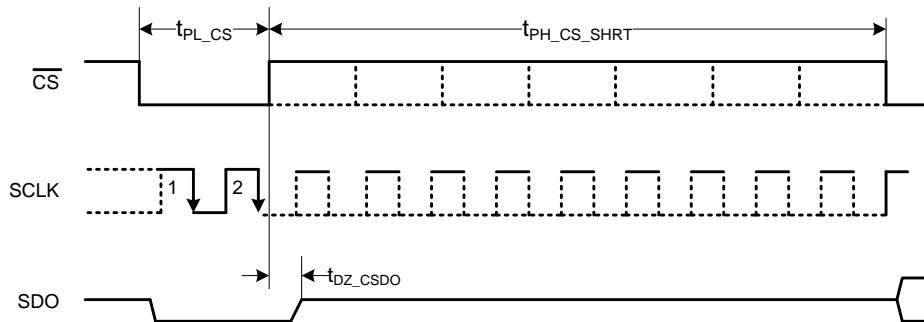


Figure 53. Frame Aborted before 15th SCLK Falling Edge

If  $\overline{\text{CS}}$  is brought high after the 15th SCLK falling edge (as shown in Figure 54), the output data bits latched into the digital host before this  $\overline{\text{CS}}$  rising edge are still valid data corresponding to sample N.

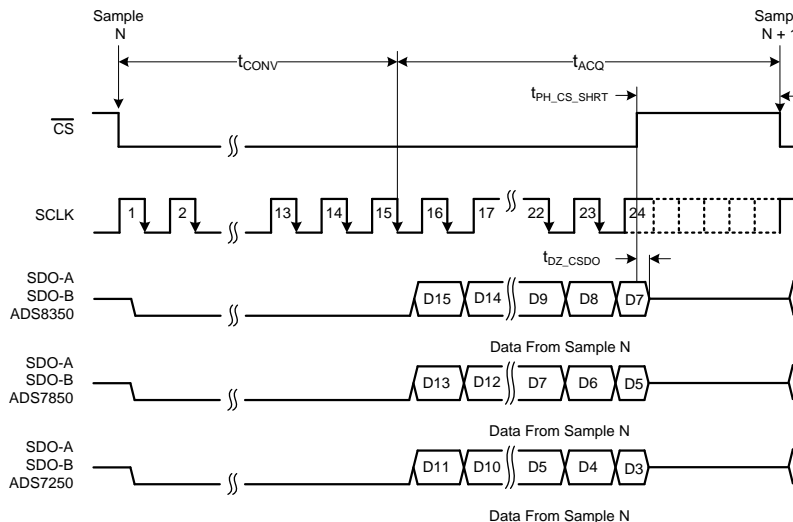


Figure 54. Frame Aborted after 15th SCLK Falling Edge

After aborting the current frame,  $\overline{\text{CS}}$  must be kept high for  $t_{\text{PH\_CS\_SHRT}}$  to ensure that the minimum acquisition time ( $t_{\text{ACQ}}$ ) is provided for the next conversion.

## 8 Application and Implementation

### NOTE

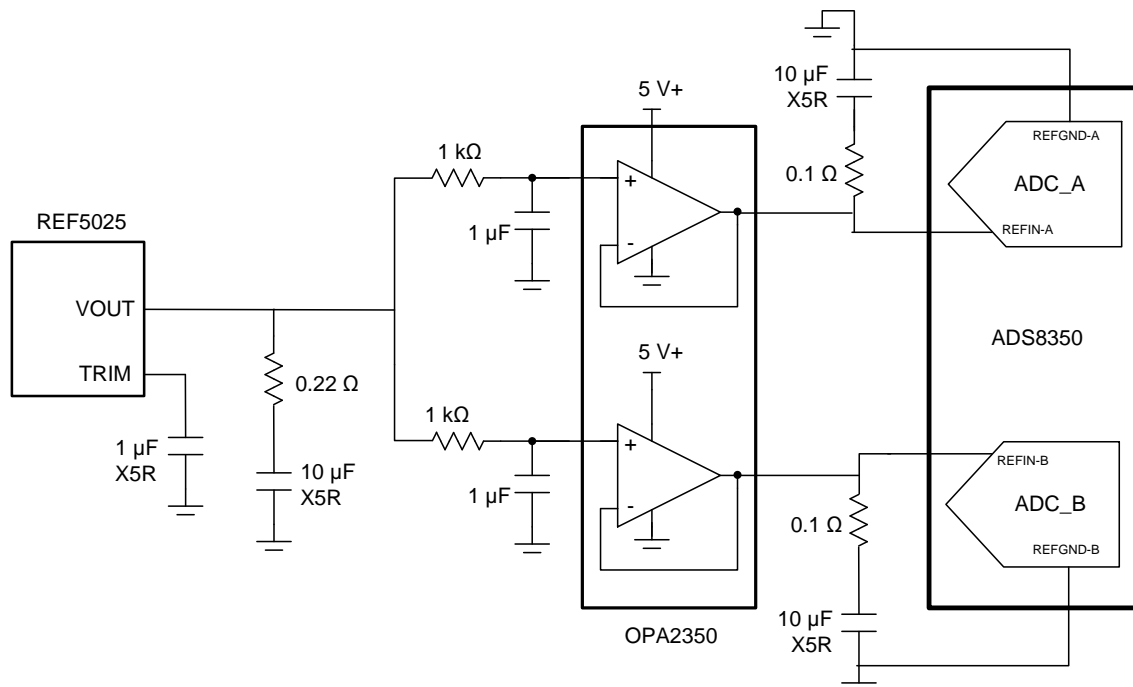
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits and provides some application circuits designed using these devices.

### 8.2 Typical Applications

#### 8.2.1 DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput



**Figure 55. Reference Drive Circuit with  $V_{REF} = 2.5\text{ V}$**

## Typical Applications (continued)

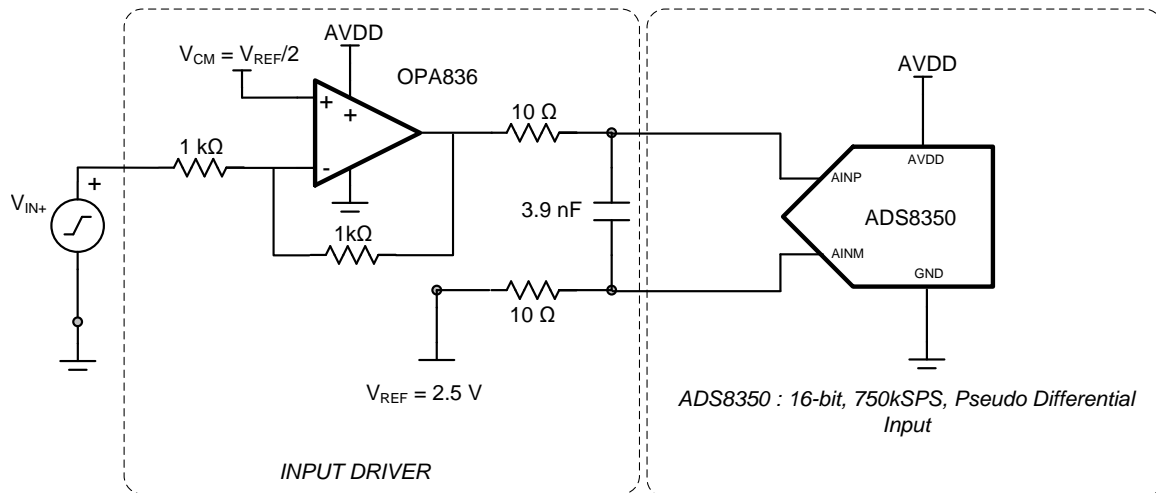


Figure 56. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput

### 8.2.1.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve > 84-dB SNR and < -90-dB THD at a 100-kHz input frequency.

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 ADC Reference Driver

The external reference source to the device must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few 100  $\mu\text{V}_{\text{RMS}}$ . Therefore, in order to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred Hertz.

After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive this large capacitor should have low output impedance, low offset, and temperature drift specifications.

To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The application circuit in [Figure 55](#) shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply.

The 2.5-V reference voltage is generated by the high-precision, low-noise [REF5025](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10  $\mu\text{F}$ . The low output impedance, low noise, and fast settling time makes the [OPA2350](#) a good choice for driving this high capacitive load.

#### 8.2.1.2.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

## Typical Applications (continued)

### 8.2.1.2.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in [Equation 7](#):

$$\text{Unity - Gain Bandwidth} \geq 4 \times \left( \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (7)$$

- **Noise.** Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in [Equation 8](#).

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left( \frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu V_{RMS}$ ,
- $e_{n\_RMS}$  is the amplifier broadband noise density in  $nV/\sqrt{Hz}$ ,
- $f_{-3dB}$  is the 3-dB bandwidth of the RC filter, and
- $N_G$  is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (8)
- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in [Equation 9](#).

$$\text{THD}_{AMP} \leq \text{THD}_{ADC} - 10 \text{ (dB)} \quad (9)$$

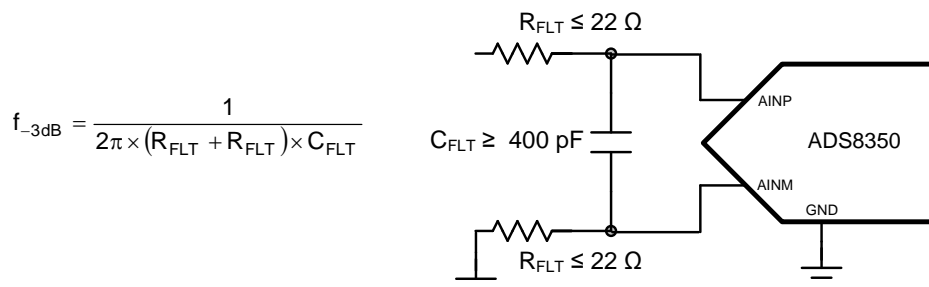
- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

## Typical Applications (continued)

### 8.2.1.2.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor,  $C_{FLT}$ , is connected across the ADC inputs (as shown in [Figure 57](#)).



**Figure 57. Antialiasing Filter**

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of  $C_{FLT}$  should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{FLT}$ ) are used at the output of the amplifiers. A higher value of  $R_{FLT}$  is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{FLT}$  requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of  $R_{FLT}$  to a maximum of 22  $\Omega$  in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22- $\Omega$  resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

The application circuit shown in [Figure 56](#) is optimized to achieve lowest distortion and lowest noise for a 10-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

## Typical Applications (continued)

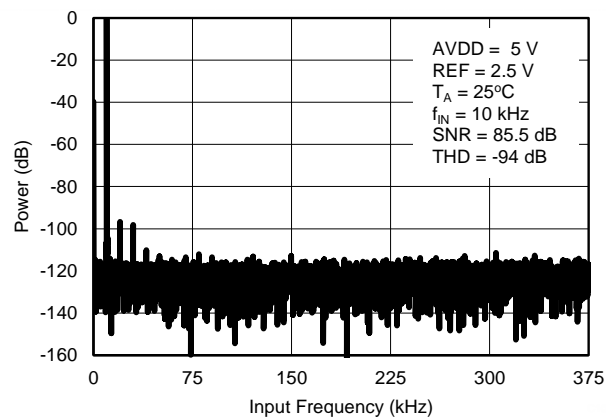
As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. The low-power [OPA836](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion, high-bandwidth specifications. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

### NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

### 8.2.1.3 Application Curve

[Figure 58](#) shows FFT plot and test results obtained with circuit configuration shown in [Figure 56](#).



**Figure 58. FFT Plot and Test Results with ADS8350**

Typical Applications (continued)

8.2.2 DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

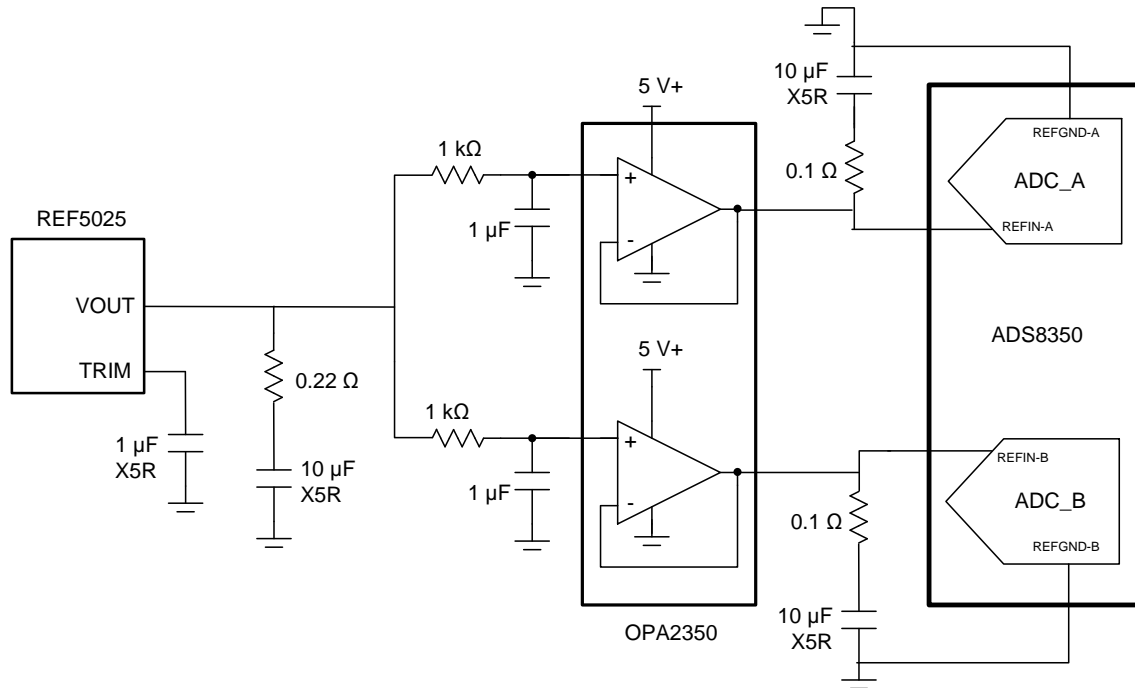


Figure 59. Reference Drive Circuit with  $V_{REF} = 2.5\text{ V}$

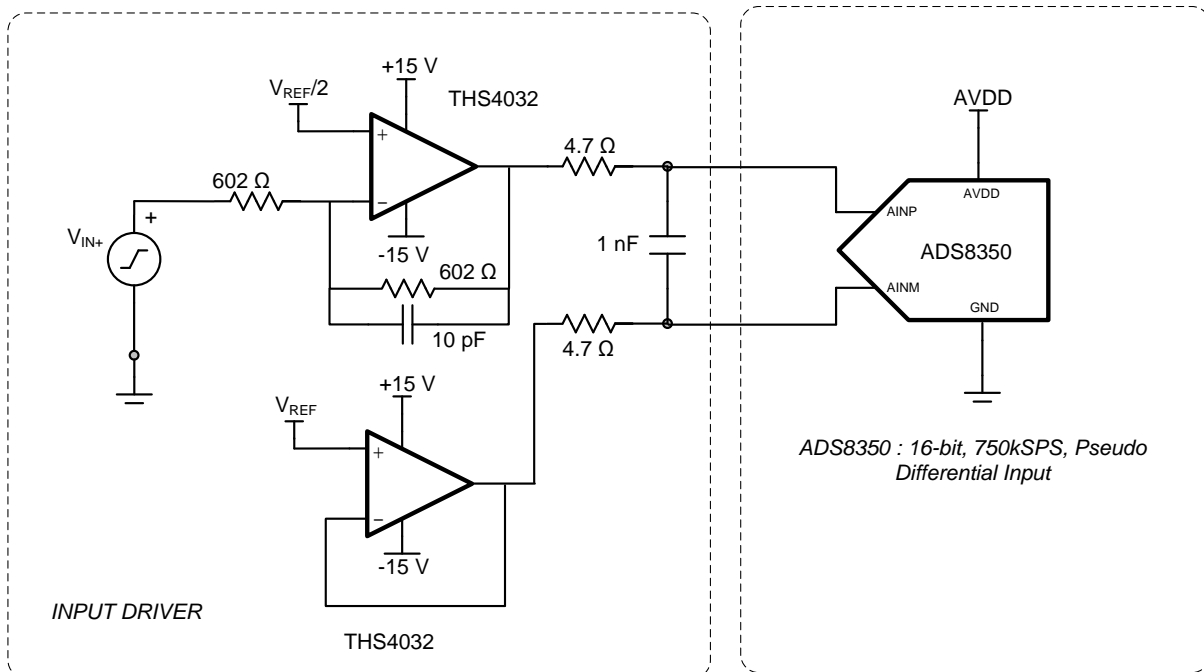


Figure 60. DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

## Typical Applications (continued)

### 8.2.2.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve > 84-dB SNR and < –90-dB THD at a 100-kHz input frequency.

### 8.2.2.2 Detailed Design Procedure

#### 8.2.2.2.1 ADC Reference Driver

Refer to the [ADC Reference Driver](#) section for a detailed design procedure for the ADC reference driver.

The application circuit in [Figure 55](#) shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8350 at sampling rates up to 750 kSPS.

The 2.5-V reference voltage is generated by the high-precision, low-noise [REF5025](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10  $\mu$ F. The low output impedance, low noise, and fast settling time makes the [OPA2350](#) a good choice for driving this high capacitive load.

#### 8.2.2.2.2 ADC Input Driver

Refer to [ADC Input Driver](#) section for the detailed design procedure for an ADC input driver.

The application circuit shown in [Figure 60](#) is optimized to achieve lowest distortion and lowest noise for a 100-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the input of the amplifier. The [THS4032](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion, low-noise, and high-bandwidth specifications. The ADC AINM pin is also driven to  $V_{REF}$  with the same amplifier to match the source impedance and to take full advantage of the pseudo-differential input structure of the ADC. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

---

#### NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

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## Typical Applications (continued)

### 8.2.2.3 Application Curve

Figure 61 shows FFT plot and test results obtained with circuit configuration shown in Figure 60.

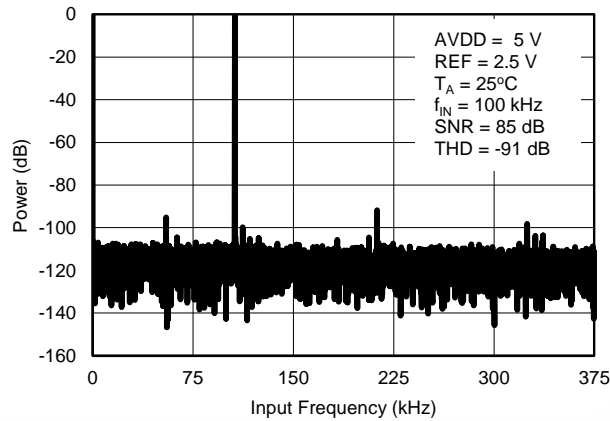


Figure 61. FFT Plot and Test Results with ADS8350

## 9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The ADC operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible range.

The AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, the external reference voltages  $V_{REFIN\_A}$  and  $V_{REFIN\_B}$  should be as shown in Equation 10:

$$2\text{ V} \leq V_{REFIN\_x} \leq AVDD / 2 \quad (10)$$

In other words, in order to use the  $V_{REFIN\_x}$  external reference voltage and use the full dynamic range on the analog input pins, AVDD must be set as shown in Equation 11, Equation 12, and Equation 13:

$$AVDD \geq 2 \times V_{REFIN\_A} \quad (11)$$

$$AVDD \geq 2 \times V_{REFIN\_B} \quad (12)$$

$$4.5\text{ V} \leq AVDD \leq 5.5\text{ V} \quad (13)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10- $\mu$ F decoupling capacitors, as shown in Figure 62.

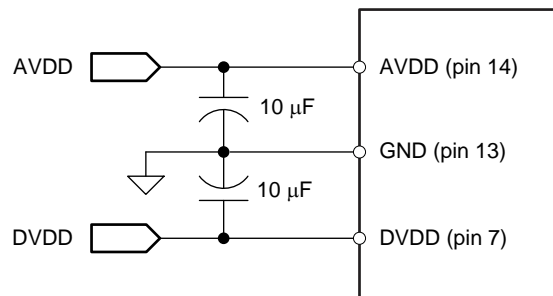


Figure 62. Power-Supply Decoupling

## 10 Layout

### 10.1 Layout Guidelines

Figure 63 shows a board layout example for the ADS7250, ADS7850, and ADS8350. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 63, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the ADS8350 must be clean and well-bypassed. Use 10- $\mu\text{F}$  ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFIN-A and REFIN-B reference inputs are bypassed with 10- $\mu\text{F}$ , X7R-grade ceramic capacitors ( $C_{\text{REF-X}}$ ). Although the reference inputs of the device draw little current on average, there are instantaneous dynamic current demands placed on the reference circuitry characteristic of SAR ADCs. Place the reference bypass capacitors as close as possible to the reference REFIN-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIN-x pins and the bypass capacitors. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation. Small 0.1- $\Omega$  to 0.2- $\Omega$  resistors ( $R_{\text{REF-X}}$ ) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 63 shows the  $C_{\text{IN-A}}$  and  $C_{\text{IN-B}}$  filter capacitors placed across the analog input pins of the device.

### 10.2 Layout Example

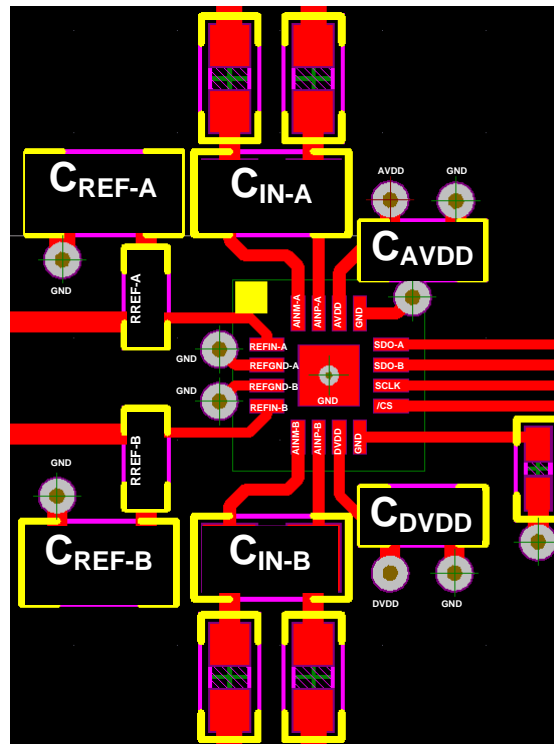


Figure 63. Layout Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference](#)
- [OPAx350 High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series](#)
- [OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifiers](#)
- [THS403x 100-MHz Low-Noise High-Speed Amplifiers](#)

#### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS8350	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADS7850	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADS7250	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 11.5 Trademarks

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#### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7250IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250	<a href="#">Samples</a>
ADS7250IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250	<a href="#">Samples</a>
ADS7850IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850	<a href="#">Samples</a>
ADS7850IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850	<a href="#">Samples</a>
ADS8350IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350	<a href="#">Samples</a>
ADS8350IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7250IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7250IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7250IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7250IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7850IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7850IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS8350IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS8350IRTET	WQFN	RTE	16	250	210.0	185.0	35.0



## GENERIC PACKAGE VIEW

**RTE 16**

**WQFN - 0.8 mm max height**

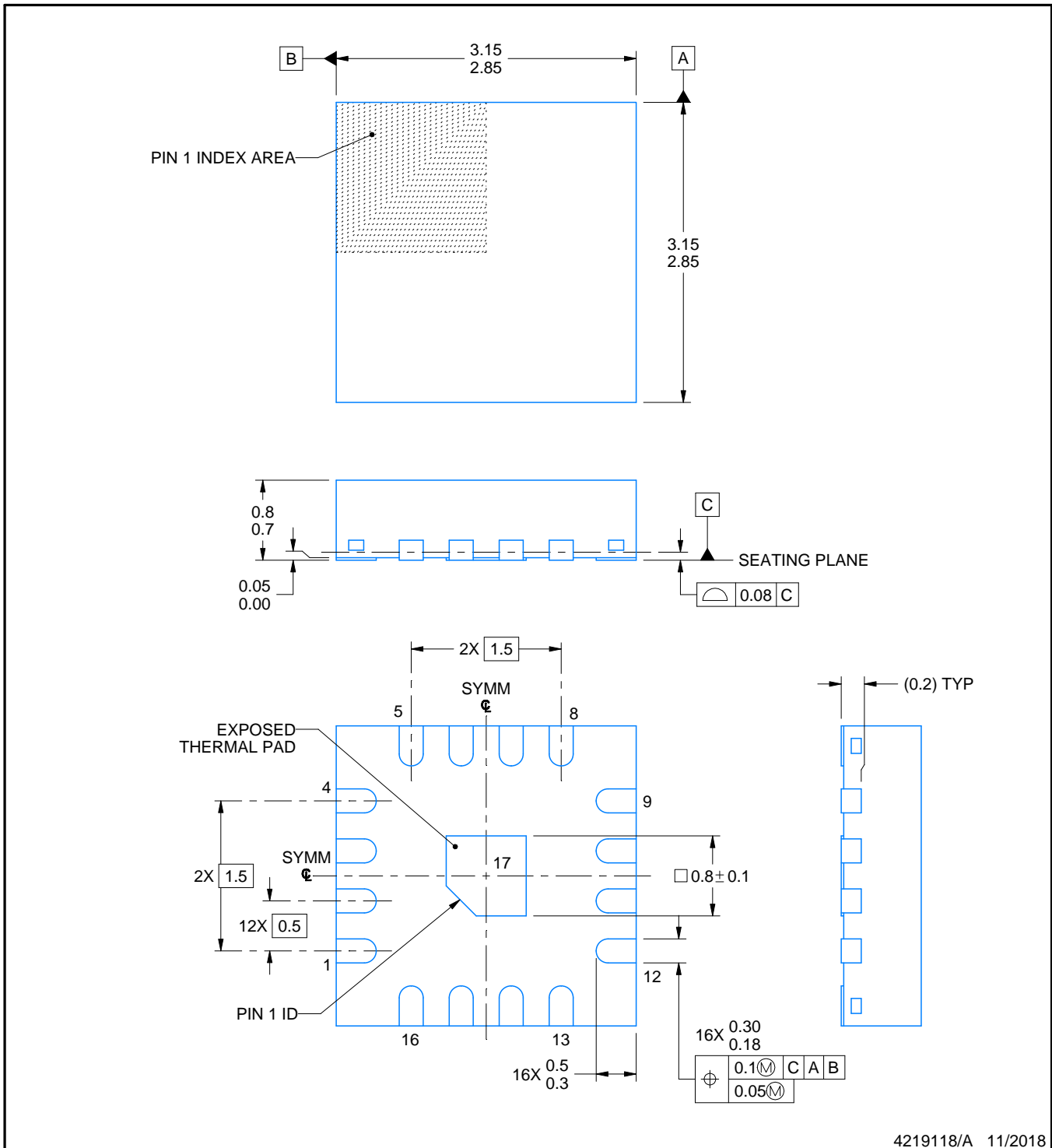
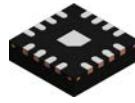
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A



4219118/A 11/2018

NOTES:

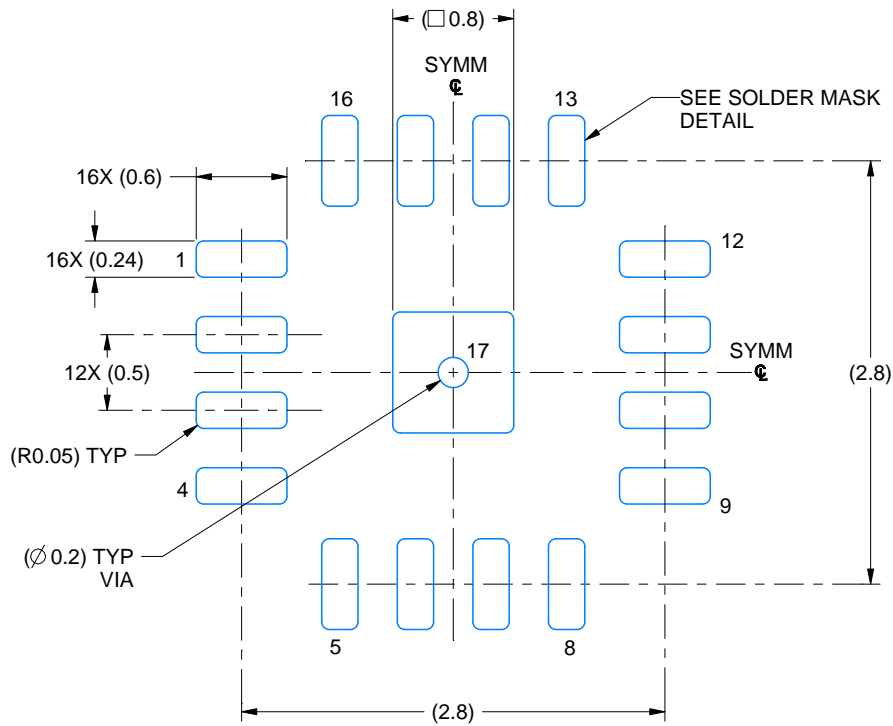
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4219118/A 11/2018

NOTES: (continued)

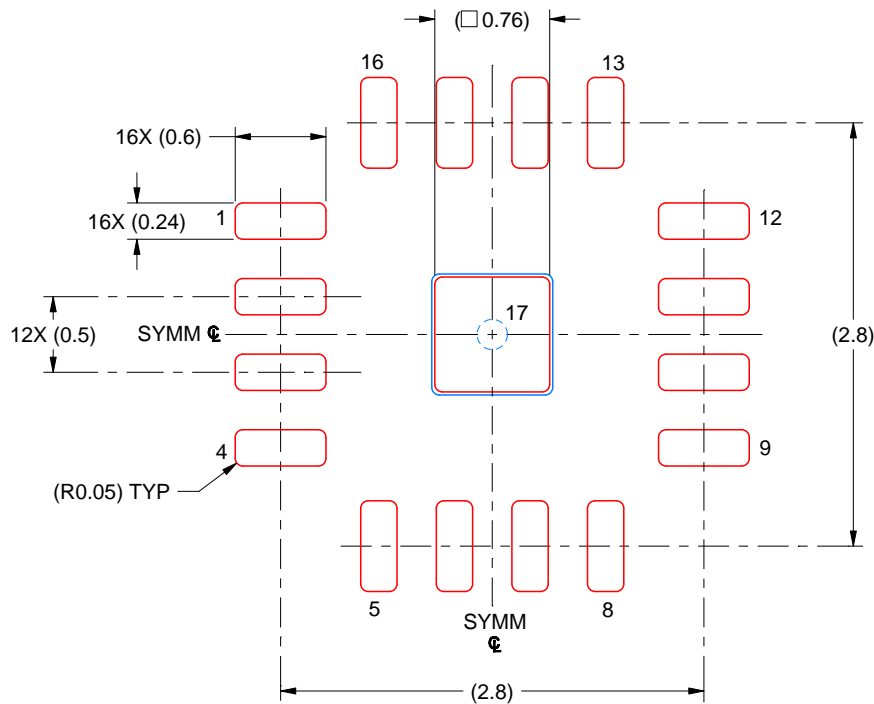
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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