P3I2005A

General Purpose Peak EMI Reduction IC

ON Semiconductor®

http://onsemi.com

Product Description

P3I2005A is a versatile, 3.3 V / 5 V, 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

P3I2005A modulates the output of a PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

P3I2005A accepts an input from an external reference clock and locks to a 1x modulated clock output. Two logic pins S0 and D_C enable selecting one of the 4 different frequency deviations. Refer *Deviation Selection table.* Frequency Range Selection pin enables operation in one of the two frequency ranges. P3I2005A operates over a supply voltage range of 5 V / 3.3 V. P3I2005A is available in 8 Pin SOIC Package.

Features

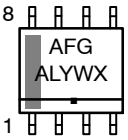
- 1x, LVCMOS Peak EMI Reduction
- Input Clock Frequency : 10 MHz – 100 MHz
- Output Clock Frequency : 10 MHz – 100 MHz
- Four different Frequency Deviation selection
- Frequency range Selection
- Supply voltage: 5 V ± 0.5 V
  3.3 V ± 0.3 V
- 8 Pin SOIC Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Application

- P3I2005A is targeted for use in a broad range of notebook and desktop PCs and consumer electronic applications.

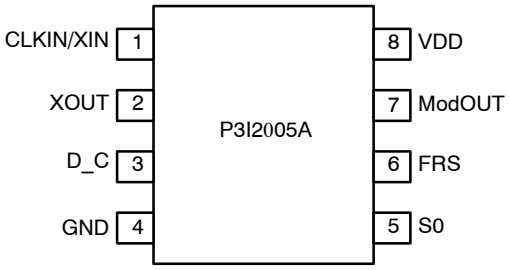
SOIC−8
CASE 751

MARKING DIAGRAM



AFG	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

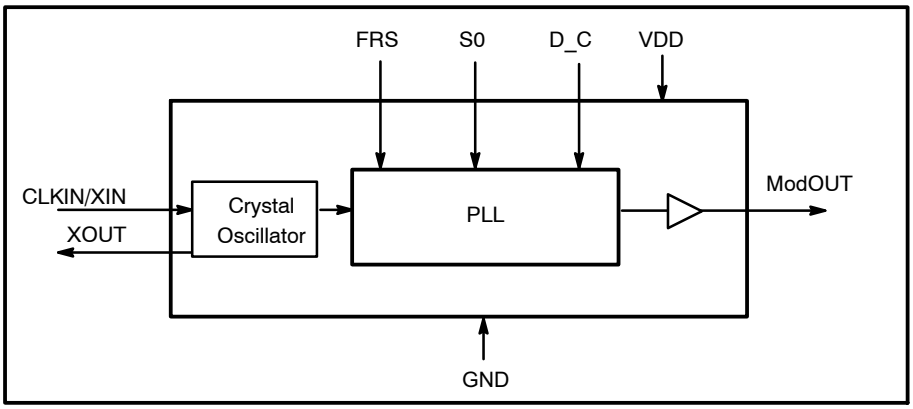


Figure 1. Block Diagram

PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	External reference Clock input or Crystal connection.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	D_C	I	Deviation Selection. Has an internal pull−up resistor. *Refer to Deviation Selection table*
4	GND	P	Ground connection.
5	S0	I	Deviation Selection. Has an internal pull−up resistor. *Refer to Deviation Selection table*
6	FRS	I	Frequency Range Selection. Has an internal pull−up resistor
7	ModOUT	O	Buffered Modulated Clock Output.
8	VDD	P	Power supply for the entire chip(3.3 V/5 V)

FREQUENCY RANGE SELECTION TABLE

FRS	Frequency(MHz)
0	10 – 30
1	30 – 100

DEVIATION SELECTION TABLE

Deviation (%)							
		FS = 0			FS = 1		
D_C	S0	10 MHz	20 MHz	30 MHz	30 MHz	80 MHz	100 MHz
0	0	−4.5	−3.6	−1.7	−4.8	−3.6	−2.6
0	1	−2.6	−2	−1	−2.7	−2	−1.5
1	0	±2.6	±2	±1	±2.75	±2	±1.5
1	1	±1.7	±1.25	±0.7	±1.8	±1.25	±1

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$VDD_{(5V)}$	Supply Voltage	4.5	5.5	V
$VDD_{(3.3V)}$	Supply Voltage	3	3.6	V
T_A	Operating Temperature	−40	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any input pin with respect to Ground	−0.5 to +7.0	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

DC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 5 V ± 0.5 V

Symbol	Parameter		Min	Typ	Max	Unit
VDD	Operating voltage		4.5	5.0	5.5	V
V_{IL}	Input low voltage		GND − 0.3		0.8	V
V_{IH}	Input high voltage		2.0		V_{DD} + 0.3	V
I_{IL}	Input low current				100	μA
I_{IH}	Input high current				100	μA
V_{OL}	Output low voltage (I_{OL} = 12 mA)				0.4	V
V_{OH}	Output high voltage (I_{OH} = −12 mA)		2.5			V
I_{CC}	Static supply current (CLKIN/XIN pulled to GND)				12	mA
I_{DD}	Dynamic supply current (Unloaded Output)	FS = 0 (@ 30 MHz)			34	mA
		FS = 1 (@ 100 MHz)			40	
Z_{OUT}	Output impedance			30		Ω

AC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 5 V ± 0.5 V

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN/XIN	Input Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
MODOUT	Output Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
t_{LH} (Notes 1 & 2)	Output Rise time (measured between 20% to 80%)			1.6	2	nS
t_{HL} (Notes 1 & 2)	Output Fall time (measured between 80% to 20%)			1.2	1.6	nS
t_D (Notes 1 & 2)	Output duty cycle		45	50	55	%
t_{JC} (Note 2)	Jitter (cycle to cycle) @ FS = 0, 24 MHz and FS = 1, 80 MHz			±250	±350	pS
t_{ON} (Notes 1 & 2)	PLL lock time (Stable VDD, valid Clock presented on CLKIN/XIN)				3	mS

1. All parameters are specified with 15 pF loaded output.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

DC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 3.3 V ± 0.3 V

Symbol	Parameter		Min	Typ	Max	Unit
VDD	Operating voltage		3	3.3	3.6	V
V_{IL}	Input low voltage		GND − 0.3		0.8	V
V_{IH}	Input high voltage		2.0		VDD + 0.3	V
I_{IL}	Input low current				100	μA
I_{IH}	Input high current				100	μA
V_{OL}	Output low voltage (I_{OL} = 12 mA)				0.4	V
V_{OH}	Output high voltage (I_{OH} = −12 mA)		2.5			V
I_{CC}	Static supply current (CLKIN/XIN pulled to GND)				11	mA
I_{DD}	Dynamic supply current (Unloaded Output)	FS = 0 (@ 30 MHz)			26	mA
		FS = 1 (@ 100 MHz)			32	
Z_{OUT}	Output impedance			40		Ω

AC ELECTRICAL CHARACTERISTICS FOR V_{DD} = 3.3 V ± 0.3 V

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN/XIN	Input Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
MODOUT	Output Clock Frequency	FRS = 0	10		30	MHz
		FRS = 1	30		100	
t_{LH} (Notes 3 & 4)	Output Rise time (measured between 20% to 80%)			1.9	2.5	nS
t_{HL} (Notes 3 & 4)	Output Fall time (measured between 80% to 20%)			1.5	2	nS
t_{D} (Notes 3 & 4)	Output duty cycle		45	50	55	%
t_{JC} (Note 4)	Jitter (cycle to cycle) @ FS=0, 24MHz & FS=1, 80 MHz			±250	±350	pS
t_{ON} (Notes 3 & 4)	PLL lock time (Stable VDD, valid Clock presented on CLKIN/XIN)				3	mS

3. All parameters are specified with 15 pF loaded output.
4. Parameter is guaranteed by design and characterization. Not 100% tested in production

ORDERING INFORMATION

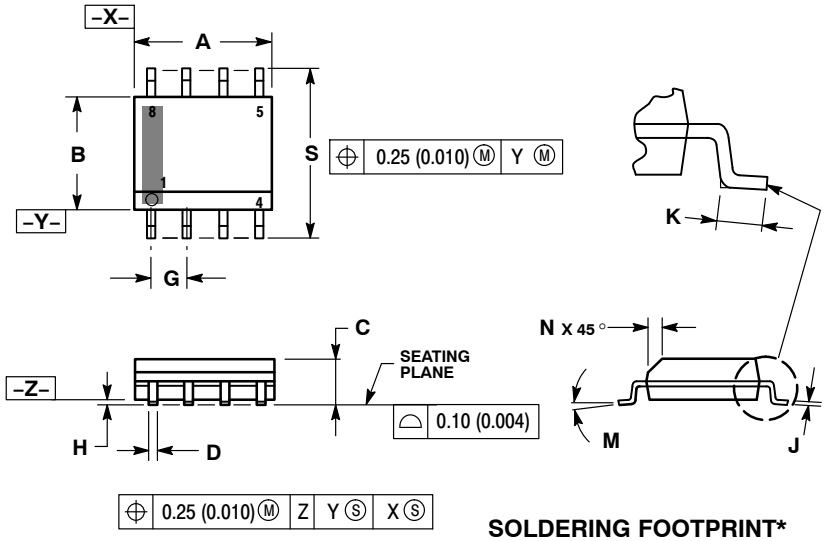
Part Number	Marking	Package	Temperature	Shipping†
P3I2005AG−08SR	AFG	8−PIN SOIC (Pb−Free)	−40°C to +85°C	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

PACKAGE DIMENSIONS

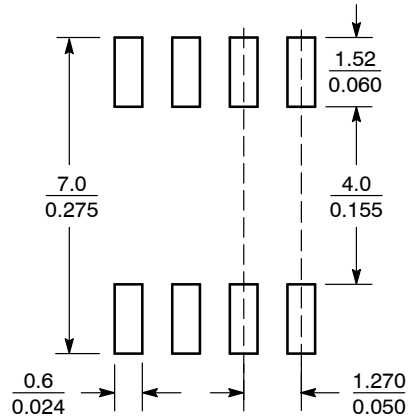
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative