



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



# FDMD8530

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

Q1: 30 V, 201 A, 1.25 mΩ Q2: 30 V, 201 A, 1.25 mΩ

### Features

- Q1: N-Channel
  - Max  $r_{DS(on)}$  = 1.25 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 35\text{ A}$
  - Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 32\text{ A}$
- Q2: N-Channel
  - Max  $r_{DS(on)}$  = 1.25 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 35\text{ A}$
  - Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 32\text{ A}$
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- RoHS Compliant

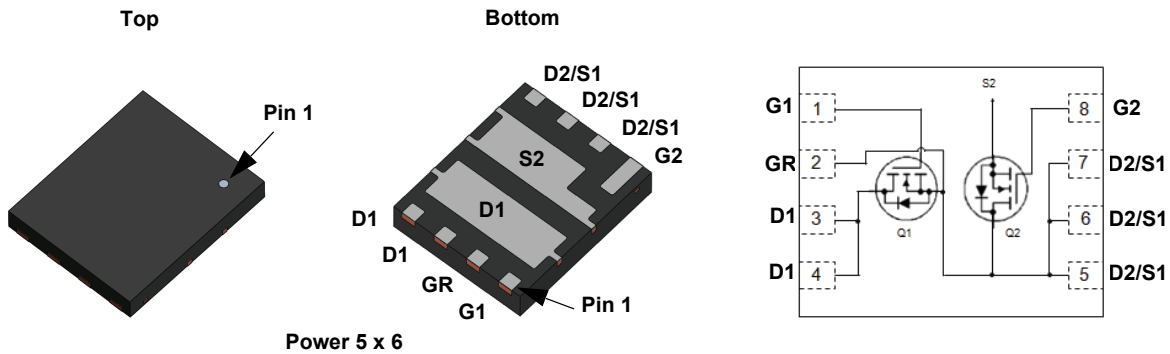


### General Description

This device includes two 30V N-Channel MOSFETs in a dual power (5 mm X 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}$ /Qg FOM silicon.

### Applications

- POL Synchronous Dual
- One Phase Motor Half Bridge
- Half/Full Bridge Secondary Synchronous Rectification



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units	
$V_{DS}$	Drain to Source Voltage	30	30	V	
$V_{GS}$	Gate to Source Voltage	±20	±20	V	
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	201	201	A
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	127	127	
	Drain Current -Continuous	$T_A = 25\text{ °C}$	35 <sup>1a</sup>	35 <sup>1b</sup>	
	-Pulsed	(Note 4)	1047	1047	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	661	661	mJ
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	78	78	W
	Power Dissipation	$T_A = 25\text{ °C}$	2.2 <sup>1a</sup>	2.2 <sup>1b</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C	

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.6	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55 <sup>1a</sup>	55 <sup>1b</sup>	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8530	FDMD8530	Power 5 x 6	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	------	-------

**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		20 20		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	Q1 Q2	1.0 1.0	1.5 1.5	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-5 -5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 35\text{ A}$	Q1		0.77	1.25	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 32\text{ A}$			0.96	1.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 35\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$			1.1	1.8	
		$V_{GS} = 10\text{ V}$ , $I_D = 35\text{ A}$	Q2		0.77	1.25	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 32\text{ A}$			0.96	1.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 35\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$			1.1	1.8	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 35\text{ A}$	Q1 Q2		259 259		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	Q1 Q2		7425 7425	10395 10395	pF
$C_{oss}$	Output Capacitance		Q1 Q2		2190 2190	3070 3070	pF
$C_{rss}$	Reverse Transfer Capacitance		Q1 Q2		220 220	310 310	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	1.9 1.9	3.8 3.8	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 35\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		14 14	25 25	ns
$t_r$	Rise Time		Q1 Q2		13 13	24 24	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		71 71	114 114	ns
$t_f$	Fall Time		Q1 Q2		21 21	34 34	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$	Q1 Q2		106 106	149 149
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q1 Q2		50 50	70 70	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 15\text{ V}$ , $I_D = 35\text{ A}$	Q1 Q2		16 16		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		13 13		nC

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

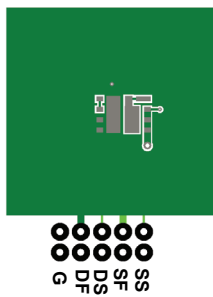
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

#### Drain-Source Diode Characteristics

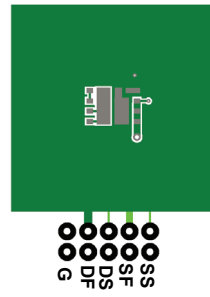
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 35\text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.3 1.3	V
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q1 Q2		0.7 0.7	1.2 1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 35\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		54 54	87 87	ns
$Q_{rr}$	Reverse Recovery Charge		Q1 Q2		39 39	63 63	nC

**NOTES:**

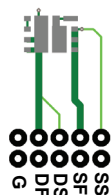
1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



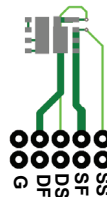
a. 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 155 °C/W when mounted on a minimum pad of 2 oz copper



d. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

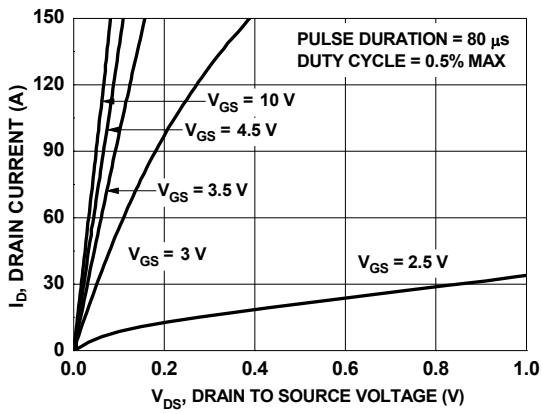
3. Q1:  $E_{AS}$  of 661 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 21\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 65\text{ A}$ .

Q2:  $E_{AS}$  of 661 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 21\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 65\text{ A}$ .

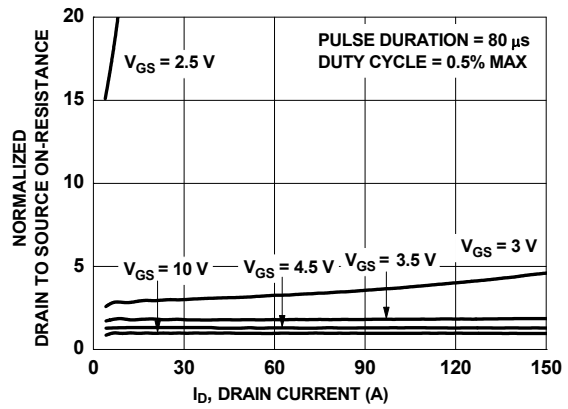
4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

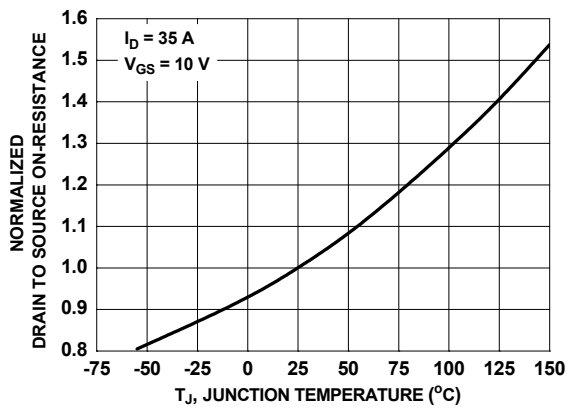
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



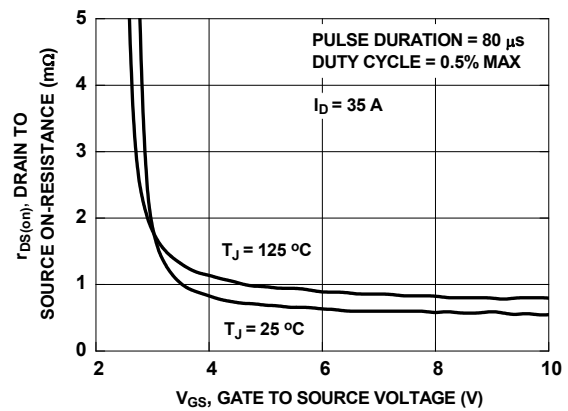
**Figure 1. On Region Characteristics**



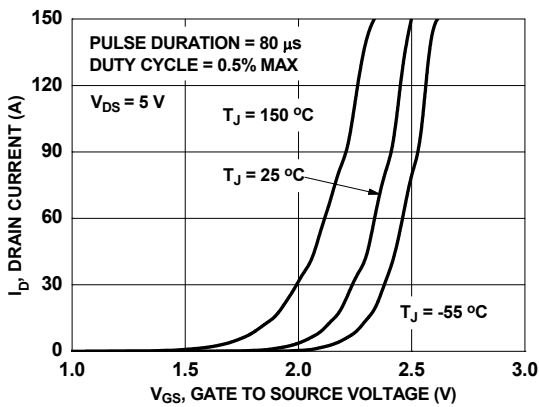
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



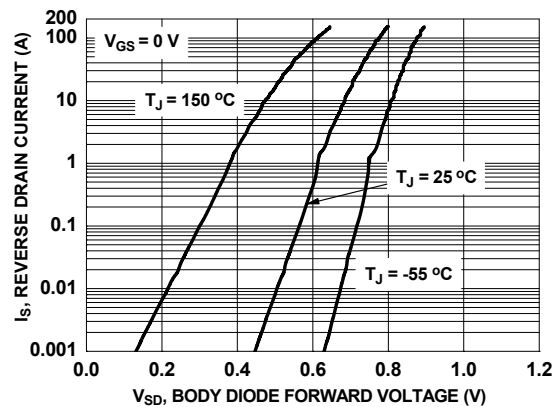
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

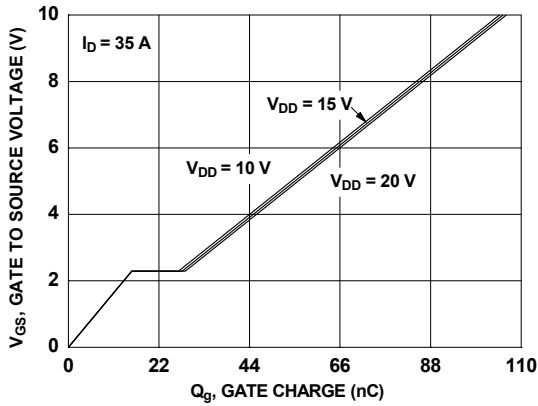


**Figure 5. Transfer Characteristics**

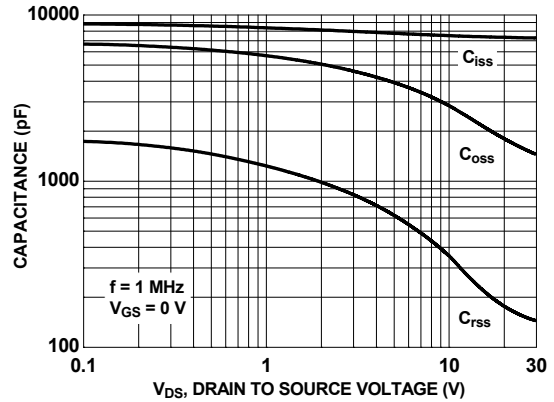


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

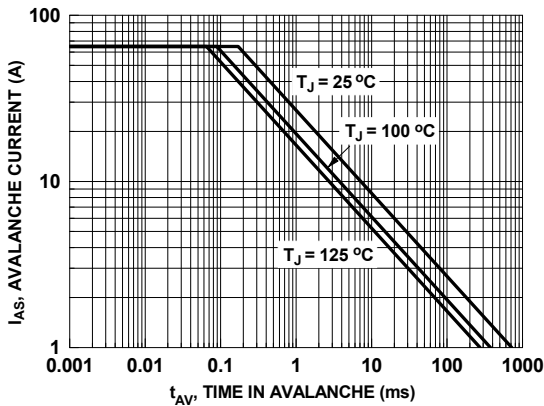
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



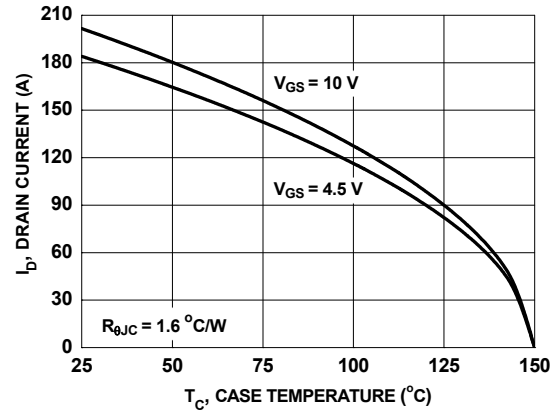
**Figure 7. Gate Charge Characteristics**



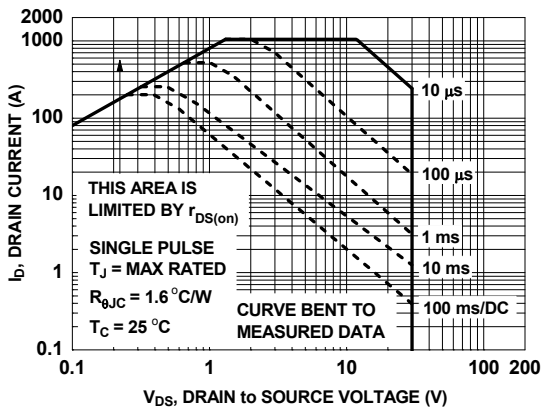
**Figure 8. Capacitance vs. Drain to Source Voltage**



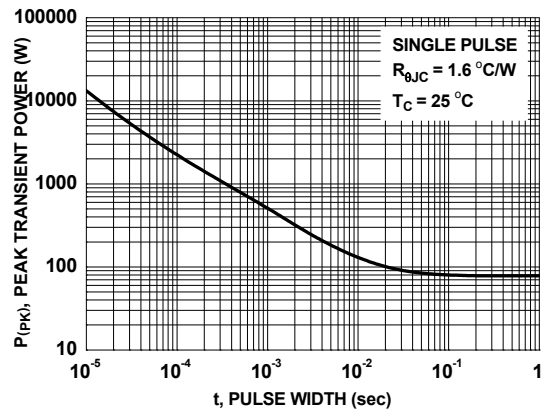
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

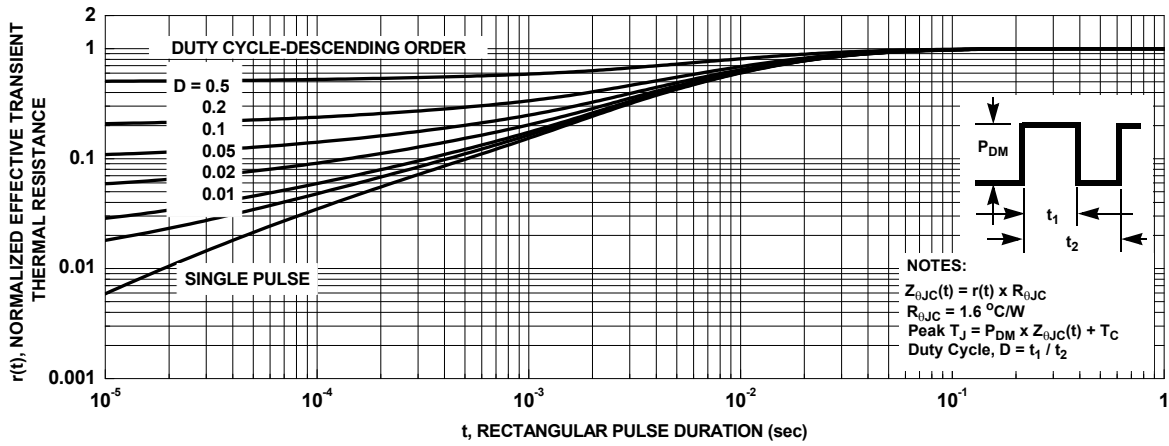


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

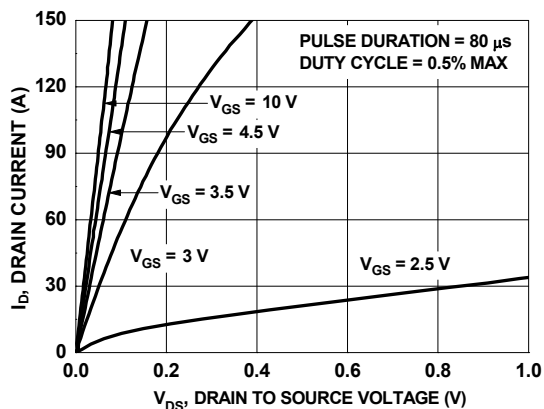


Figure 14. On-Region Characteristics

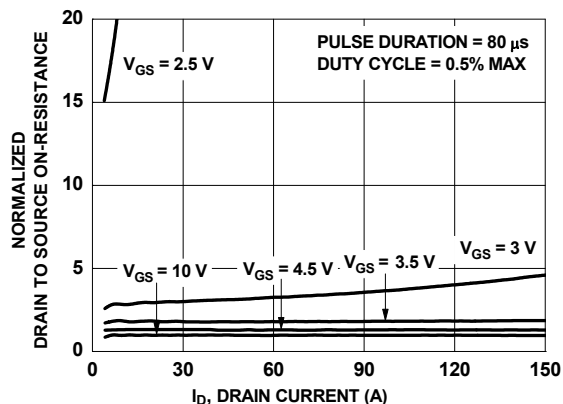


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

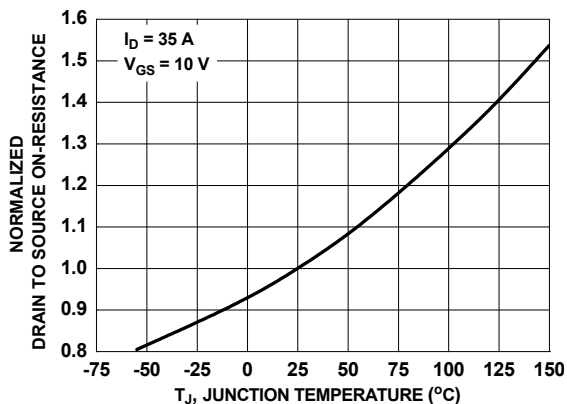


Figure 16. Normalized On-Resistance vs. Junction Temperature

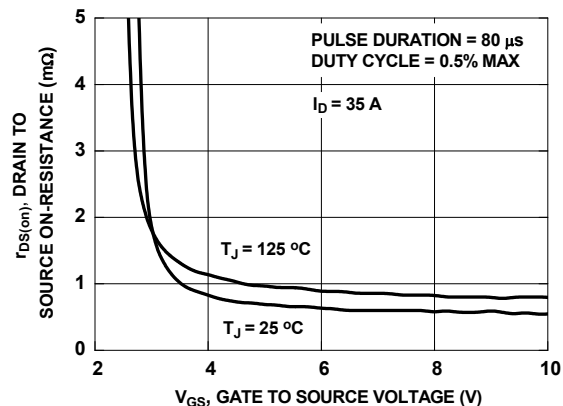


Figure 17. On-Resistance vs. Gate to Source Voltage

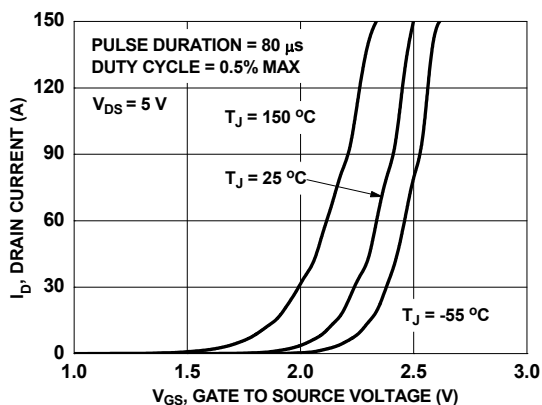


Figure 18. Transfer Characteristics

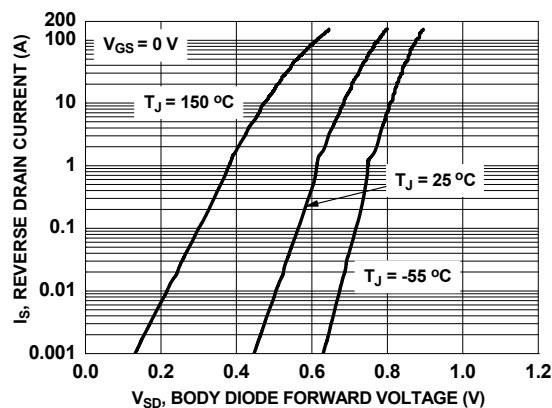
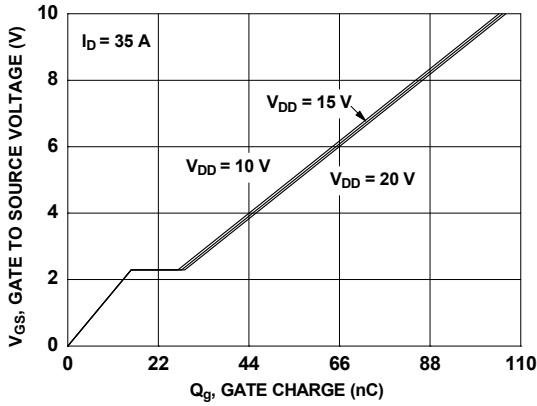


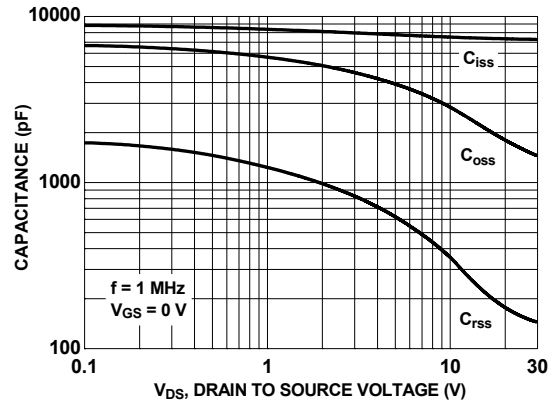
Figure 19. Source to Drain Diode Forward Voltage vs. Source Current



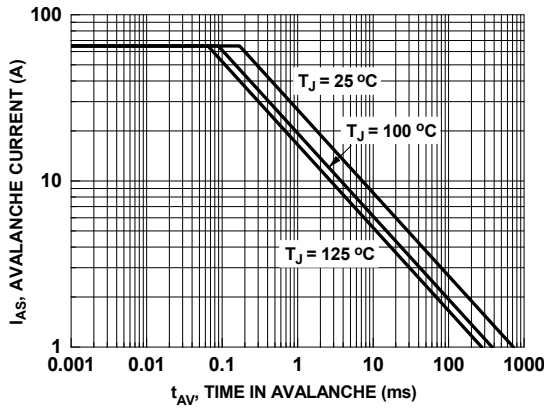
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



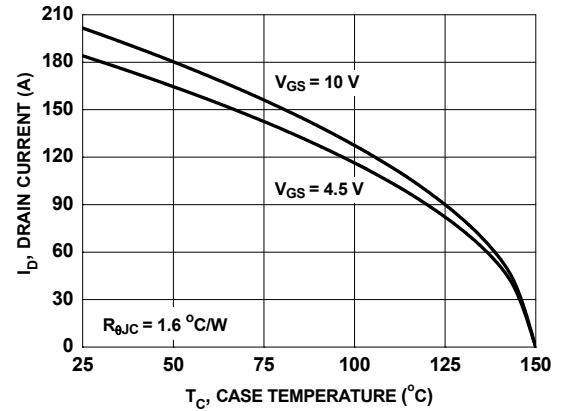
**Figure 20. Gate Charge Characteristics**



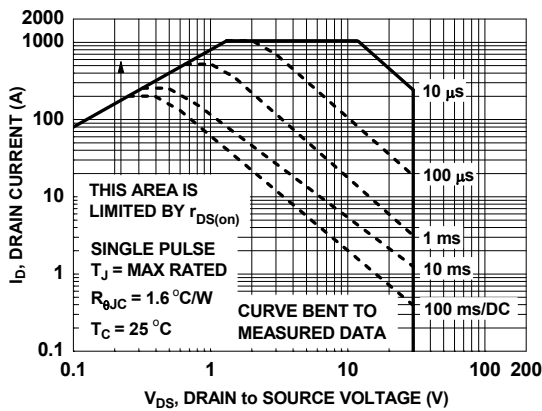
**Figure 21. Capacitance vs. Drain to Source Voltage**



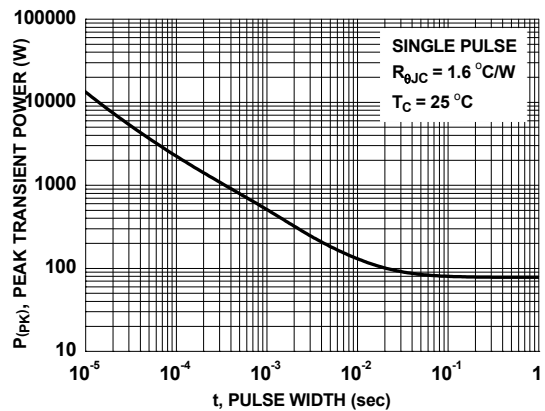
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

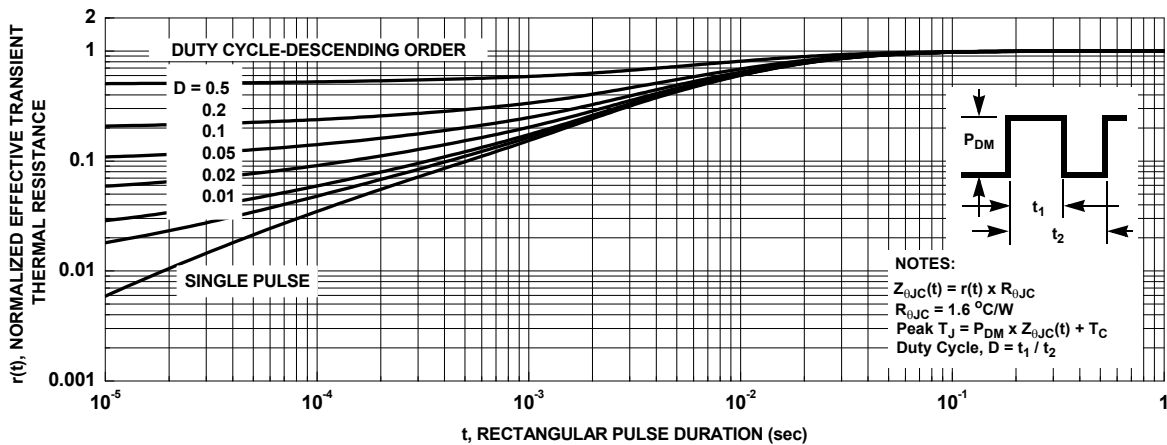


**Figure 24. Forward Bias Safe Operating Area**

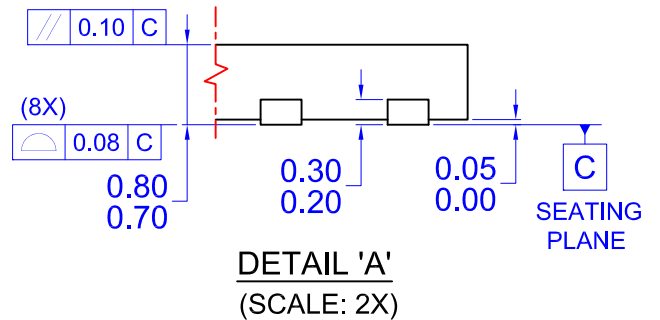
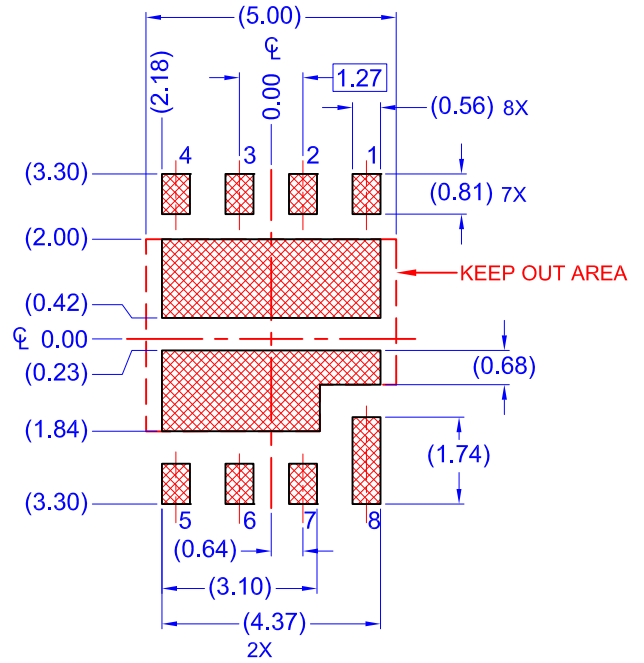
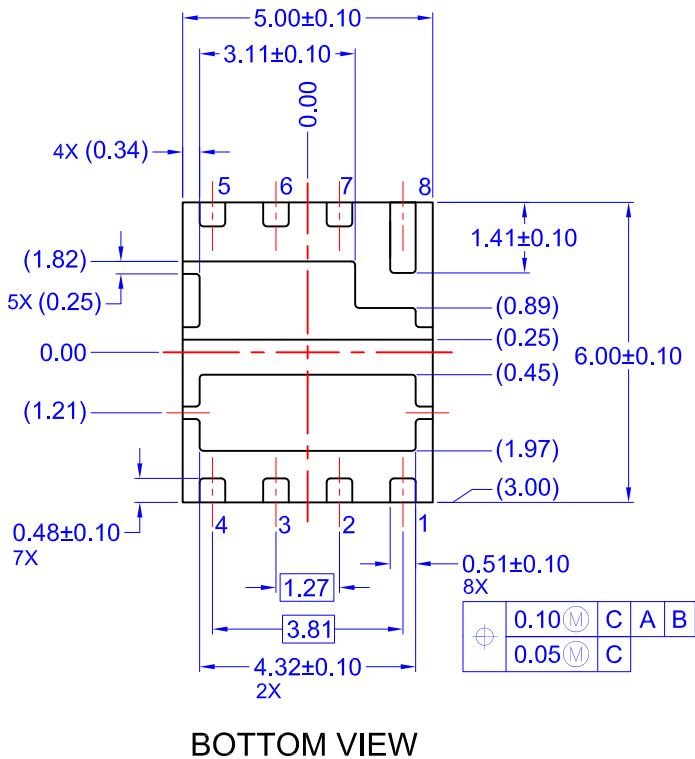
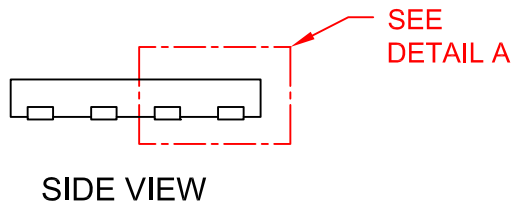
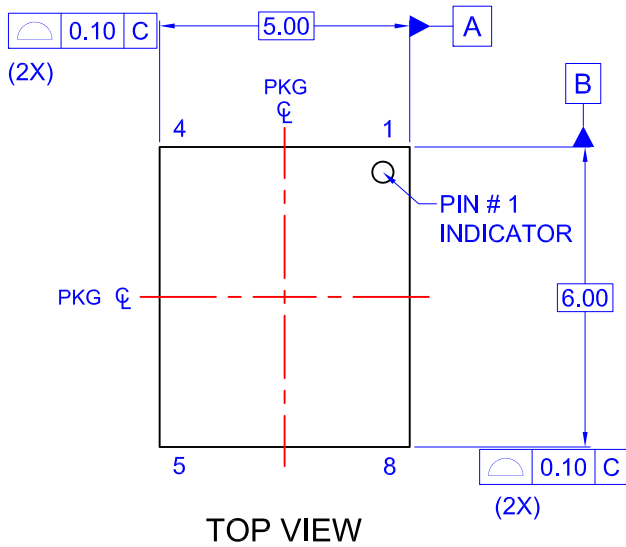


**Figure 25. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 26. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.
  - ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - DRAWING FILE NAME: MKT-PQFN08QREV2



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative