

### Description

Triad Semiconductor’s TS8000 is a complete ultrasonic receiver analog front end. Working with an external transducer the TS8000 converts ultrasonic sound waves into a digital time representation of the received pulses. The TS8000 provides digitally configurable noise filtering, gain amplification, and carrier data slicing of the weak ultrasonic input signals. The TS8000 is configured by a two-wire digital interface.

The TS8000 is available in a tiny 16-bump wafer level chip scale package (WLCSP, 1.66mm x 1.66mm, 0.4mm pitch). The device operates from a 3.3V nominal supply input and is specified over a 0°C to +85°C operating temperature range.

### Applications

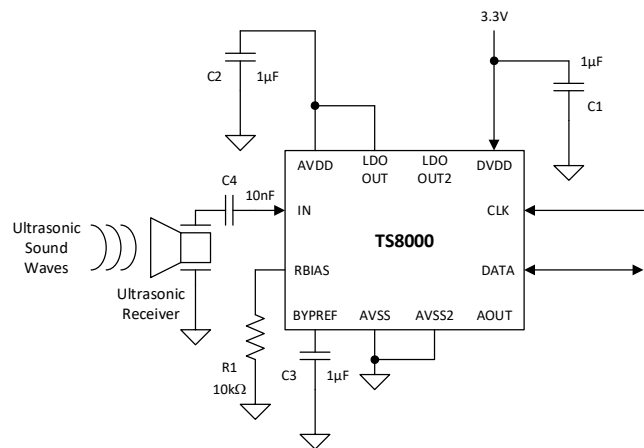
- Ultrasonic range finder
- Ultrasonic time of flight
- Tracking of Physical Objects in VR
- Ultrasonic communication
- Object detection and security systems



TS8000 Device Size  
1.66mm x 1.66mm

### Features

- Complete Ultrasonic Receiver Analog Front End (AFE)
- Receiver for 40kHz Ultrasonic Pulses
- Built in system calibrated bandpass filter for ambient noise rejection and operation in noisy environments
- Configurable high gain amplification of weak ultrasonic signals
- Configurable threshold data slicer for ultrasonic carrier waveform digital output
- Two-wire control bus for configuration, calibration, and mode control
- DVDD: 3.3V. Built in LDO for generation of clean analog supply
- Small Package Size simplifies industrial design of tracked objects
  - 16 Bump WLCSP Package
  - 1.66mm x 1.66mm, 0.4mm pitch



Simplified Application Circuit



### Programmable Gain Amplifier

The programmable gain amplifier provides an additional 0dB to 24dB gain to the output of the bandpass filter yielding a total signal path gain of approximately 49dB to 73dB. The PGA gain is configured in application through the DATA and CLK interface. The TS8000 PGA can be configured to deliver an analog output signal at the AOUT pin.

### Data Detector

The data detector is triggered as the filtered and amplified ultrasonic signal of the PGA output crosses the configured voltage threshold. The data detector is implemented using a comparator with controlled hysteresis. The detection threshold is configured in application through the DATA and CLK interface. In normal operation the DATA output toggles logic low and high as the filtered and amplified ultrasonic receiver signal crosses the configured detection threshold. See Figure 3.

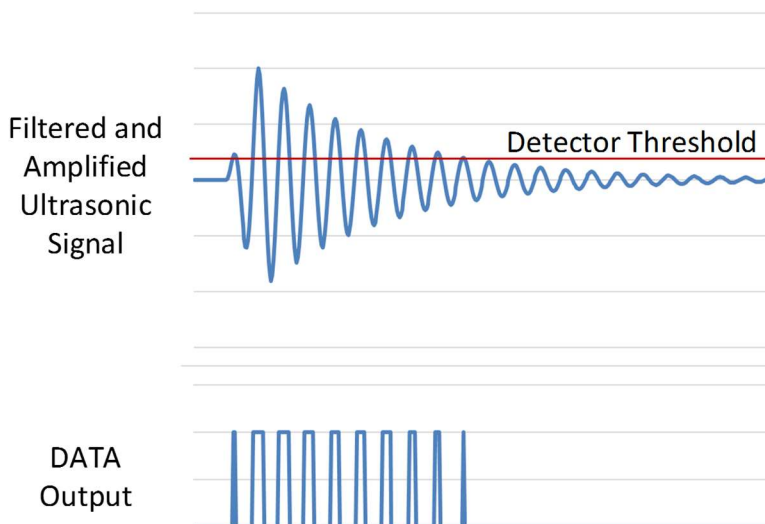


Figure 3: Output Waveform for Ultrasonic Carrier

### Digital Control Interface

The TS8000 provides a digital control interface to adjust the bandpass filter center frequency, programmable amplifier gain, data detector threshold, and device operating mode. It also provides the calibration output signal that is required by the external system to adjust the bandpass filter to the optimal center frequency (~ 40kHz).

Figure 4 demonstrates the communications interface timing. After device power on the system logic communicates with the TS8000 over the DATA and CLK pins to configure the device. To enter configuration mode the CLK and DATA pins are toggled in the demonstrated order and a write or read transaction can then be initiated. While in write or read configuration mode the TS8000 will weakly drive the DATA pin with a 120uA source or sink bus keeper current to sustain the logic HIGH or LOW pin state that was clocked in or out of the device during the low clock phase. To allow for easy bus turnaround the TS8000 weakly sustains but does not strongly drive the DATA pin state during the CLK pin HIGH phase. For read or calibration cycles the TS8000 drives the DATA pin strongly only during the CLK LOW phase. For write transactions the pull state will dynamically change to match bits written into the ASIC.

At the end of each transaction cycle the configuration mode must be exited with the CLK and DATA pins toggled in the defined order. The DATA output may chatter for several hundred microseconds as configuration mode is exited and the bandpass filter is internally reconnected. At the end of a 'read' transaction a calibration data pulse may be initiated by the system (see Bandpass Filter Calibration section).

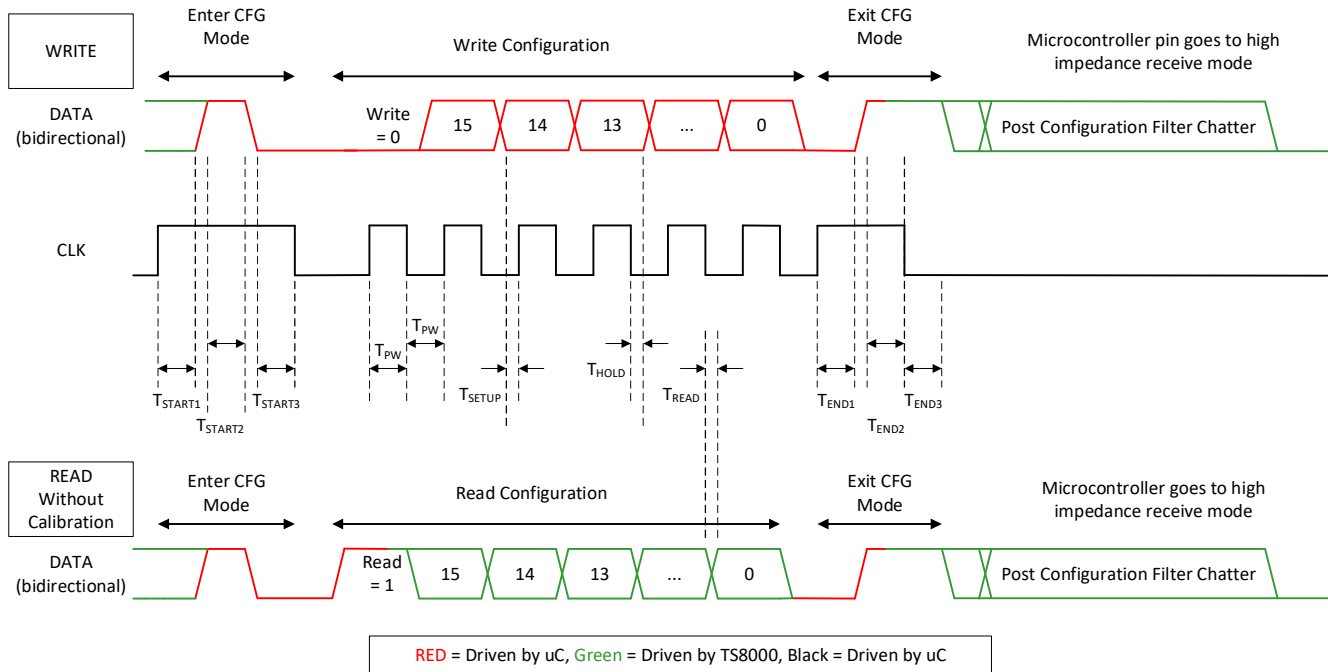


Figure 4: Configuration Interface Timing

### Configuration Registers

The TS8000 contains a single 16-bit configuration register to adjust the filter center frequency trim, the programmable amplifier gain, the data slicer threshold, and the device operational mode. The register map is given in Table 1.

| Field Name                                                                           | Bit Range | Default     | Pin Type | Description                                                                                                                                                                            |
|--------------------------------------------------------------------------------------|-----------|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Functional Mode                                                                      | [15:13]   | 000         | R/W      | 000 – Default (AOUT disabled / Data out EN)<br>001 – AOUT enabled / Data Out enabled<br>010 – AOUT enabled / Data Out disabled<br>011 → 101 Test (Do Not Use)<br>111 – Sleep (standby) |
| Data Slicer Offset Threshold (approximate values)                                    | [12:10]   | 010         | R/W      | 000 – Off (center slicing)<br>001 – Minimum<br>010 – Default<br>....<br>111 – Maximum                                                                                                  |
| PGA Amplifier Gain (above ~49 dB signal path gain prior to PGA) (approximate values) | [9:7]     | 000         | R/W      | 000 – 0 dB<br>001 – 3 dB<br>010 – 6 dB<br>011 – 11 dB<br>100 – 17 dB<br>101 – 21 dB<br>110 – 24 dB<br>111 – N/A - Do Not Use                                                           |
| Filter Variable Capacitor Trim                                                       | [6:0]     | 010110<br>0 | R/W      | 0000000 – Minimum value<br>....<br>0101100 – Default<br>....<br>1111111 – Maximum value                                                                                                |

Table 1: Configuration Register Map

### Bandpass Filter Calibration

The digital control interface is used to initiate and pass a calibration pulse from the TS8000 DATA output to the system controller to facilitate calibration. The calibration DATA pulse may be initiated at the end of each configuration register read cycle. The calibration pulse is generated after the last falling edge of CLK in the read cycle. For a 40kHz bandpass filter center frequency the ideal DATA calibration pulse is 75µs. The system controller measures the time from the rising edge of the calibration pulse to the falling edge. The values of the capacitive components of the filter are then adjusted by the system controller through a configuration write cycle and the measurement is repeated. This sequence is repeated until the closest (within acceptable margin) value to the ideal is determined and the final configuration is set. At the end of the calibration read / measure / write sequence the configuration mode must be exited.

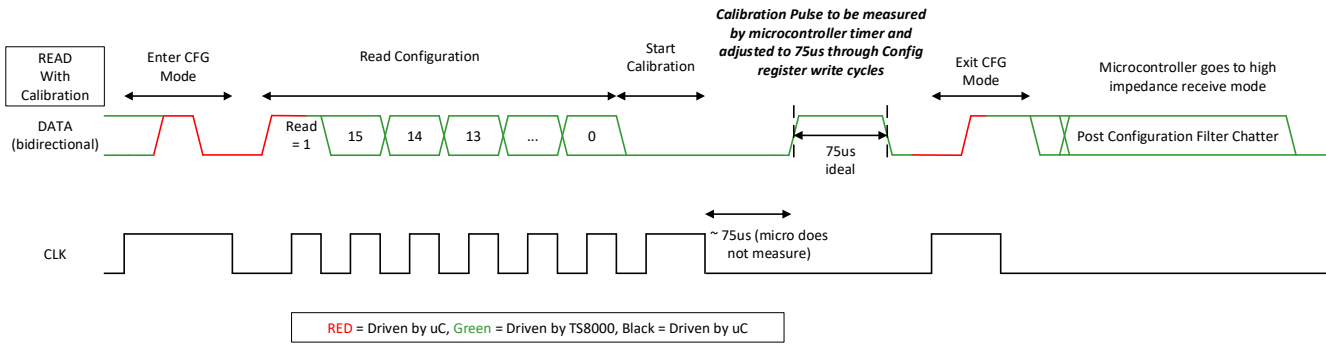


Figure 5: Calibration Interface Timing

## Performance Characteristics

### Absolute Maximum Ratings

| Parameter <sup>(1)(2)</sup>                            | Notes/Conditions               | MIN  | MAX | units |
|--------------------------------------------------------|--------------------------------|------|-----|-------|
| DVDD                                                   |                                |      | 3.6 | V     |
| Digital Input Voltage                                  |                                | -0.3 | 3.6 | V     |
| Junction Temperature, T <sub>JMAX</sub>                | Maximum Junction Temperature   |      | 150 | °C    |
| Storage Temperature, T <sub>STOR</sub>                 | Storage Temperature Range      | -40  | 150 | °C    |
| Soldering Information: infrared or convection (30 sec) | Peak body temperature (reflow) |      | 260 | °C    |

(1) All Voltages are specified with respect to GND = 0Vdc

(2) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

### ESD Ratings

| Parameter                                  | Notes/Conditions                                                       | Value | units |
|--------------------------------------------|------------------------------------------------------------------------|-------|-------|
| V <sub>(ESD)</sub> Electrostatic Discharge | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001-2014 <sup>(1)</sup> | 2000  | V     |

(1) JEDEC document JEP155 States that 500-V HBM allows safe manufacturing with a standard ESD control process

### Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

| Parameter                       | Notes/Conditions            | MIN | TYP | MAX | units |
|---------------------------------|-----------------------------|-----|-----|-----|-------|
| DVDD                            | Supply voltage              | 3.0 | 3.3 | 3.6 | V     |
| T <sub>AMB</sub> <sup>(1)</sup> | Operating temperature range | 0   |     | 85  | °C    |

(1) The maximum power dissipation is a function of T<sub>J(MAX)</sub>,  $\Theta_{JA}$  and the ambient temperature T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is  $PD = (T_{J(MAX)} - T_{AMB})/\Theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board

### Thermal Information

| Parameter                                  | Notes/Conditions                                                       | Value | units |
|--------------------------------------------|------------------------------------------------------------------------|-------|-------|
| V <sub>(ESD)</sub> Electrostatic Discharge | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001-2014 <sup>(1)</sup> | 2000  | V     |

(1) JEDEC document JEP155 States that 500-V HBM allows safe manufacturing with a standard ESD control process

### Electrical Characteristics

Operating conditions: DVDD = 3.3 V, T<sub>AMB</sub> = 25 °C unless otherwise noted<sup>(1)</sup>.

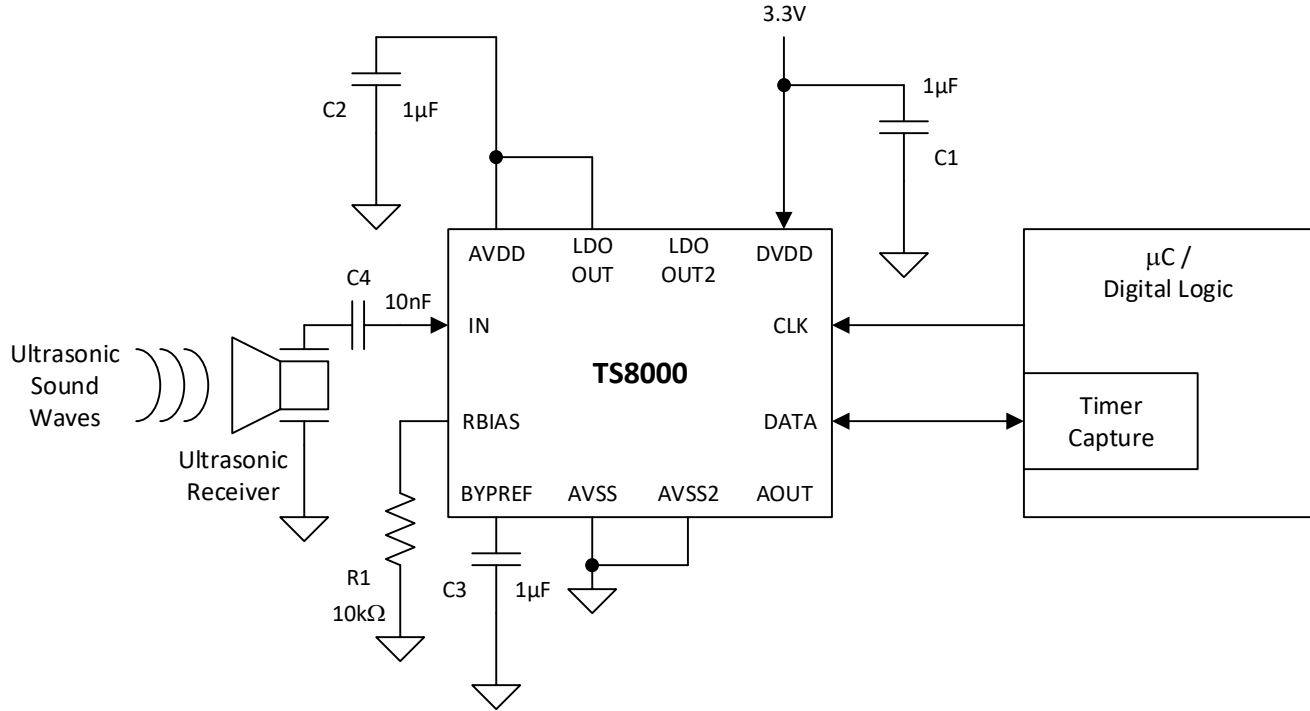
| Parameter              | Notes/Conditions        | MIN <sup>(2)</sup> | TYP <sup>(3)</sup> | MAX <sup>(2)</sup> | units |
|------------------------|-------------------------|--------------------|--------------------|--------------------|-------|
| <b>Power Supply</b>    |                         |                    |                    |                    |       |
| I <sub>VDD</sub>       | Operating Current       |                    | 2.5                |                    | mA    |
| Sleep_I <sub>VDD</sub> | Sleep mode current      |                    | 1                  |                    | mA    |
| <b>Digital IO</b>      |                         |                    |                    |                    |       |
| V <sub>IL</sub>        | Input Low Voltage       |                    |                    | 0.25 * VDD         | V     |
| V <sub>IH</sub>        | Input High Voltage      | 0.75 * VDD         |                    |                    | V     |
| V <sub>OL</sub>        | Output Low Voltage      |                    |                    | 0.1 * VDD          | V     |
| V <sub>OH</sub>        | Output High Voltage     | 0.9 * VDD          |                    |                    | V     |
| I <sub>PU</sub>        | Output Pullup Current   |                    | 120                |                    | μA    |
| I <sub>PD</sub>        | Output Pulldown Current |                    | 120                |                    | μA    |

| Parameter                 | Notes/Conditions            | MIN <sup>(2)</sup>       | TYP <sup>(3)</sup> | MAX <sup>(2)</sup> | units |
|---------------------------|-----------------------------|--------------------------|--------------------|--------------------|-------|
| Rise <sup>(2)</sup>       | 10/90% Output Rise Time     | 20pF load                | 9                  |                    | ns    |
| Fall <sup>(2)</sup>       | 10/90% Output Fall Time     | 20pF load                | 7                  |                    | ns    |
| T <sub>start1,2,3</sub>   |                             |                          | 100                |                    | ns    |
| T <sub>pw</sub>           |                             | Min CLK HIGH or LOW time | 100                |                    | ns    |
| T <sub>setup</sub>        |                             |                          | 50                 |                    | ns    |
| T <sub>hold</sub>         |                             |                          | 50                 |                    | ns    |
| T <sub>end1,2,3</sub>     |                             |                          | 100                |                    | ns    |
| T <sub>read</sub>         |                             | 20pF load                |                    | 100                | ns    |
| <b>Analog Signal Path</b> |                             |                          |                    |                    |       |
| f <sub>c</sub>            | Filter Center Frequency     | Post 40kHz Calibration   | 39                 | 41                 | kHz   |
| f <sub>-3dB LP</sub>      | Filter Low-Pass -3dB        |                          | f <sub>c</sub> + 2 |                    | kHz   |
| f <sub>-3dB HP</sub>      | Filter High-Pass -3dB       |                          | f <sub>c</sub> - 2 |                    | kHz   |
|                           | Gain (minimum PGA setting)  |                          | 49                 |                    | dB    |
|                           | Gain (maximum PGA setting)  |                          | 73                 |                    | dB    |
| <b>Bias</b>               |                             |                          |                    |                    |       |
|                           | RBIAS pin stray capacitance |                          |                    | 10                 | pF    |
|                           | RBIAS resistor value        | 1% tolerance             | 10                 |                    | kΩ    |

- (1) Electrical Characteristic values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested
- (2) Rise and Fall Times are ensured by design and not production tested.
- (3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material

## Applications and Design Considerations

### Application Schematic<sup>(1)</sup>



(1) Minimize stray capacitance at device pins IN and RBIAS.

**Figure 7: TS8000 Application Schematic**

### Power Supply Recommendations

The TS8000 was designed to be operated from a 3.3V power supply. The voltage range for DVDD is shown in *Recommended Operating Conditions*. Power supply accuracy of 10% or better is advised. The internal LDO output should be bypassed with a 1μF capacitor at the AVDD pin.

### Capacitor Selection

To achieve the best performance, C1, C2, and C3 should have low ESR / ESL, and a self-resonant frequency above the maximum input signal bandwidth. Typically, size 0402 or smaller is better for high self-resonance.

### Layout Guidelines

Optimum performance can be achieved with the TS8000 by adhering to the following layout guidelines which will help minimize performance degradation due to layout parasitics and noise. The following guidelines are assuming the implementation of the application schematic shown in Figure 7.

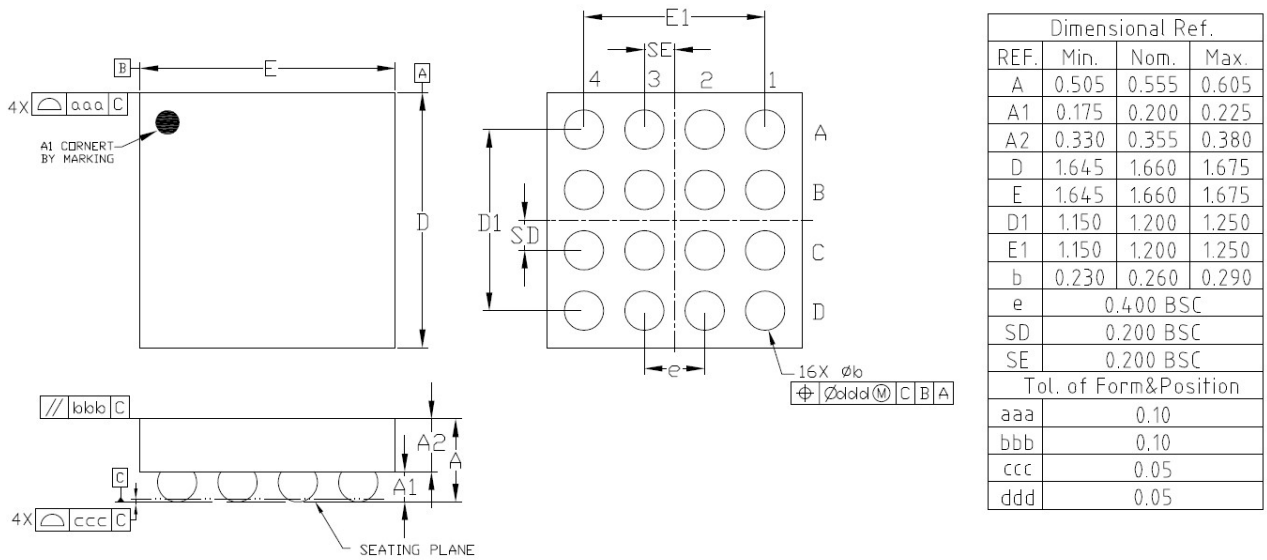
- 1) C1, C2, and C3 should be placed as close as practical to their respective AVDD, DVDD, and BYPREF package bumps
- 2) Shield the IN net with ground fills
- 3) Minimize routing lengths on the IN and RBIAS
- 4) The DATA and CLK outputs should be routed over a solid ground plane



## Part Packaging Information

### Package Drawing

The TS8000 – Ultrasonic to Digital Converter is packaged as a 16 bump WLCSP. Figure 8 shows the WLCSP configuration. Recommended Land Pattern is 0.200mm for each bump (per IPC 7351A guidelines).



### Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Figure 8: TS8000 Outline Drawing

### Date Code

The manufacturing date code is printed on the package as described in Section 14 of this document. The date code has the format of YYWW where YY is the last 2 digits of the manufacturing year, and WW is the week of manufacture in the year.

Pin List

| #  | Pin Name | Pin Type             | Pin Description                                                                                                 |
|----|----------|----------------------|-----------------------------------------------------------------------------------------------------------------|
| A1 | LDOOUT   | Supply               | LDO output. Internally connected to AVDD. Externally connect LDOOUT to AVDD. Bypass with 1µF capacitor at AVDD. |
| A2 | AVDD     | Supply               | Power. Internally connected to LDOOUT. Externally connect AVDD to LDOOUT. Bypass with 1µF capacitor.            |
| A3 | RBIAS    | Input                | 1% 10k resistor for bias.                                                                                       |
| A4 | IN       | Input                | Detector input.                                                                                                 |
| B1 | AOUT     | Analog Output        | Analog signal path output.                                                                                      |
| B2 | NC       |                      | Not internally connected.                                                                                       |
| B3 | NC       |                      | Not internally connected.                                                                                       |
| B4 | BYPREF   | Input                |                                                                                                                 |
| C1 | LDOOUT2  | Supply               | LDO output. Internally connected to AVDD. Externally connect LDOOUT2 to AVDD or leave floating.                 |
| C2 | NC       |                      | Not internally connected.                                                                                       |
| C3 | AVSS2    | Supply               | Ground. Internally connected to AVSS. Connect to ground or leave floating.                                      |
| C4 | AVSS     | Supply               | Ground (must be connected).                                                                                     |
| D1 | DATA     | Digital Input/Output | Data output in normal operation. Data input/output in configuration mode.                                       |
| D2 | CLK      | Digital Input        | Configuration clock input.                                                                                      |
| D3 | NC       |                      | Connect to ground, AVDD, or leave floating.                                                                     |
| D4 | DVDD     | Digital Supply       | LDO input supply and Digital IO power. Bypass with 1µF capacitor.                                               |

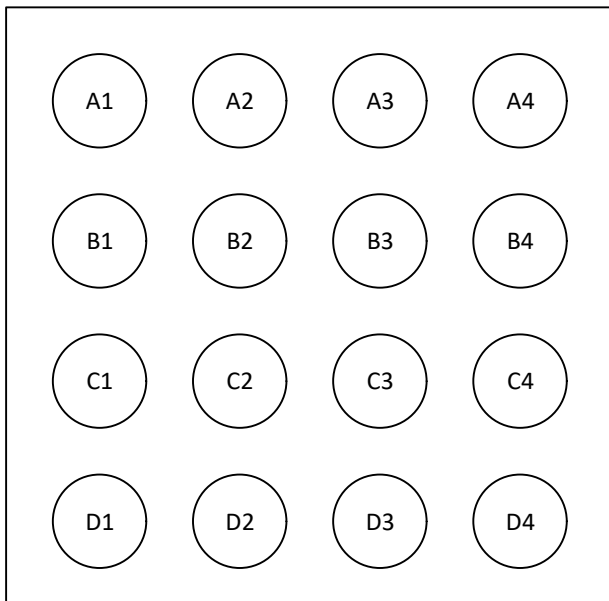


Figure 9: Top View Pin Location

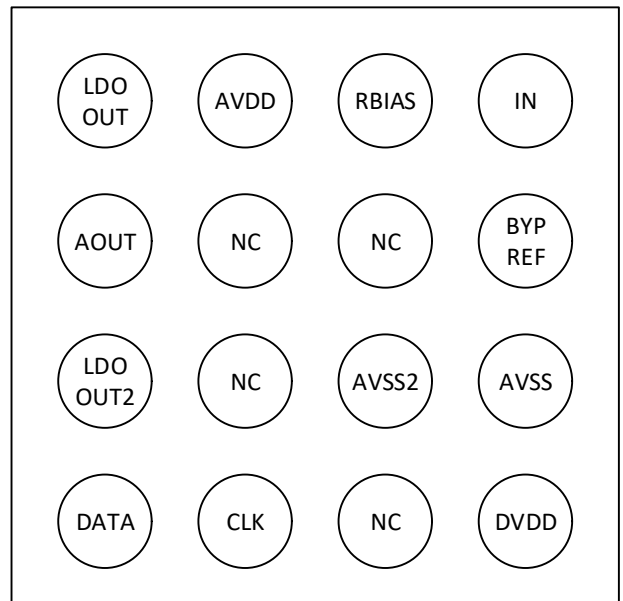
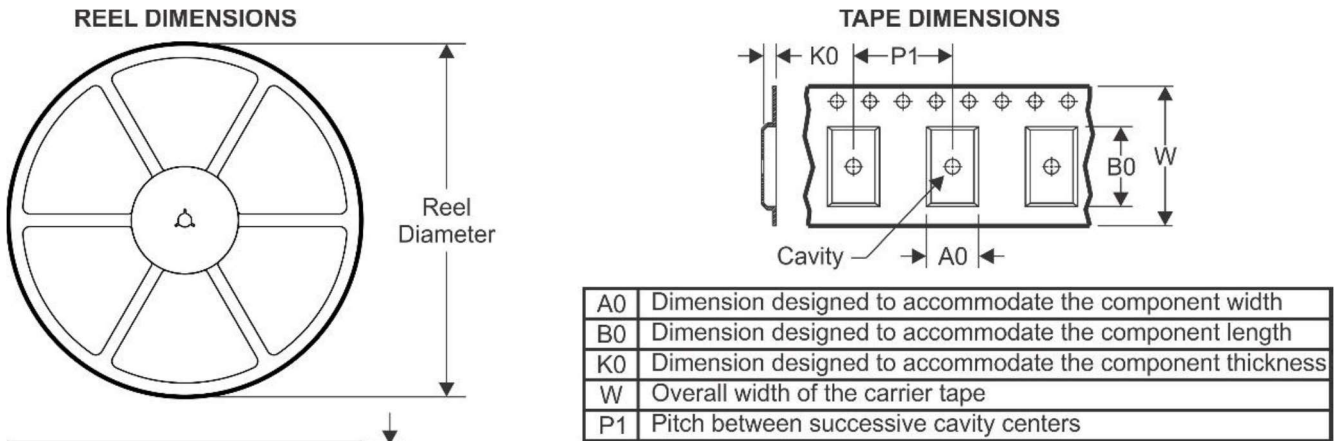


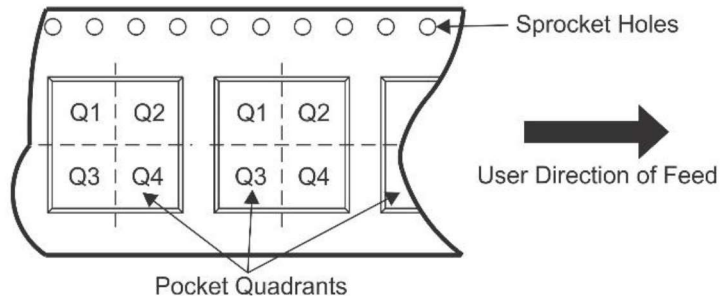
Figure 10: Top View – 4x4 Bump WLCSP IO MAP

## Tape and Reel Packaging

### Tape and Reel Information

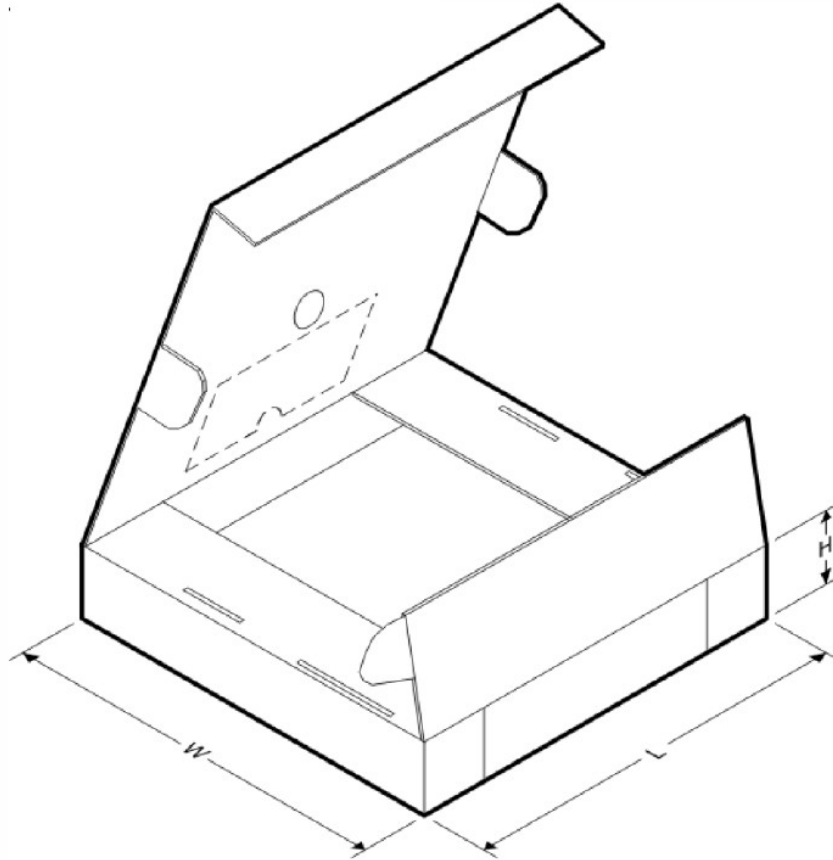


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package Type | Bumps | Qty/ Reel | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin 1 Quadrant |
|--------|--------------|-------|-----------|--------------------|--------------------|---------|---------|---------|---------|--------|----------------|
| TS8000 | WLCSP        | 16    | 4000      | 178.0              | 9.0                | 1.85    | 1.85    | 0.7     | 4.0     | 8.0    | Q1             |

### Tape and Reel Box Dimensions



| Device | Package Type | Bumps | Qty / Reel | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-------|------------|-------------|------------|-------------|
| TS8000 | WLCSP        | 16    | 4000       | 178.0       | 9.0        | 1.85        |

Note: All dimensions are nominal

### Branding

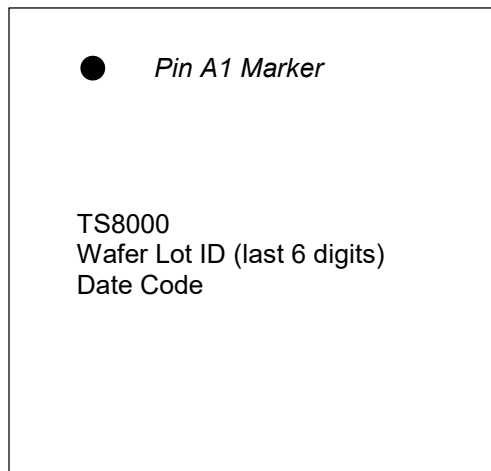


Figure 11: TS8000 Branding Diagram

### Mechanical, Packaging and Handling Information

| Device | Package Type | Bumps | Package Qty | RoHS Plan       | Lead/Ball Finish | MSL Peak Temp       | Op Temp (°C) | Storage Temp (°C) | Device Marking |
|--------|--------------|-------|-------------|-----------------|------------------|---------------------|--------------|-------------------|----------------|
| TS8000 | WLCSP        | 16    | 4000        | RoHS & no Sb/Br | Cu Sn Ag         | Level-1-260C-168 HR | 0 to 85      | -40 to 150        | TS8000         |

#### Electrostatic Discharge Caution



TS8000 is an ESD sensitive device with an HBM rating of Class 1C (2,000V) per JS-001-2014. The device should be placed in conductive foam during storage or handling to prevent damage due to electrostatic discharge. Refer to JESD625 for handling precautions.

#### MSL

TS8000 is an MSL1 device per J-STD-020. Refer to J-STD-033 for specific handling requirements and conditions.

#### Shelf Life

Shelf life is 12 months as per J-STD-033. Refer to J-STD-033 for additional shelf life information.

#### RoHS

TS8000 fully complies with the RoHS Directive 002/95/EC requirements without exemption and is Halogen-Free as defined by IEC 61249-2-21.

### Revision History

| Revision | Modifications             | Modification Date |
|----------|---------------------------|-------------------|
| 1        | Draft Rev 1 Datasheet     | 30 Aug 2017       |
| 1.1      | Draft Rev 1.1 Datasheet   | Xx Sep 2017       |
| 1.2      | Preliminary 1.2 Datasheet | 12 Sep 2017       |

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Triad Semiconductor  
1760 Jonestown Road  
Winston-Salem NC 27103  
United States

[www.triadsemi.com](http://www.triadsemi.com)

[info@triadsemi.com](mailto:info@triadsemi.com)  
[sales@triadsemi.com](mailto:sales@triadsemi.com)

phone: (336) 774-2150  
fax: (336) 774-2140