Audio Jack Detector with Send / End Detect

DESCRIPTION

The DG2592 is an audio jack detector and pop noise control switch IC. It integrates the circuits necessary to detect the presence of a stereo headset with a microphone and send / end control button.

When there is no ear phone detected, the DG2592 connects the microphone bias line to ground through the MIC pin. The DG2592 also gives a logic high signal to the baseband controller through the DET pin.

The DG2592 senses the DC levels at both L_Detect and GND_Detect. When an ear phone is plugged in, the voltage at both pins will go low. The DG2592 will indicate the presence of the ear phone by pulling DET low and the MIC switch will turn off.

The DG2592 is available in small miniQFN10 of 1.4 mm x 1.8 mm x 0.55 mm and ultra thin UTMQFN10 of 0.35 mm thickness.

FEATURES

- Wide operating voltage range: 1.6 V to 5.5 V
- Low quiescent current of 10 μA, max. at V_{DD} = 1.8 V
- Integrated sense comparator for audio L of 1.4 V ± 5 % threshold
- 1.2 Ω/max. MIC bias switch provides quick discharge and clamping
- ESD Protected
  - Human body model > 8 kV
  - Charged device model > 2 kV
  - IEC 61000-4-2 air discharge > 15 kV
  - IEC 61000-4-2 contact discharge > 8 kV
- Ultra thin and compact miniQFN10 and UTDFN10
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Cellular phones
- Tablet devices
- Portable media players
- Digital cameras

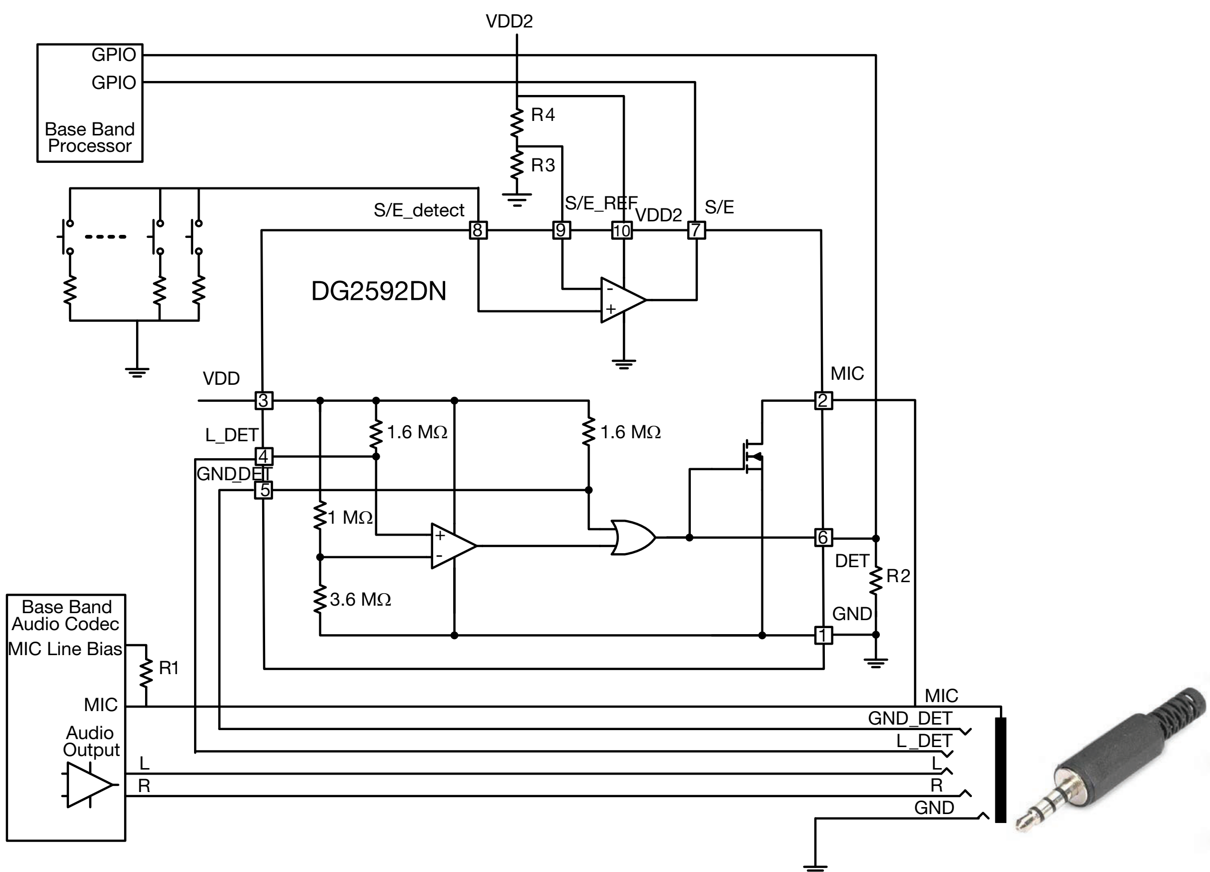


Fig. 1 - Typical Application Circuit

PACKAGE OUTLINE

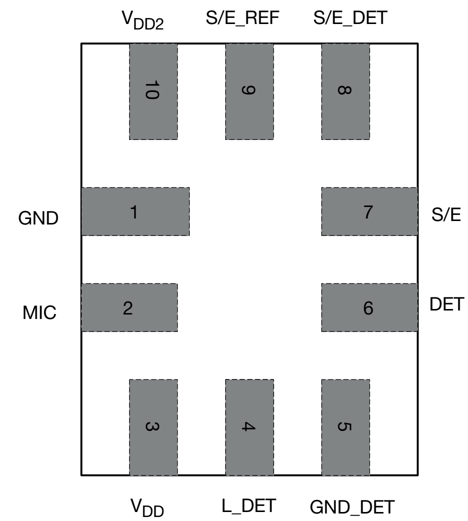
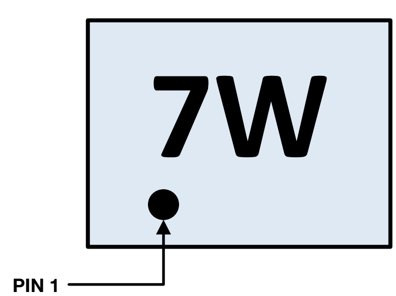


Fig. 2 - Device Pin Out miniQFN10 Top View, Pin 1 Dot Marking is on Top of the Device

PIN DESCRIPTION			
PIN#	**NAME**	**TYPE**	**FUNCTION**
1	GND	Power	Ground
2	MIC	Output	Microphone bias switch input
3	V_{DD}	Power	Power supply for ear jack plug in detection circuit. A bypass capacitor of 0.1 μF is recommended as close as possible to this pin
4	L_DET	Input	Connected to L_DET pin at audio jack
5	GND_DET	Input	Connect to GND_DET pin at audio jack
6	DET	Output	Detect logic output connected to baseband controller
7	S/E	Output	S/E detect comparator output
8	S/E_DET	Input	Non-inverting input of S/E press detection comparator
9	S/E_REF	Input	Inverting input of S/E press detection comparator. External voltage is provided as press detection reference threshold
10	V_{DD2}	Power	Power supply pin for the S/E detection circuit. A bypass capacitor of 0.1 μF is recommended as close as possible to this pin

ORDERING INFORMATION					
PART NUMBER	**FUNCTION**	**TEMPERATURE RANGE**	**PACKAGE**	**SIZE**	**REEL QUANTITY**
DG2592DN-T1-GE4	Audio jack detector with S/E detect	-40 °C to 85 °C	miniQFN-10	1.4 mm x 1.8 mm x 0.55 mm	3000
DG2592DN1-T1-GE4			UTMQFN-10	1.4 mm x 1.8 mm x 0.35 mm	3000

DEVICE MARKING



7 = DG2592 Marking Code, W = Date / Lot Traceability Code

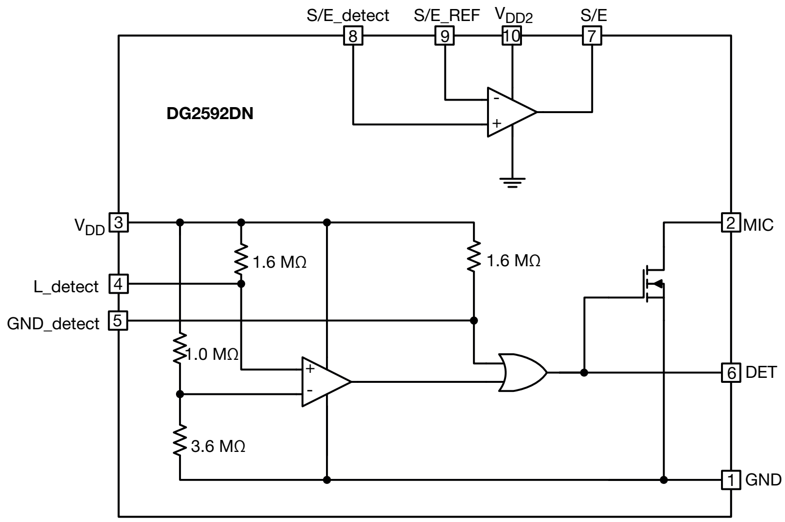


Fig. 3 - Functional Block Diagram

TRUTH TABLE

INPUTS		OUTPUTS		AUDIO JACK
L_DET	GND_DET	DET	MIC	
0	0	Low	High	Detected
1	0	High	Low	Not detected
0	1	High	Low	Not detected
1	1	High	Low	Not detected

ABSOLUTE MAXIMUM RATINGS

PINS OR PARAMETERS	CONDITIONS		LIMITS	UNIT
V_{DD}, V_{DD2}	Reference to GND		-0.3 to 6	V
L_Detect, GND_Detect, DET	Reference to GND		-0.3 V to V_{DD}	
S/E_DET, S/E_REF, S/E	Reference to GND		-0.3 V to V_{DD2}	
MIC			-0.3 to 6	
Storage Temperature			-65 to +150	°C
MSL	Moisture sensitivity level (JEDEC® J-STD-020)		1	Level
I_{MIC}	Switch DC current		200	mA
$I_{MICPEAK}$	Switch peak current (pulsed at 1 ms, < 10 % duty cycle)		500	
Latch Up Current	JESD78		± 600	
ESD	Human body model; ANSI / ESDA / JEDEC JS-001		> 8000	V
	Charged device model; JESD22-C101		> 2000	
	Machine model; JESD22-A115		> 400	
	IEC61000-2-4, level 4 L_DET, GND_DET, MIC and GND pins	Contact	> 8000	
		Air	> 15 000	
RECOMMENDED OPERATING CONDITION				
V_{DD}, V_{DD2}			1.6 to 5.5	V
Ear Jack Detection Input Pins			0 to V_{DD}	V
S/E Press Detection Input Pins			0 to V_{DD2}	V
MIC Bias Voltage			0 to 5.5	V
Operating Junction Temperature			-40 to +125	°C

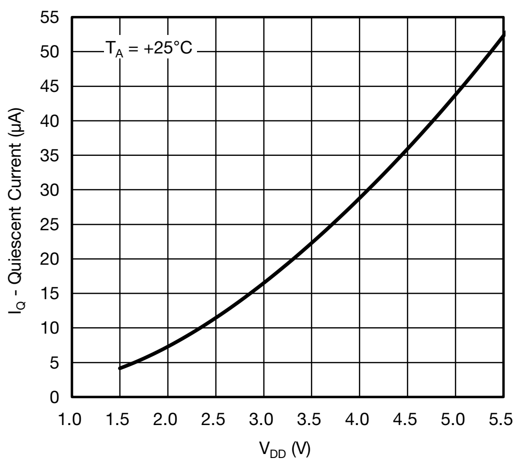
Note

- The control logic pins should not float and should be set to either high or low logic levels.

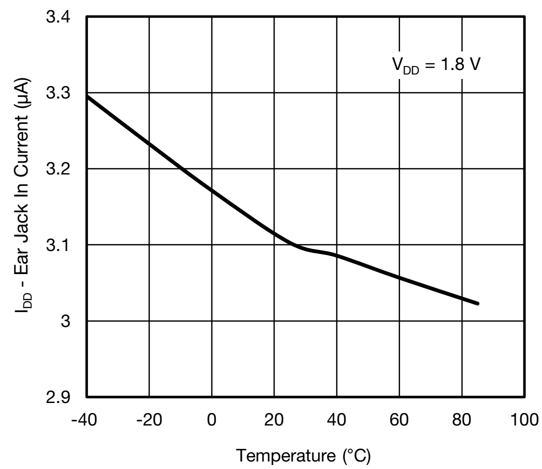
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED, V_{DD} = 1.8 V, V_{DD2} = 2.1 V, T_A = -40 °C to 85 °C, TYPICAL VALUES are at 25 °C	LIMITS MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_Q	L_Detect, GND_Detect are open	-	6	10	μA
Ear Jack In Current	I_{DD}	L_Detect, GND_Detect are connected with 10 kΩ to GND	-	3	6	μA
S/E Detection Current	I_{DD2}	S/E_DET =0 V, S/E_REF = 1.05 V	-	2	3.5	μA
L_Detect Reference Voltage	V_{TH_L}	L_DET switching low to high	1.33	1.4	1.5	V
Propagation Delay to DET	t_{PLH}	C_{OUT} = 15 pF, GND_DET = 0 V, L_DET = 1.52 V to DET = 0.9 V	80	149	300	ns
Propagation Delay to DET	t_{PHL}	C_{OUT} = 15 pF, GND_DET = 0 V, L_DET = 1.31 V to DET = 0.9 V	130	325	550	ns
Low Voltage L_DET Leakage	IL_{L_DET}	L_DET = 0 V	-	0.84	2	μA
High Voltage L_DET Leakage	IH_{L_DET}	L_DET = 1.8 V	-	30	-	pA
L_DET Input Capacitance	C_{L_DET}		-	4	-	pF
GND_Detect Logic Low Voltage	V_{IL_GND}		0.63	0.86	-	V
GND_Detect Logic High Voltage	V_{IH_GND}		-	0.89	1.17	V
GND_DET Propagation Delay to DET	t_{PGND_DET}	C_{OUT} = 15 pF, R_L = 1 MΩ, L_DET = 0 V, GND_DET switches between 0 V and 1.8 V	-	10	-	ns
Low Voltage GND_DET Leakage	I_{IL}	GND_DET = 0 V	-	0.93	2	μA
High Voltage GND_DET Leakage	I_{IH}	GND_DET = 1.8 V	-	80	-	pA
GND_DET Input Capacitance	C_{G_DET}	f = 1 MHz	-	3.5	-	pF
MIC Pull Down Resistance	R_{MIC}	I_{MIC} = 1 mA L_Detect, GND_Detect = open	-	-	1.25	Ω
MIC Leakage		V_{MIC} = 2.4 V	-1	-	1	μA
DET Pull Up Resistance	$R_{OUT}H$	L_Detect, GND_Detect = open	-	135	200	Ω
DET Pull Down Resistance	$R_{OUT}L$	L_Detect, GND_Detect are connected with 10 kΩ to GND	-	120	200	Ω
DET High Logic Voltage	$V_{OUT}H$	I_{DET} = 0.1 mA, L_Detect, GND_Detect = open	1.6	-	-	V
DET Low Logic Voltage	$V_{OUT}L$	I_{DET} = 0.1 mA, L_Detect, GND_Detect are connected with 10 kΩ to GND	-	-	0.3	V
DET Rise Time	t_{DET_R}	C_{OUT} = 15 pF, R_L = 1 MΩ, DET = 10 % to 90 %	-	14	-	ns
DET Fall Time	t_{DET_F}	C_{OUT} = 15 pF, R_L = 1 MΩ, DET = 90 % to 10 %	-	4.4	-	ns
Propagation Delay to S/E	$t_{PS/E}$	C_{OUT} = 15 pF, R_L = 1 MΩ, V_{CM} = mid-supply, 100 mV overdrive	50	170	500	ns
Input Leakage	I_{SE_IN}	V_{CM} = 0.9 V	-	4	-	pA
Input Capacitance	C_{SE_IN}	f = 1 MHz	-	3.5	-	pF
Voltage Output Low	V_{OL}	I_{OL} = 0.1 mA	-	-	0.2	V
Voltage Output High	V_{OH}	I_{OH} = 0.1 mA	1.9	-	-	V
Rise Time	t_{S/E_R}	C_{OUT} = 15 pF, R_L = 1 MΩ, S/E = 10 % to 90 %	-	16	-	ns
Fall Time	t_{S/E_F}	C_{OUT} = 15 pF, R_L = 1 MΩ, S/E = 90 % to 10 %	-	12.1	-	ns

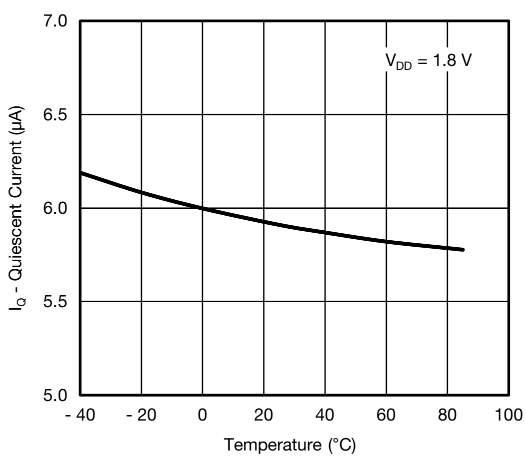
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



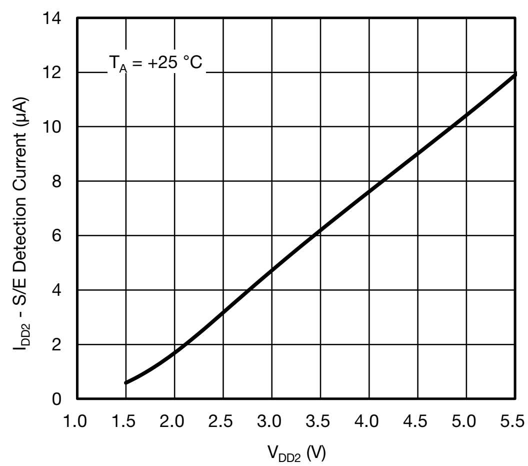
Quiescent Current vs. V_{DD}



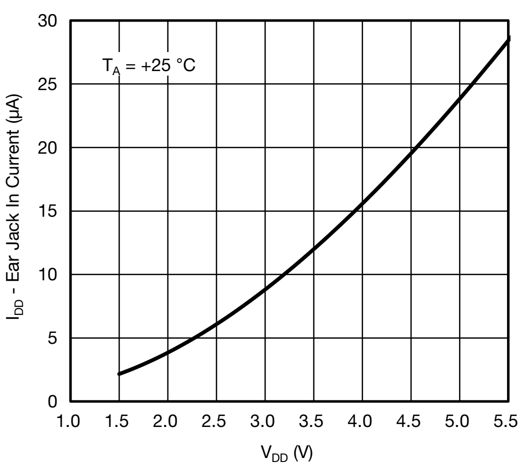
Ear Jack In Current vs. Temperature



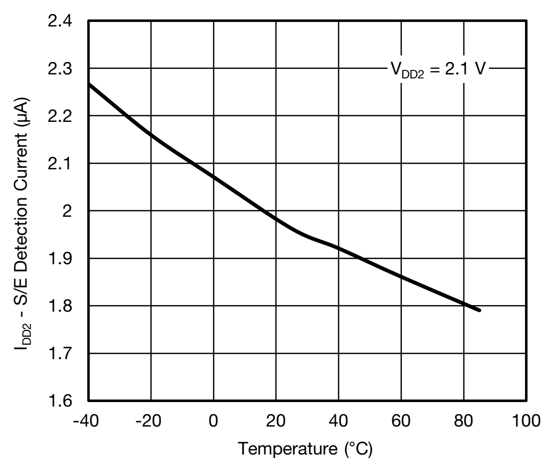
Quiescent Current vs. Temperature



S/E Detection Current vs. V_{DD2}

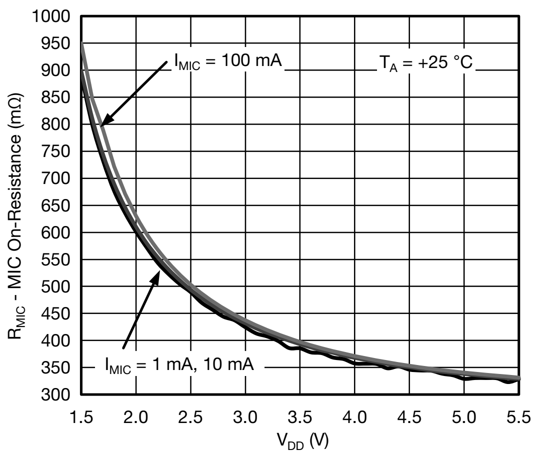


Ear Jack In Current vs. V_{DD}

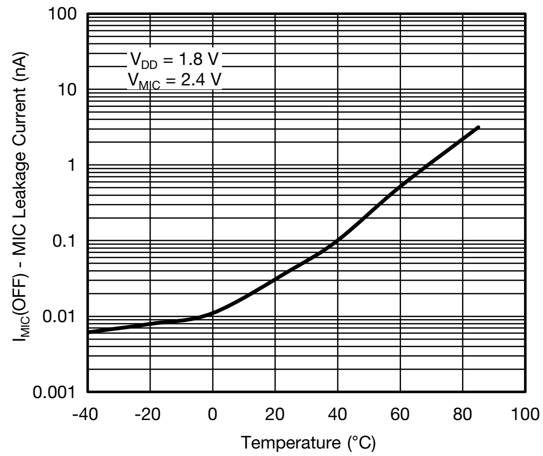


S/E Detection Current vs. Temperature

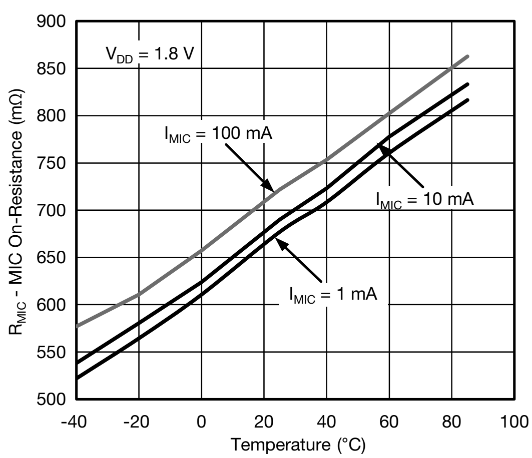
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



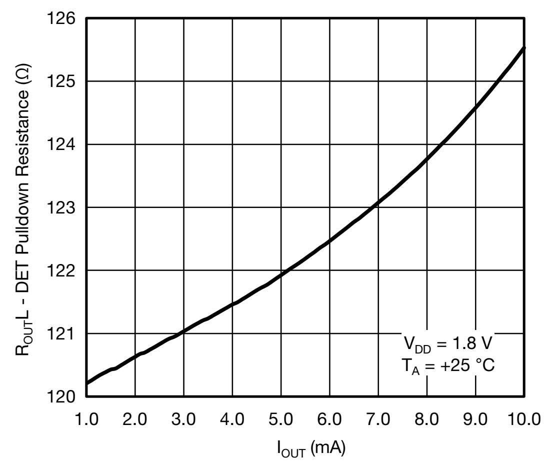
MIC On Resistance vs. V_{DD}



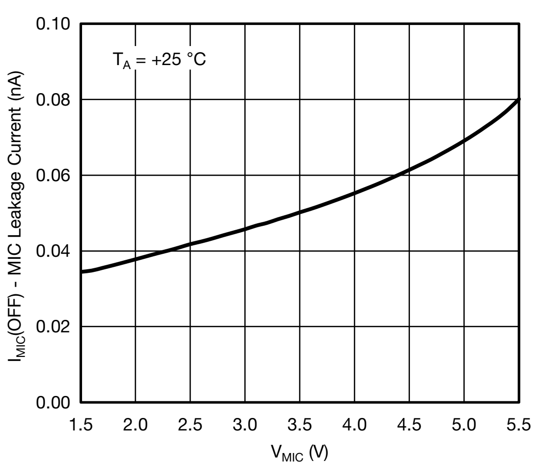
MIC Leakage Current vs. Temperature



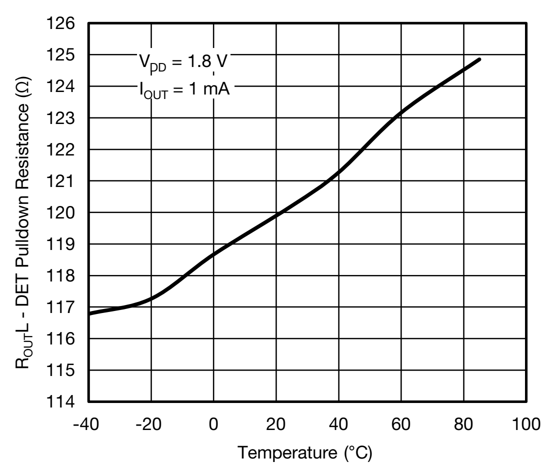
MIC On Resistance vs. Temperature



DET Pulldown Resistance vs. I_{OUT}

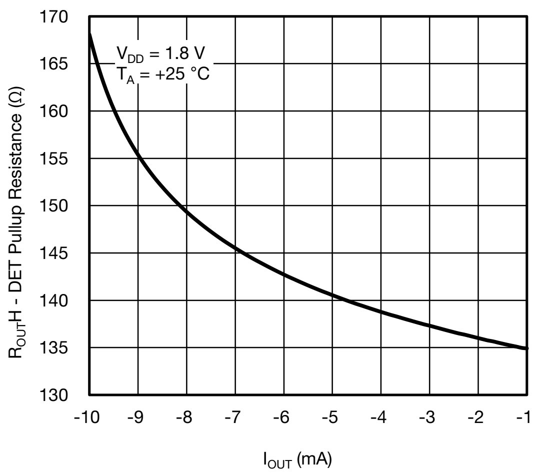


MIC Leakage Current vs. V_{MIC}

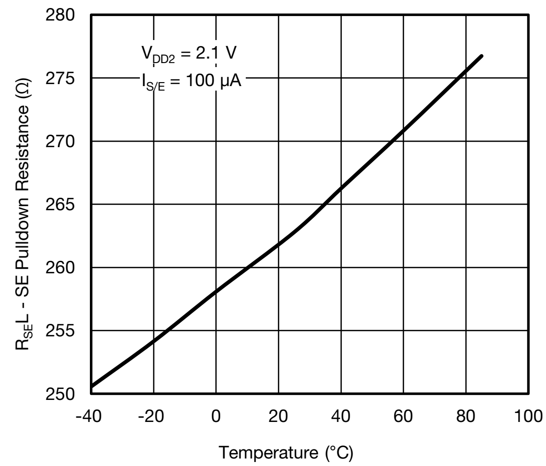


DET Pulldown Resistance vs. Temperature

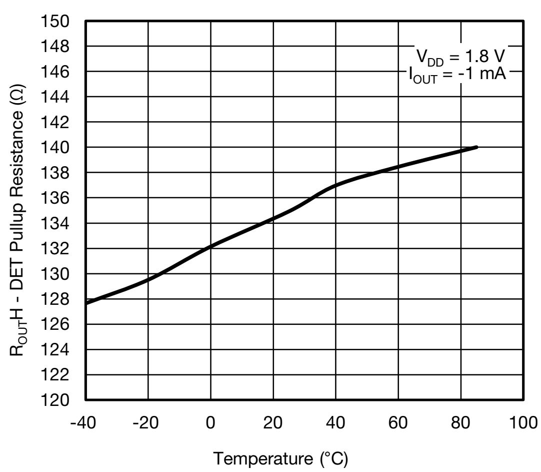
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



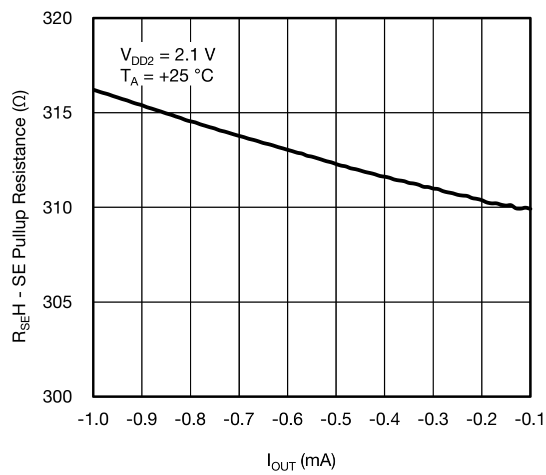
DET Pullup Resistance vs. I_{OUT}



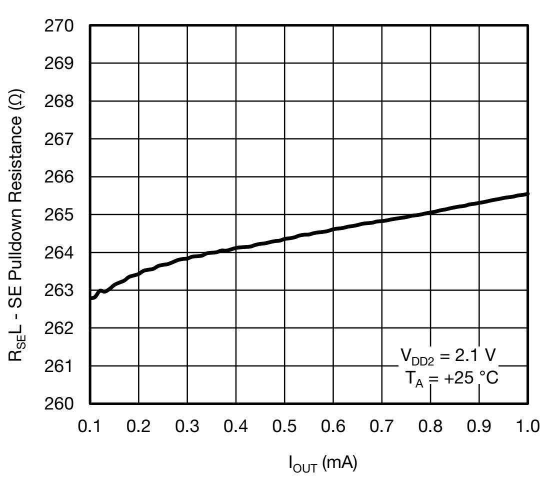
SE Pulldown Resistance vs. Temperature



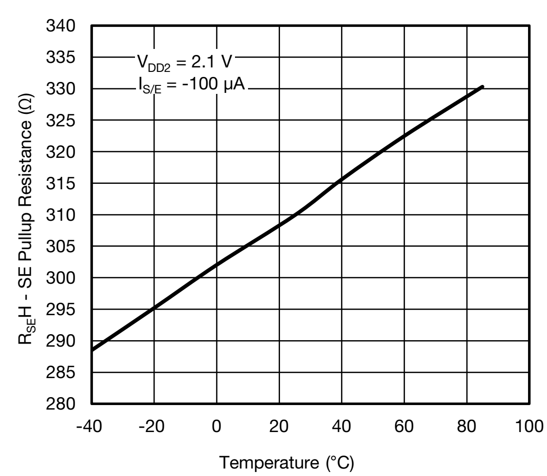
DET Pullup Resistance vs. Temperature



SE Pullup Resistance vs. I_{OUT}

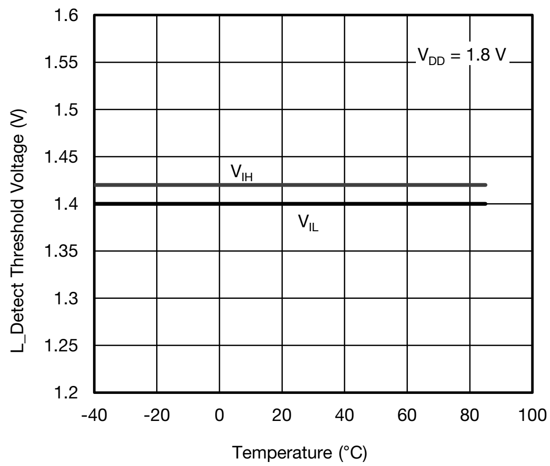


SE Puldown Resistance vs. I_{OUT}

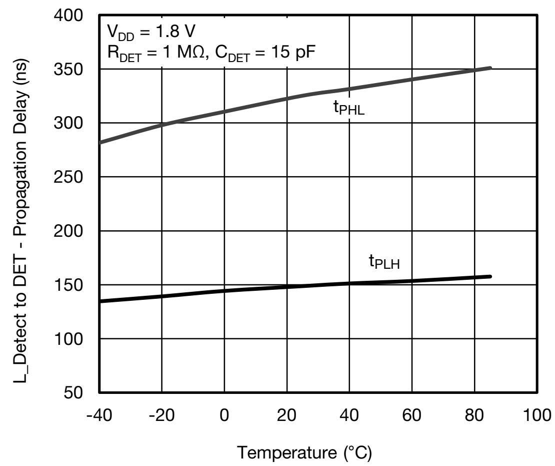


SE Pullup Resistance vs. Temperature

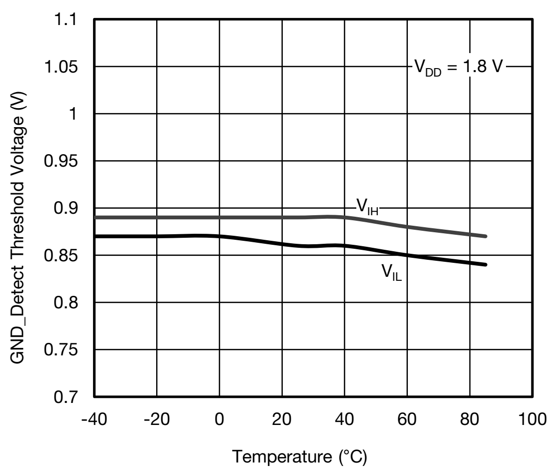
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



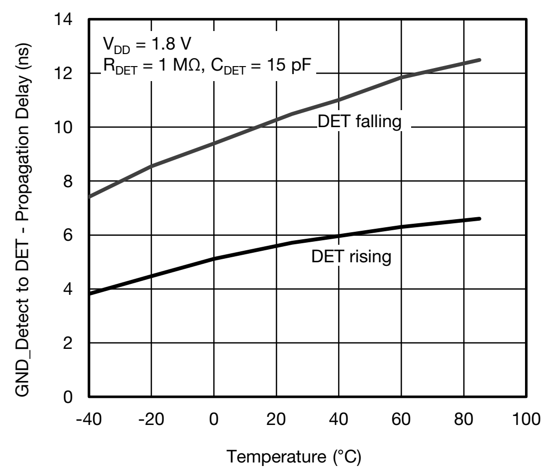
L_Detect Threshold Voltage vs. Temperature



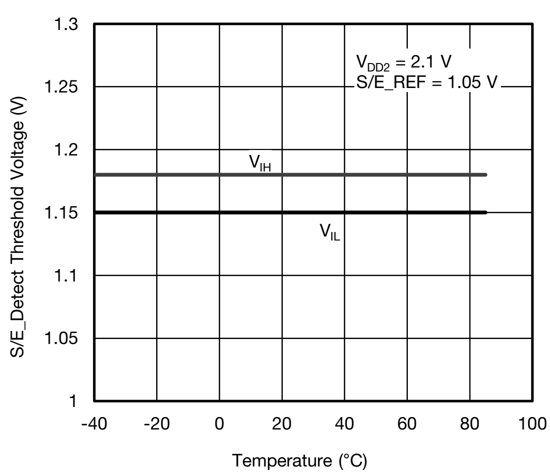
L_Detect to DET Propagation Delay vs. Temperature



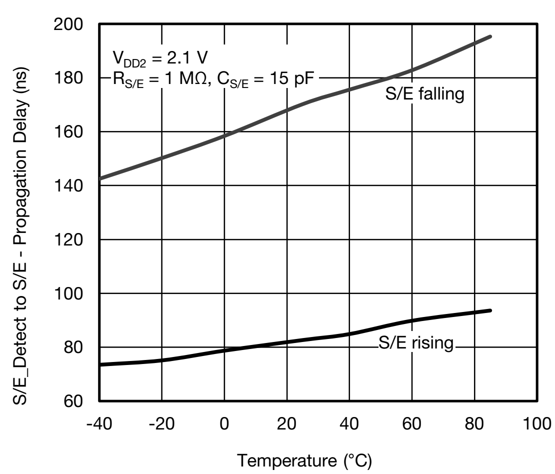
GND_Detect Threshold Voltage vs. Temperature



GND_Detect to DET Propagation Delay vs. Temperature

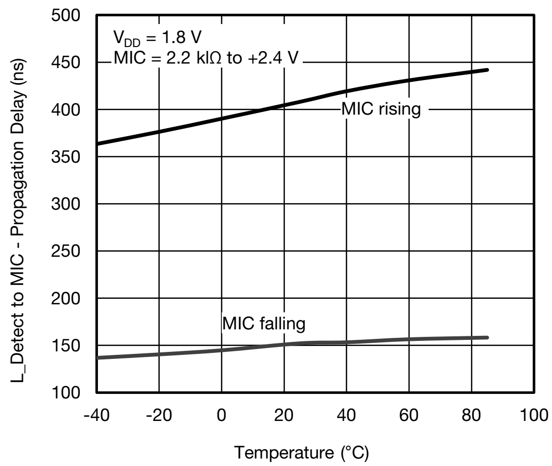


S/E_Detect Threshold Voltage vs. Temperature

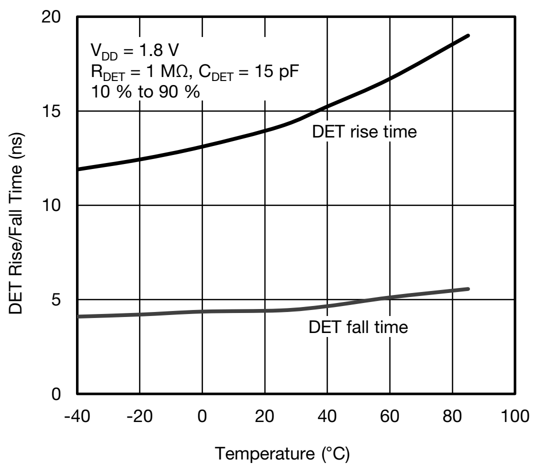


S/E_Detect to S/E Propagation Delay vs. Temperature

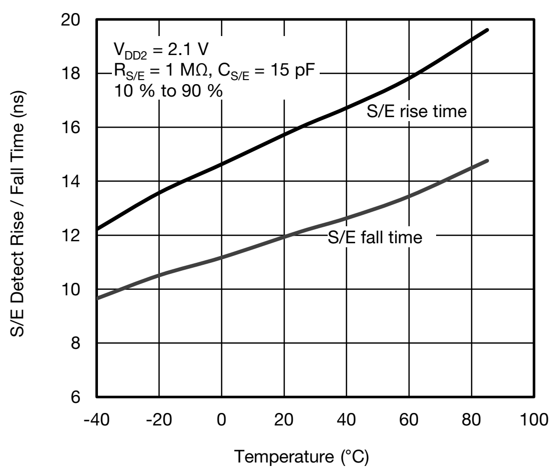
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



L_Detect to MIC Propagation Delay vs. Temperature



DET Rise / Fall Time vs. Temperature



S/E_Detect to Rise / Fall Time vs. Temperature

TEST CIRCUIT

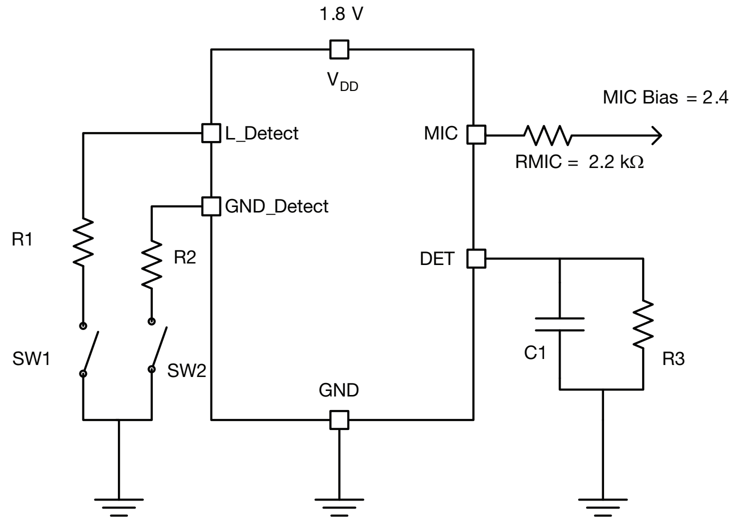


Fig. 4 - Test Circuit

TIMING DIAGRAM

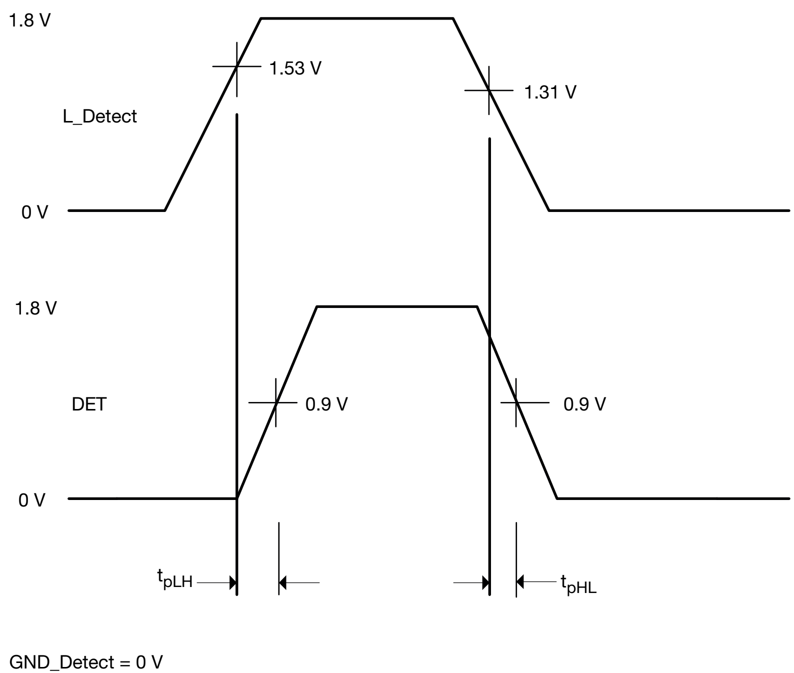


Fig. 5 - Timing Diagram

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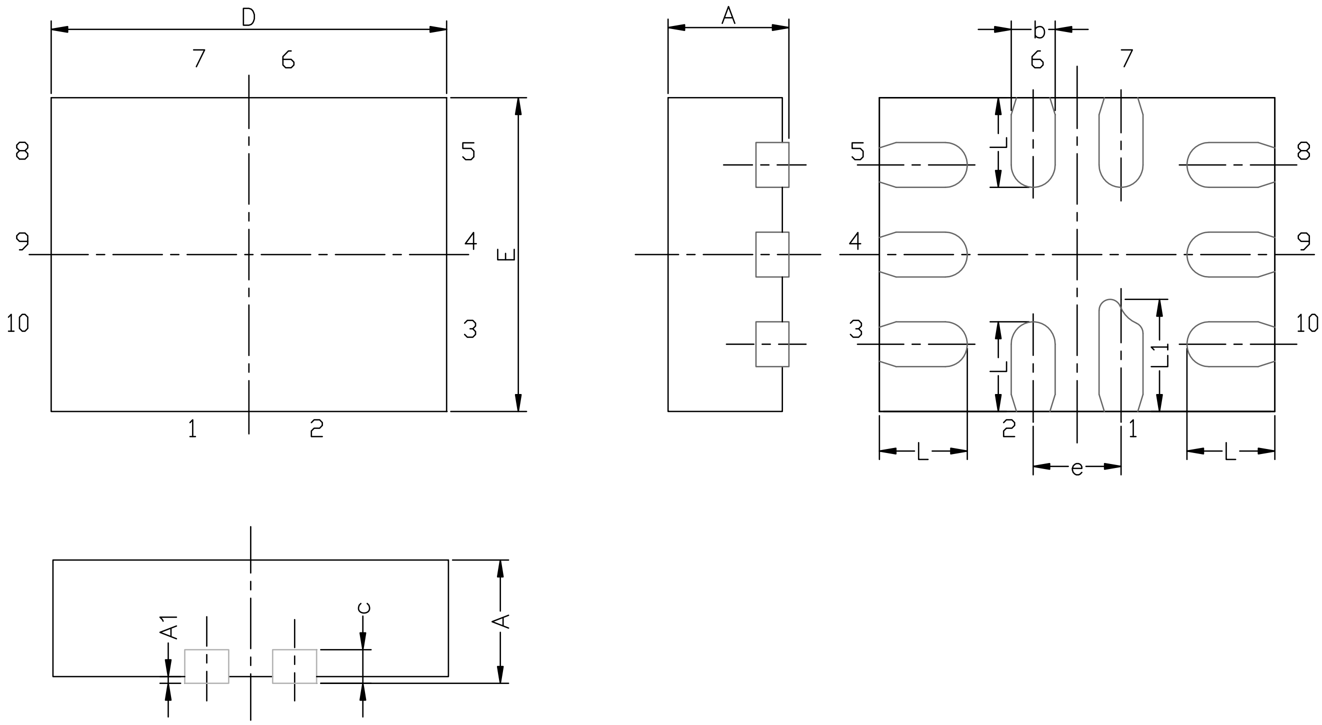
MINI QFN-10L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.45	0.55	0.60	0.0177	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.150 or 0.127 REF (1)			0.006 or 0.005 REF (1)		
D	1.70	1.80	1.90	0.067	0.071	0.075
E	1.30	1.40	1.50	0.051	0.055	0.059
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

Note

(1) The dimension depends on the leadframe that assembly house used.

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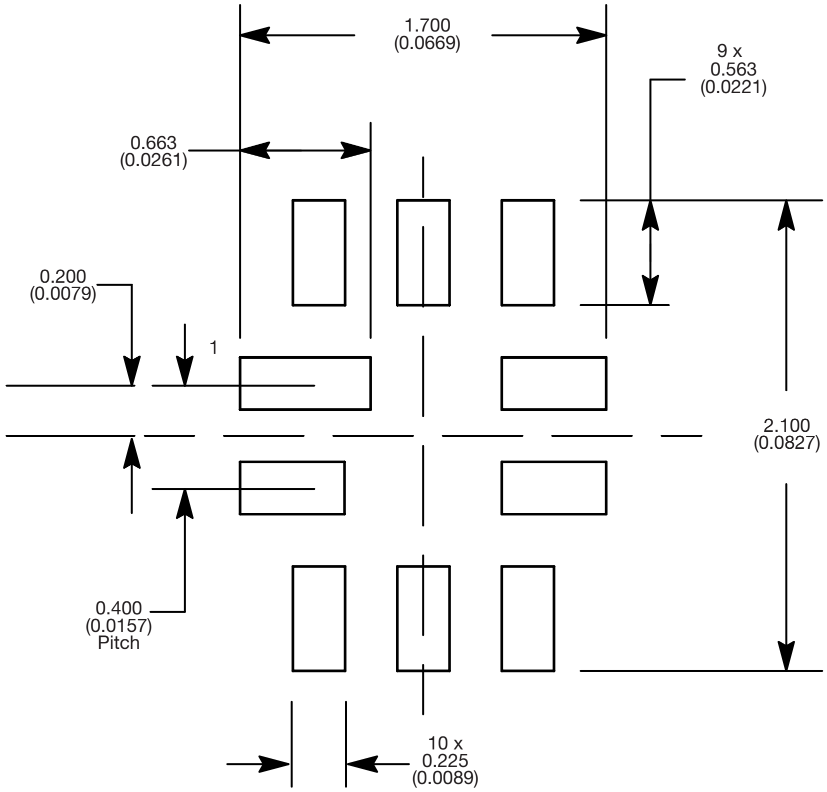
DWG: 5957

RECOMMENDED MINIMUM PADS FOR MINI QFN 10L



Mounting Footprint
Dimensions in mm (inch)

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