

# MAX V and MAX II CPLD Features

PRODUCT LINE		MAX V CPLDS <sup>1</sup>						MAX II CPLDS <sup>1</sup>							
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z	EPM240Z	EPM570Z	EPM240	EPM570	EPM1270	EPM2210	
Resources	LEs	40	80	160	240	570	1,270	2,210	-	-	-	-	-	-	
	Equivalent macrocells <sup>2</sup>	32	64	128	192	440	980	1,700	192	440	192	440	980	1,700	
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0	4.7	5.4	7.5	9.0	6.2	7.0	
	User flash memory (Kb)	8	8	8	8	8	8	8	8	8	8	8	8	8	
	Logic convertible to memory <sup>3</sup>	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	-	-	-	-	-	
Clocks, Maximum I/O Pins, and Architectural Features	Internal oscillator	✓	✓	✓	✓	✓	✓	✓	-	-	-	-	-	-	
	Fast power-on reset	✓	✓	✓	✓	✓	✓	✓	-	-	-	-	-	-	
	Boundary-scan JTAG	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	JTAG ISP	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Fast input registers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Programmable register power-up	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	JTAG translator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Real-time ISP	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	MultiVolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0 <sup>4</sup>			1.5, 1.8, 2.5, 3.3				1.5, 1.8, 2.5, 3.3, 5.0 <sup>4</sup>	
	I/O power banks	2	2	2	2	2	4	4	2	2	2	2	4	4	
	Maximum output enables	54	54	79	114	159	271	271	80	160	80	160	212	272	
	LVTTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	LVDS outputs	✓	✓	✓	✓	✓	✓	✓	-	-	-	-	-	-	
	32 bit, 66 MHz PCI compliant	-	-	-	-	-	✓ <sup>4</sup>	✓ <sup>4</sup>	-	-	-	-	✓ <sup>4</sup>	✓ <sup>4</sup>	
	Schmitt triggers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Programmable slew rate	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
	Programmable pull-up resistors	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
Programmable GND pins	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Open-drain outputs	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Bus hold	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		

Package Options and I/O Pins<sup>5</sup>

E64 pin (9 mm, 0.4 mm pitch)	54	54	54	-	-	-	-	-	-	-	-	-	-
T100 pin <sup>6</sup> (16 mm, 0.5 mm pitch)	-	79	79	79	74	-	-	-	-	80	76	-	-
T144 pin <sup>6</sup> (22 mm, 0.5 mm pitch)	-	-	-	114	114	114	-	-	-	-	116	116	-
M64 pin (4.5 mm, 0.5 mm pitch)	30	30	-	-	-	-	-	-	-	-	-	-	-
M68 pin (5 mm, 0.5 mm pitch)	-	52	52	52	-	-	-	54	-	-	-	-	-
M100 pin (6 mm, 0.5 mm pitch)	-	-	79	79	74	-	-	80	76	80	76	-	-
M144 pin (7 mm, 0.5 mm pitch)	-	-	-	-	-	-	-	-	116	-	-	-	-
M256 pin (11 mm, 0.5 mm pitch)	-	-	-	-	-	-	-	-	160	-	160	212	-
U256 pin (14 mm, 0.8 mm pitch)	-	-	-	-	-	-	-	-	-	-	-	-	-
F100 pin (11 mm, 1.0 mm pitch)	-	-	-	-	-	-	-	-	-	80	76	-	-
F256 pin (17 mm, 1.0 mm pitch)	-	-	-	-	159	211	204	-	-	-	160	212	204
F324 pin (19 mm, 1.0 mm pitch)	-	-	-	-	-	271	271	-	-	-	-	-	272

Notes:

- All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit [www.intel.com/fpga](http://www.intel.com/fpga).
- Typical equivalent macrocells.
- Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.

- An external resistor must be used for 5.0 V tolerance.
- For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Intel's online selector guide.
- Thin quad flat pack (TQFP).

54 Number indicates available user I/O pins.

Pin migration (same Vcc, GND, ISP, and input pins). User I/Os may be less than labelled for pin migration.