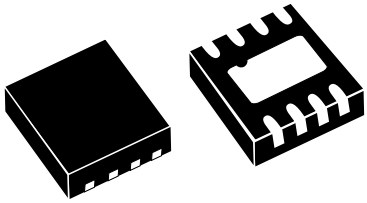
STBP112

Overvoltage protection device

Datasheet - production data

Features

- Input overvoltage protection up to 28 V
- Integrated high voltage N-channel MOSFET switch - low $R_{DS(on)}$ of 165 mΩ
- Integrated charge pump
- Maximum continuous current of 2 A
- Thermal shutdown
- Soft-start feature to control the inrush current
- Enable input ($\overline{EN}$)
- Fault indication output ($\overline{FLT}$)
- IN input ESD protection: ±15 kV air discharge, ±8 kV contact discharge (with 1 µF input capacitor), ±2 kV HBM (standalone device)
- Certain overvoltage options compliant with the China Communications Standard YD/T 1591-2006 (overvoltage protection only)
- Small, RoHS compliant 2 x 2 x 0.75 mm TDFN 8-lead package with thermal pad.



TDFN 8-lead (2 x 2 x 0.75 mm)

Applications

- Smart phones
- Digital cameras
- PDA and palmtop devices
- MP3 players
- Low power handheld devices.

This is information on a product in full production. www.st.com

Contents

1 **Description** 6

2 **Pin description** 7

2.1 Input (IN) 7

2.2 Output (OUT) 7

2.3 Fault indication output ($\overline{FLT}$) 7

2.4 Enable input ($\overline{EN}$) 7

2.5 No connect (NC) 8

2.6 Ground (GND) 8

3 **Operation** 10

3.1 Power-up 10

3.2 Normal operation 10

3.3 Undervoltage lockout (UVLO) 10

3.4 Overvoltage lockout (OVLO) 10

3.5 Thermal shutdown 11

4 **Timing diagrams** 12

5 **Typical operating characteristics** 14

Typical operating characteristics (STBP112CV) 15

6 **Maximum rating** 25

7 **DC and AC parameters** 26

8 **Application information** 28

8.1 Calculating the power dissipation 28

8.2 Calculating the junction temperature 28

8.3 PCB layout recommendations 29

9 **Package information** 30

10 **Tape and reel information** 32

11 Part numbering 35

12 Package marking information 36

13 Revision history 37

List of tables

Table 1. Pin description and signal names . . . 8
Table 2. Absolute maximum ratings . . . 25
Table 3. Thermal data . . . 25
Table 4. Operating and AC measurement conditions . . . 26
Table 5. DC and AC characteristics . . . 26
Table 6. Package mechanical dimensions for TDFN 8-lead (2 x 2 x 0.75 mm) . . . 31
Table 7. Carrier tape dimensions . . . 32
Table 8. Further tape and reel information . . . 32
Table 9. Reel dimensions . . . 33
Table 10. Ordering information scheme . . . 35
Table 11. Marking description . . . 36
Table 12. Document revision history . . . 37

List of figures

Figure 1. Logic diagram . . . 6
Figure 2. Pinout . . . 6
Figure 3. Block diagram . . . 9
Figure 4. Typical application circuit . . . 9
Figure 5. Power-up . . . 12
Figure 6. Overvoltage protection . . . 12
Figure 7. Disable ($\overline{EN}$ = high) . . . 12
Figure 8. Recovery from OVP . . . 13
Figure 9. Maximum load current at T_A = 50 °C and 85 °C for various PCB thermal performance and T_J ≤125 °C . . . 14
Figure 10. Maximum load current vs. ambient temperature for R_{thJA} = 59 K/W and T_J ≤125 °C . . . 14
Figure 11. Startup, t_{on} . . . 15
Figure 12. Overvoltage, t_{off} . . . 15
Figure 13. Recovery from overvoltage, t_{rec} . . . 16
Figure 14. Disable, t_{dis} . . . 16
Figure 15. Startup to overvoltage . . . 17
Figure 16. Startup to overvoltage (detail) . . . 17
Figure 17. Soft-start performance for 10 µF capacitive load . . . 18
Figure 18. Soft-start performance for 100 µF capacitive load . . . 18
Figure 19. I_{CC} vs. temperature at V_{IN} = 5 V . . . 19
Figure 20. I_{CC} vs. V_{IN} . . . 19
Figure 21. I_{CC} vs. V_{IN} (detail) . . . 19
Figure 22. $I_{CC(STDBY)}$ vs. temperature at V_{IN} = 5 V . . . 20
Figure 23. $I_{CC(STDBY)}$ vs. V_{IN} . . . 20
Figure 24. $I_{CC(STDBY)}$ vs. V_{IN} (detail) . . . 20
Figure 25. V_{OVLO} vs. temperature . . . 21
Figure 26. V_{UVLO} vs. temperature . . . 21
Figure 27. $V_{OL(\overline{FLT})}$ vs. temperature at $I_{SINK(\overline{FLT})}$ = 5 mA, V_{IN} = 5 V . . . 21
Figure 28. $R_{DS(on)}$ vs. temperature at 5 V, 1 A . . . 22
Figure 29. $V_{IL(\overline{EN})}$ vs. temperature . . . 22
Figure 30. $V_{IH(\overline{EN})}$ vs. temperature . . . 22
Figure 31. $I_{(\overline{EN})}$ vs. V_{IN} at $V_{(\overline{EN})}$ = 5 V . . . 23
Figure 32. $R_{PD(\overline{EN})}$ vs. temperature at $V_{(\overline{EN})} = V_{IN}$ = 5 V . . . 23
Figure 33. t_{on} vs. temperature . . . 24
Figure 34. t_{rec} vs. temperature . . . 24
Figure 35. Package outline for TDFN 8-lead (2 x 2 x 0.75 mm) . . . 30
Figure 36. Tape and reel . . . 32
Figure 37. Reel dimensions . . . 33
Figure 38. Tape trailer/leader . . . 33
Figure 39. Pin 1 orientation . . . 34

1 Description

The STBP112 device provides overvoltage protection for input voltage up to +28 V. Its low $R_{DS(on)}$ N-channel MOSFET switch protects the systems connected to the OUT pin against failures of the DC power supplies in accordance with the China MII Communications Standard YD/T 1591-2006.

In the event of an input overvoltage condition, the device immediately disconnects the DC power supply by turning off an internal low $R_{DS(on)}$ N-channel MOSFET to prevent damage to protected components.

In addition, the device also monitors its own junction temperature and switches off the internal MOSFET if the junction temperature exceeds the specified limit.

The device can be controlled by the microcontroller and can also provide status information about fault conditions.

The STBP112 is offered in a small, RoHS-compliant 8-lead TDFN (2 mm x 2 mm) package.

Figure 1. Logic diagram

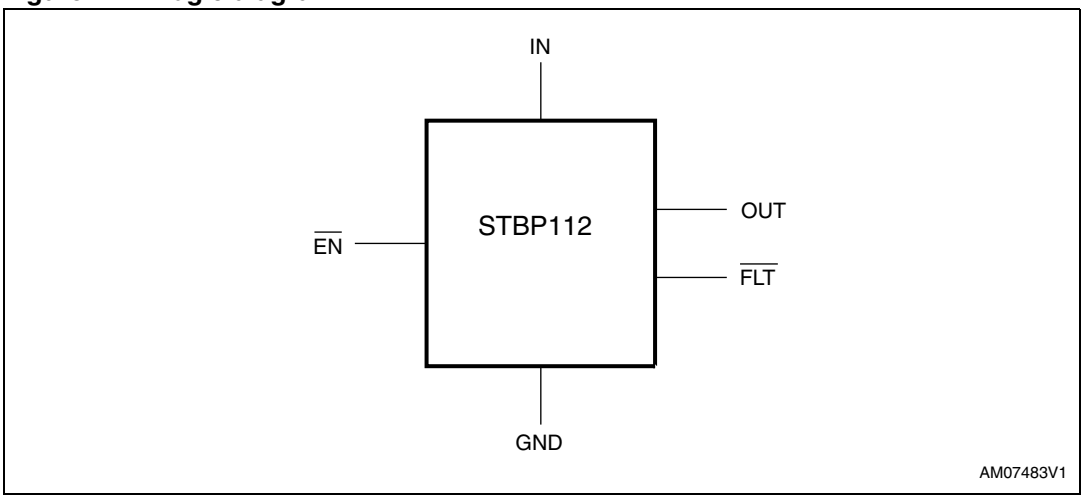
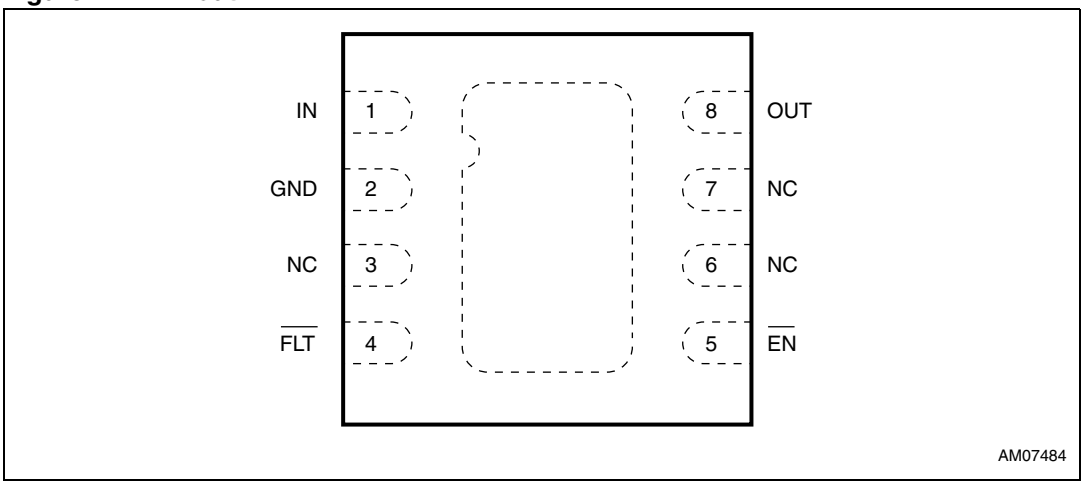


Figure 2. Pinout



1. Exposed thermal pad may be tied to GND.

2 Pin description

2.1 Input (IN)

Input voltage (IN) pin. The IN pin is connected to the DC power supply. An external low ESR ceramic capacitor of minimum value 1 µF must be connected between IN and GND. This capacitor is needed for decoupling and also protects the IC against fast voltage spikes and ESD events. This capacitor should be located as close to the IN pin as possible.

2.2 Output (OUT)

Output voltage (OUT) pin. The OUT pin is connected to the input through a low $R_{DS(on)}$ N-channel MOSFET switch.

If no fault is detected and the STBP112 is enabled by the $\overline{EN}$ input, this switch is turned on and the output voltage follows the input voltage.

The output is disconnected from the input when the input voltage is under the UVLO threshold or above the OVLO threshold, when the junction temperature is above the thermal shutdown threshold or when the device is disabled by the $\overline{EN}$ input.

After the input voltage or junction temperature returns to the specified range, there is a recovery delay, t_{rec}, and the power output is then connected to the input (see *Figure 8 on page 13*).

The switch turn-on time is intentionally prolonged to limit the inrush current and voltage drop caused, for example, by charging output capacitors (soft-start feature).

2.3 Fault indication output ($\overline{FLT}$)

The active low, open-drain fault indication output provides information on the STBP112 state to the application controller. The $\overline{FLT}$ is asserted (i.e. driven low), if the STBP112 is in the overvoltage condition or thermal shutdown mode is active.

As the $\overline{FLT}$ output is of the open-drain type, it may be pulled up by an external resistor R_{PU} to the controller supply voltage (see *Figure 4*). If there is no need to use this output, it may be left disconnected. The suitable R_{PU} resistor value is in the range of 10 kΩ to 1 MΩ.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{FLT} can be connected between the $\overline{FLT}$ output and the controller input (see *Figure 4*). The suitable R_{FLT} resistor value is in the range of 10 kΩ to 100 kΩ.

The $\overline{FLT}$ output is in Hi-Z (high impedance) state when the device is disabled by $\overline{EN}$ input or when the input voltage is lower than the UVLO threshold.

2.4 Enable input ($\overline{EN}$)

This active low logical input can be used to enable or disable the device. When the $\overline{EN}$ input is driven high, the STBP112 is in shutdown mode and the power output is disconnected from the input (see *Figure 8 on page 13*). When the $\overline{EN}$ input is driven low and all operating conditions are within specified limits, the power output is connected to the input.

The $\overline{EN}$ input is equipped with an internal pull-down resistor of 250 kΩ (typical value). If there is no need to use this input, it may be left floating or, preferably, connected to GND.

For V_{IN} lower than 2.5 V (max.), the pull-down resistor is internally disconnected to lower the $\overline{EN}$ pin input current in case the external AC adapter is not connected, the application is running from an internal battery and the STBP112 device is disabled.

To improve safety and to prevent damage to application circuits in the event of extreme voltage or current conditions, an optional protective resistor R_{EN} can be connected between the $\overline{EN}$ input and the controller output (see *Figure 4*). The protective resistor forms a voltage divider with the internal pull-down resistor, which limits the maximum possible R_{EN} value with respect to the $V_{IH(\overline{EN})}$ threshold of $\overline{EN}$ input and the controller's output voltage for logic high, V_{OH}. For the worst case, the highest protective resistor value is

$R_{ENmax} = R_{PD(\overline{EN})min} \times (V_{OH} / V_{IH(\overline{EN})} - 1)$,

where $R_{PD(\overline{EN})min}$ is 100 kΩ and $V_{IH(\overline{EN})}$ is 1.2 V.

For most cases, an R_{EN} value of 10 kΩ to 100 kΩ is adequate.

The $\overline{FLT}$ output is in Hi-Z state when the device is disabled by $\overline{EN}$ input.

2.5 No connect (NC)

Pin 3, 6, and 7 are no connect (NC). They may be left floating or connected to GND.

2.6 Ground (GND)

Ground terminal. All voltages are referenced to GND. The exposed thermal pad is internally connected to GND.

Table 1. Pin description and signal names

Pin	Name	Type	Function
1	IN	Input/supply	Input voltage
2	GND	Supply	Ground
3, 6, 7	NC	-	Not connected
4	$\overline{FLT}$	Output	Fault indication output (open-drain)
5	$\overline{EN}$	Input	Enable input (pull-down resistor to GND)
8	OUT	Output	Output voltage

Figure 3. Block diagram

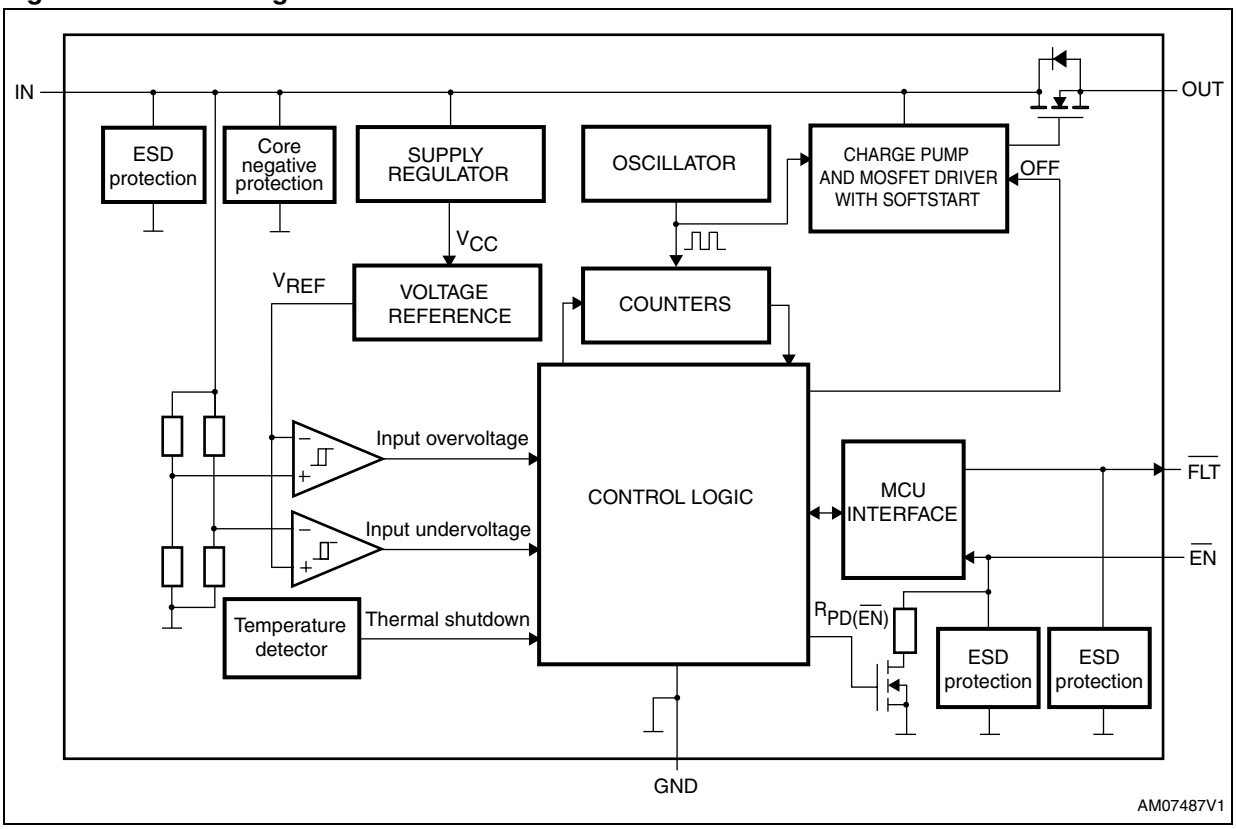
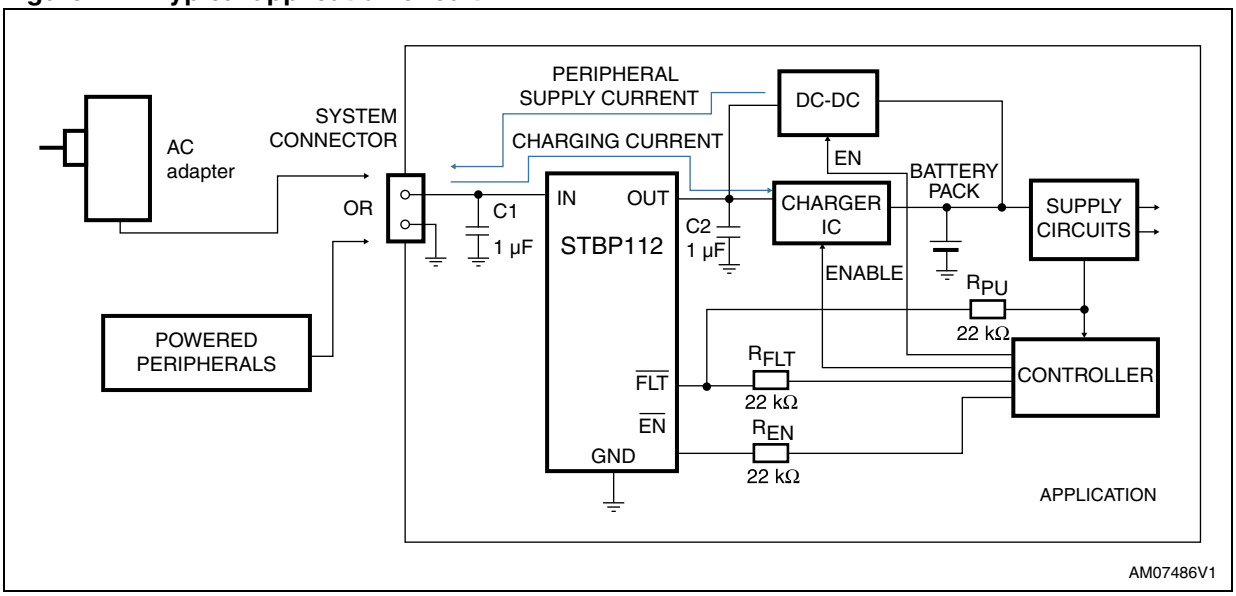


Figure 4. Typical application circuit



1. Optional resistors R_{EN} and R_{FLT} prevent damage to the controller under extreme voltage or current conditions and are not required. Low ESR ceramic capacitor C1 is necessary to ensure proper function of the STBP112. Capacitor C2 is not necessary for STBP112 but may be required by the charger IC.
2. The STBP112 MOSFET switch topology allows the current to flow also in a reverse direction, i.e. from OUT to IN, which can be useful for powering external peripherals from the system connector. If the reverse current (supply current) is undesirable, it may be prevented by connecting an external Schottky diode in series with the OUT pin. The voltage drop between IN and the charger is then increased by the voltage drop across the diode.

3 Operation

The STBP112 provides overvoltage protection for positive input voltage up to 28 V using a built-in low $R_{DS(on)}$ N-channel MOSFET switch.

3.1 Power-up

At power-up, with $\overline{EN}$ = low, the MOSFET switch is turned on after the startup delay, t_{on}, after the input voltage exceeds the UVLO threshold to ensure the input voltage is stabilized (see *Figure 5*).

3.2 Normal operation

The device continuously monitors the input voltage and its own internal temperature so the output voltage is kept within the specified range. The internal MOSFET switch is turned on and the $\overline{FLT}$ output is deasserted.

The STBP112 enters normal operation state if the input voltage returns to the interval between V_{UVLO} and V_{OVLO} - $V_{HYS(OVLO)}$ and the junction temperature falls below T_{off} - $T_{HYS(off)}$. The internal MOSFET is turned on after the t_{rec} delay to ensure that the conditions have stabilized and the $\overline{FLT}$ output is deasserted.

Note: The STBP112 MOSFET switch topology allows the current to flow also in a reverse direction, i.e. from OUT to IN, which can be useful for powering external peripherals from the system connector (see the supply current in Figure 4). At first, the current flows through the MOSFET body diode. If the voltage that appears on the IN terminal is above the UVLO threshold, the MOSFET is (after the startup delay) turned on so the voltage drop across STBP112 is significantly reduced.
If the reverse current is undesirable, it may be prevented by connecting an external, properly rated low drop Schottky diode in series with the OUT pin. The voltage drop between IN and charger is increased by the voltage drop across the diode.

3.3 Undervoltage lockout (UVLO)

To ensure proper operation under any condition, the STBP112 has an undervoltage lockout (UVLO) threshold. When the input voltage is rising, the output remains disconnected from input until the V_{IN} voltage exceeds the V_{UVLO} threshold. This circuit is equipped with hysteresis, $V_{HYS(UVLO)}$, to improve noise immunity under transient conditions.

3.4 Overvoltage lockout (OVLO)

If the input voltage V_{IN} rises above the threshold level V_{OVLO}, the MOSFET switch is immediately turned off. At the same time, the fault indication output $\overline{FLT}$ is activated (i.e. driven low), see *Figure 6*. This device is equipped with hysteresis, $V_{HYS(OVLO)}$, to improve noise immunity under transient conditions.

3.5 Thermal shutdown

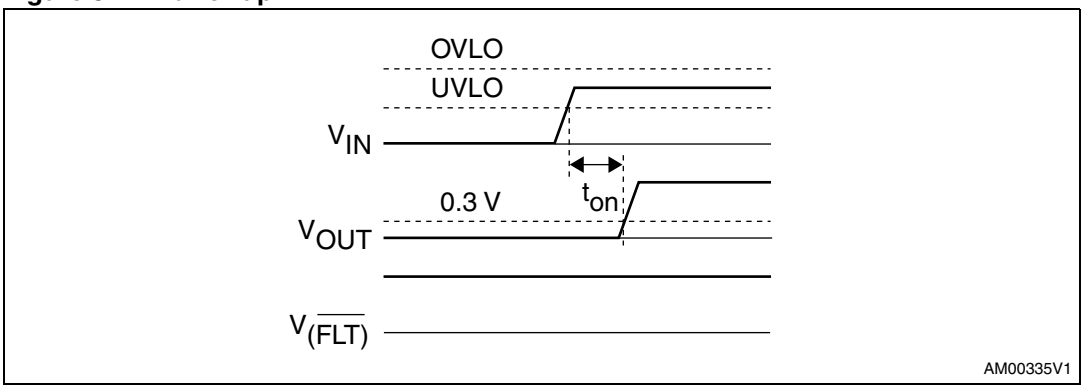
If the STBP112 internal junction temperature exceeds the T_{off} threshold, the internal MOSFET switch is turned off and the fault indication output $\overline{FLT}$ is driven low.

To improve thermal robustness, this circuit has a 20 °C hysteresis, $T_{HYS(off)}$.

Due to the internal reverse diode, the thermal shutdown is not functional for the reverse current.

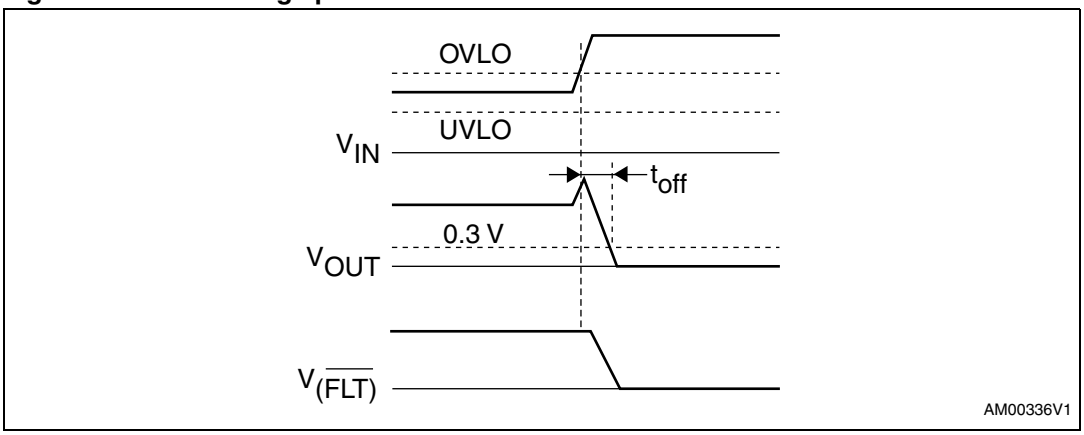
4 Timing diagrams

Figure 5. Power-up



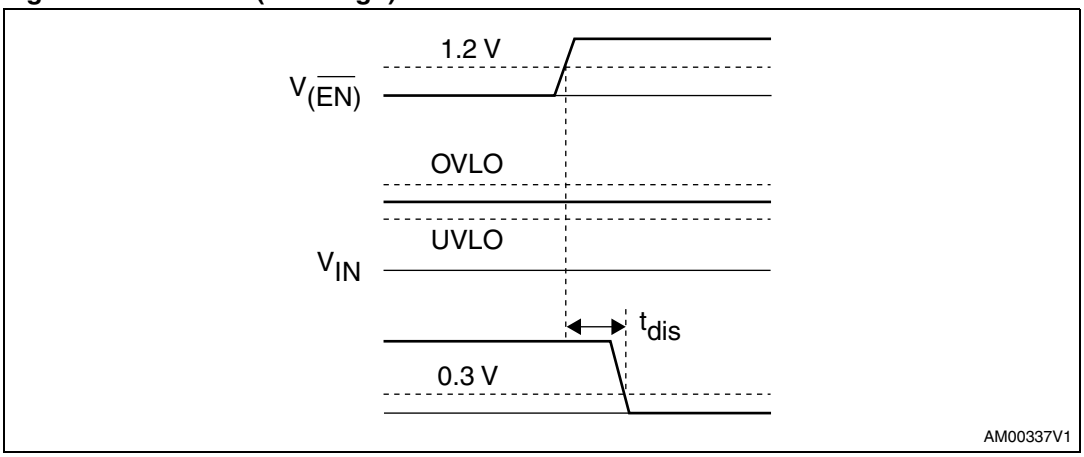
1. $\overline{EN}$ input is low.

Figure 6. Overvoltage protection



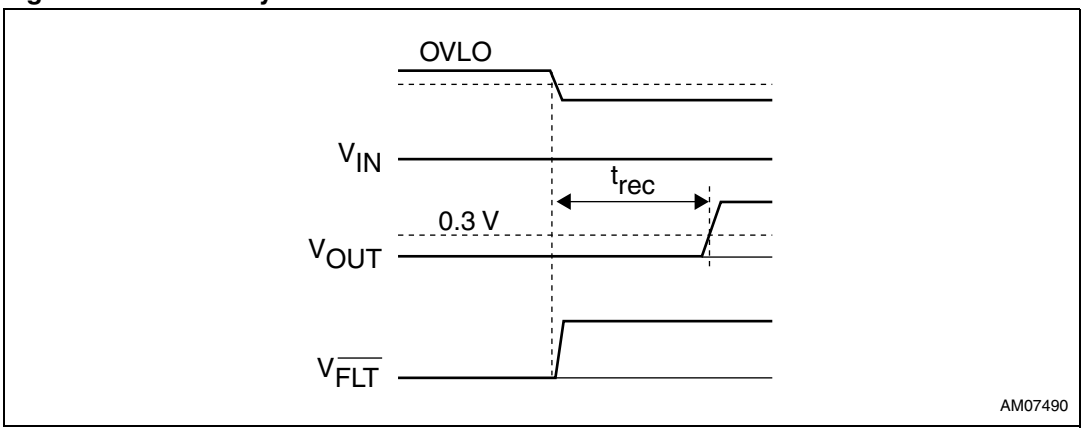
1. $\overline{EN}$ input is low.

Figure 7. Disable ($\overline{EN}$ = high)



1. $\overline{FLT}$ output is in Hi-Z state when $\overline{EN}$ driven high.

Figure 8. Recovery from OVP



1. $\overline{EN}$ input is low.

5 Typical operating characteristics

Figure 9. Maximum load current at T_A = 50 °C and 85 °C for various PCB thermal performance and $T_J \leq 125$ °C

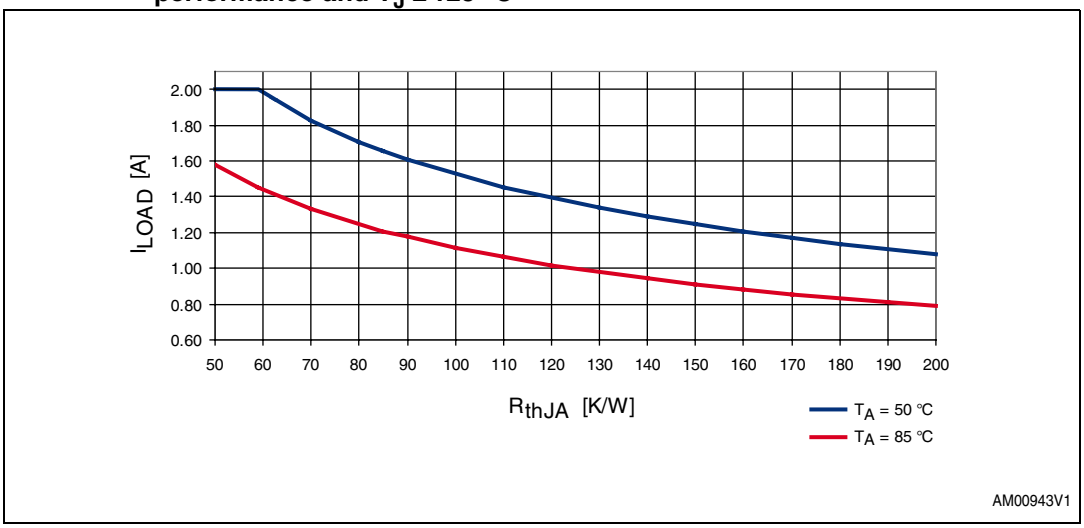
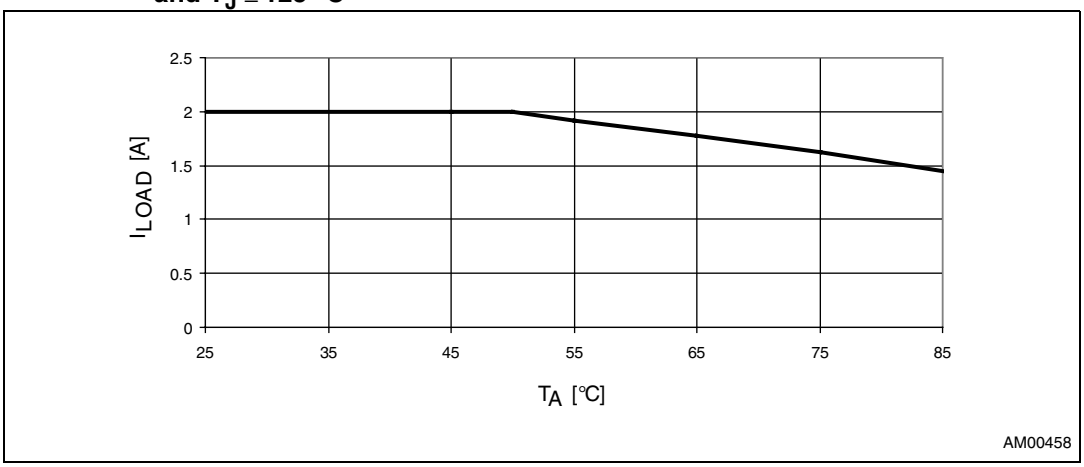
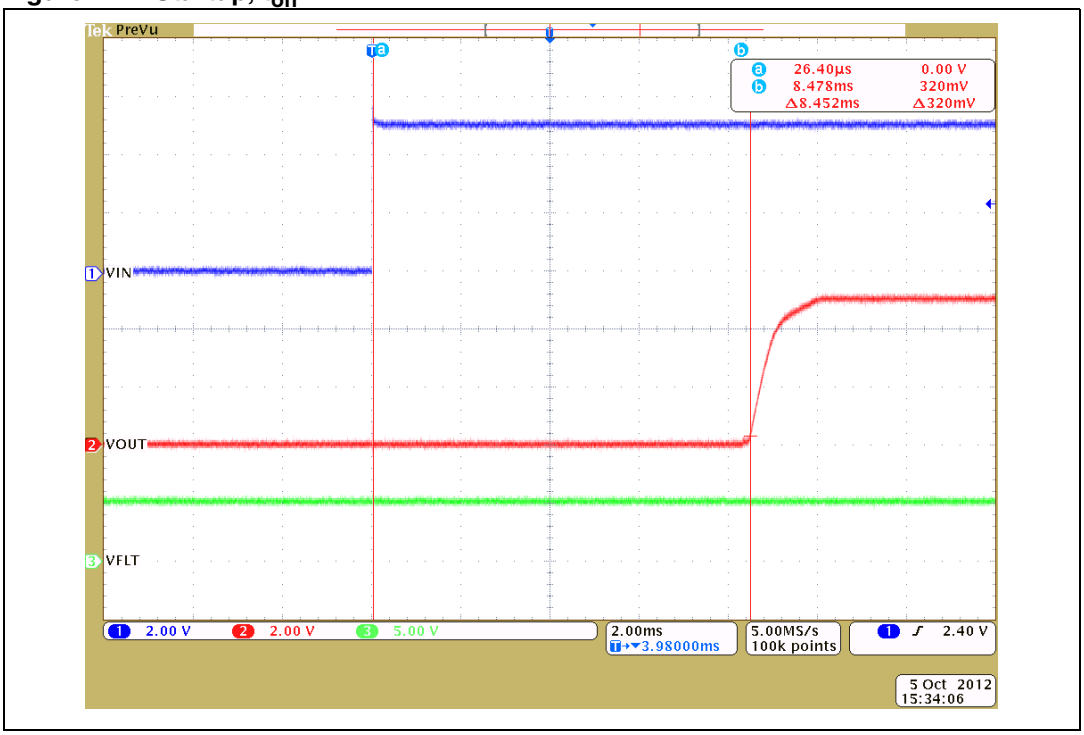


Figure 10. Maximum load current vs. ambient temperature for R_{thJA} = 59 K/W and $T_J \leq 125$ °C



Typical operating characteristics (STBP112CV)

Figure 11. Startup, t_{on}

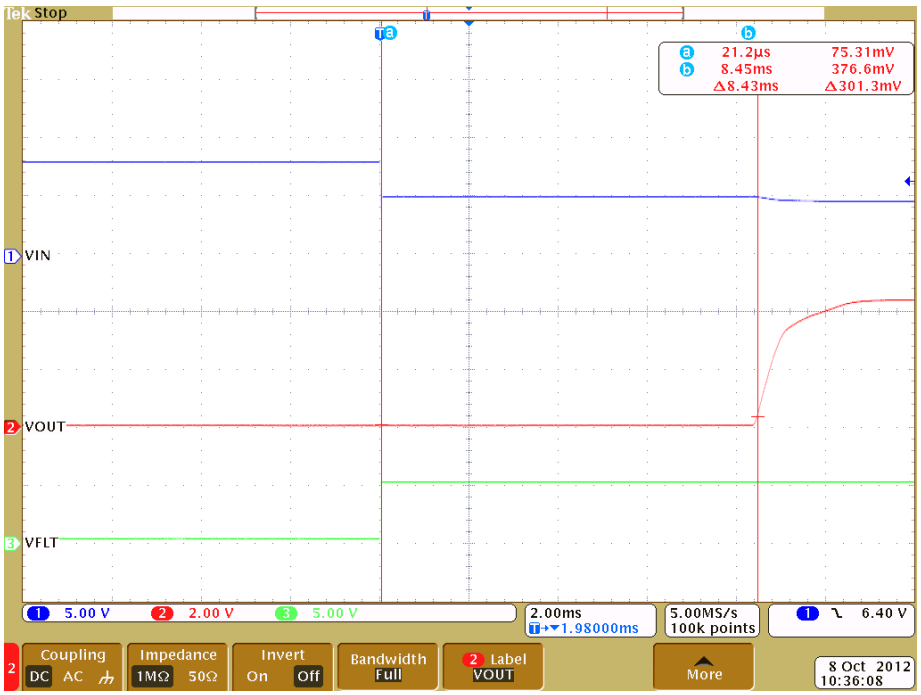


1. Output load is 100 kΩ.

Figure 12. Overvoltage, t_{off}

1. Output load is 5 Ω.

Figure 13. Recovery from overvoltage, t_{rec}

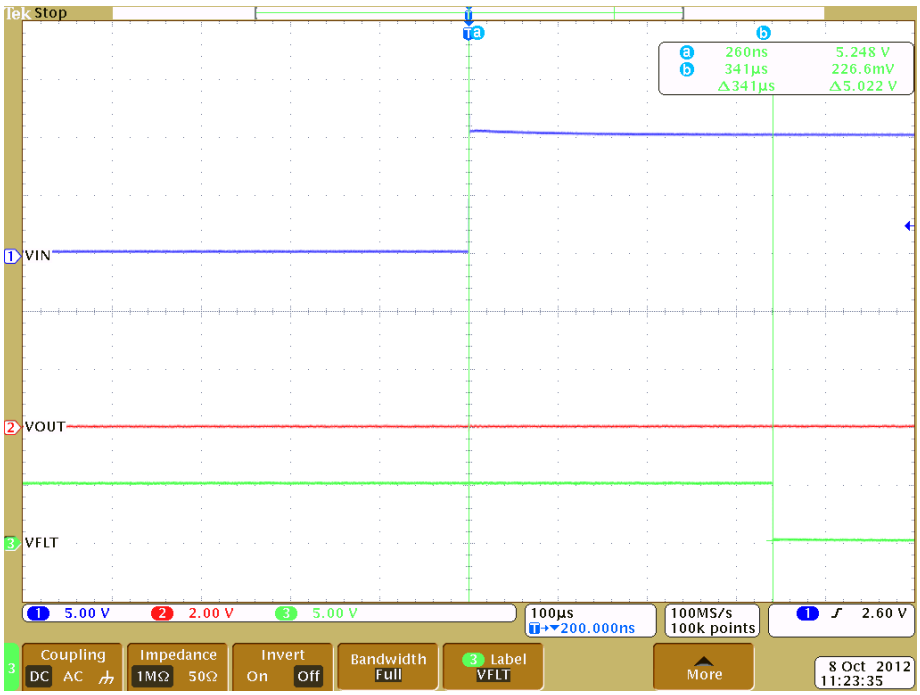


1. Output load is 5 Ω.

Figure 14. Disable, t_{dis}

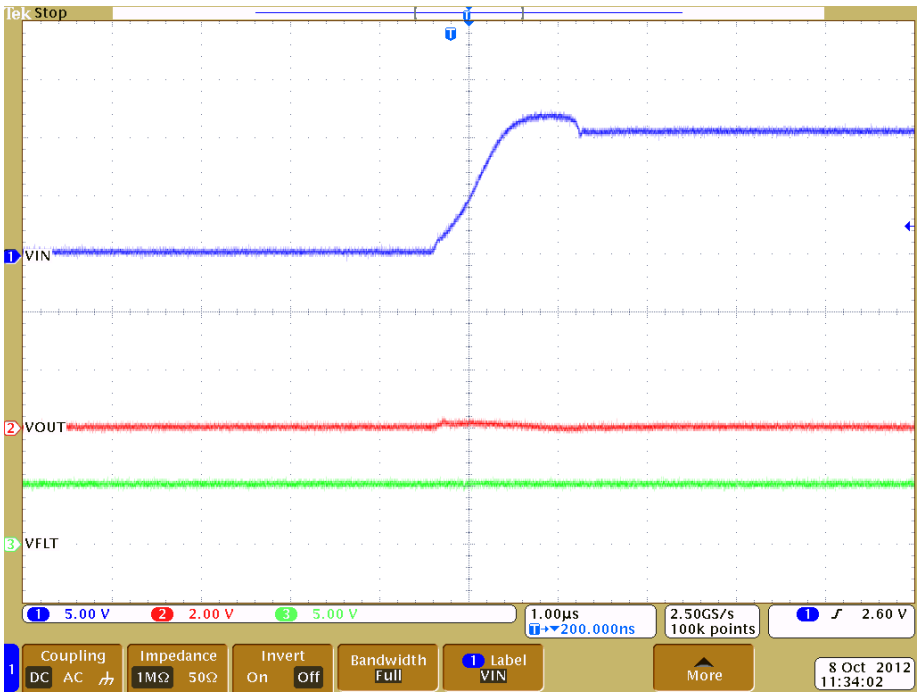
1. Output load is 5 Ω.

Figure 15. Startup to overvoltage



1. Output load is 5 Ω.

Figure 16. Startup to overvoltage (detail)

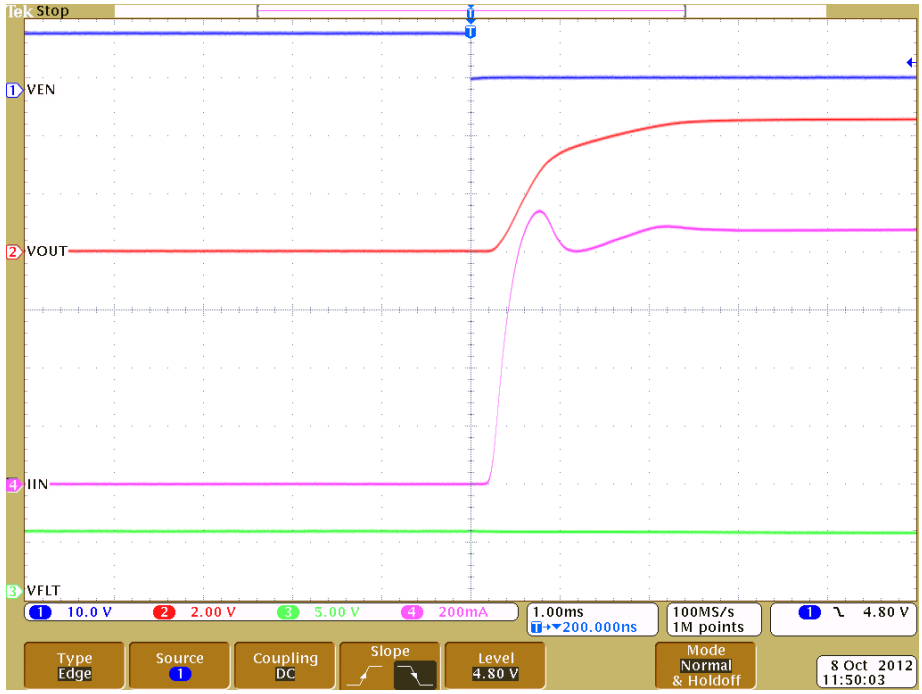


1. Output load is 5 Ω. Almost no glitch on the output.

Figure 17. Soft-start performance for 10 µF capacitive load

1. Output load is 10 µF in parallel with 5 Ω.

Figure 18. Soft-start performance for 100 µF capacitive load



1. Output load is 100 µF in parallel with 5 Ω.

Figure 19. I_{CC} vs. temperature at V_{IN} = 5 V

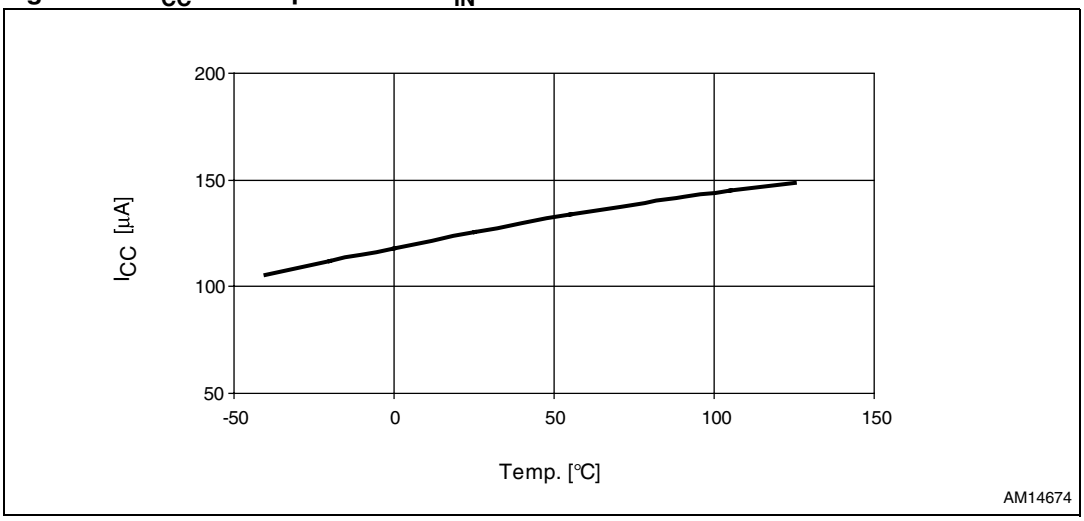


Figure 20. I_{CC} vs. V_{IN}

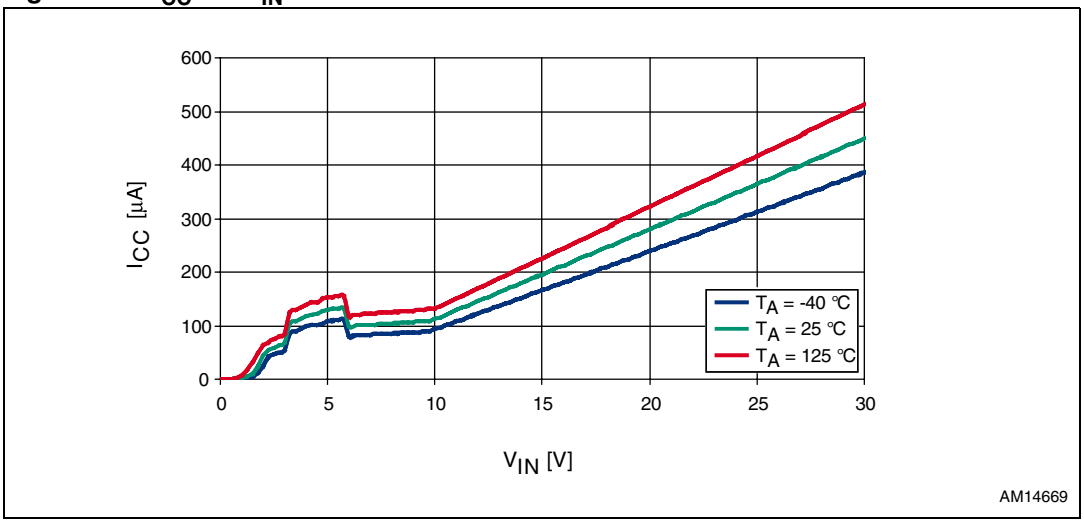


Figure 21. I_{CC} vs. V_{IN} (detail)

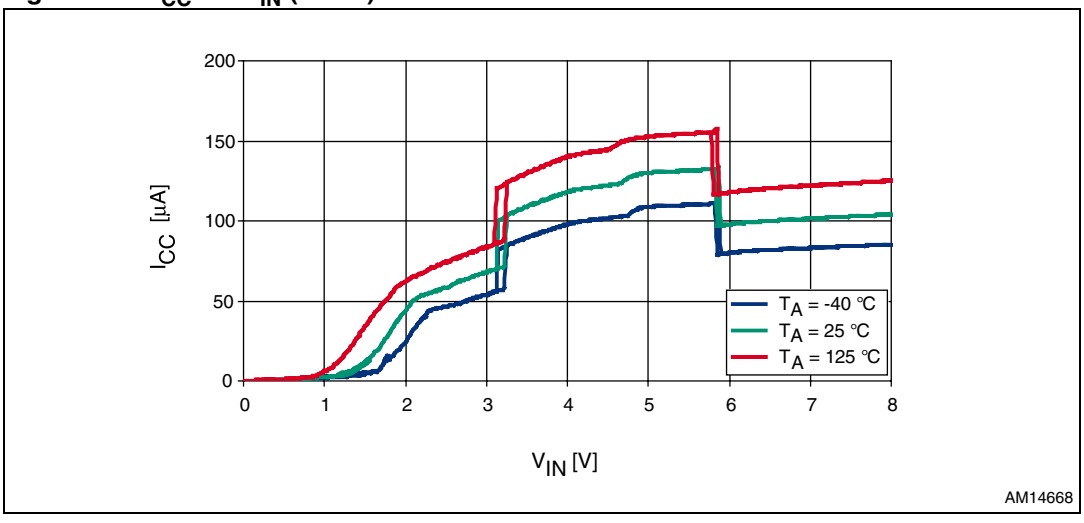


Figure 22. $I_{CC(STDBY)}$ vs. temperature at V_{IN} = 5 V

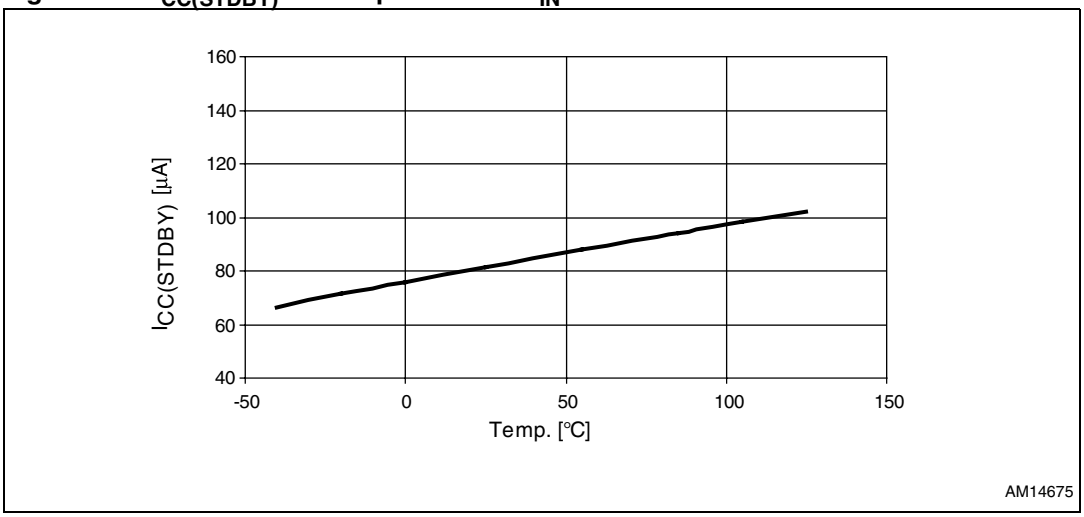


Figure 23. $I_{CC(STDBY)}$ vs. V_{IN}

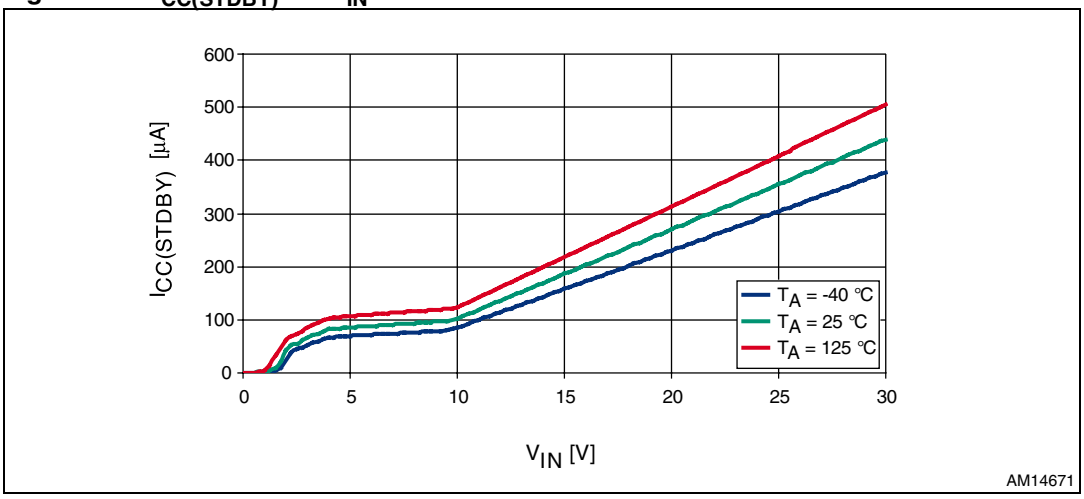


Figure 24. $I_{CC(STDBY)}$ vs. V_{IN} (detail)

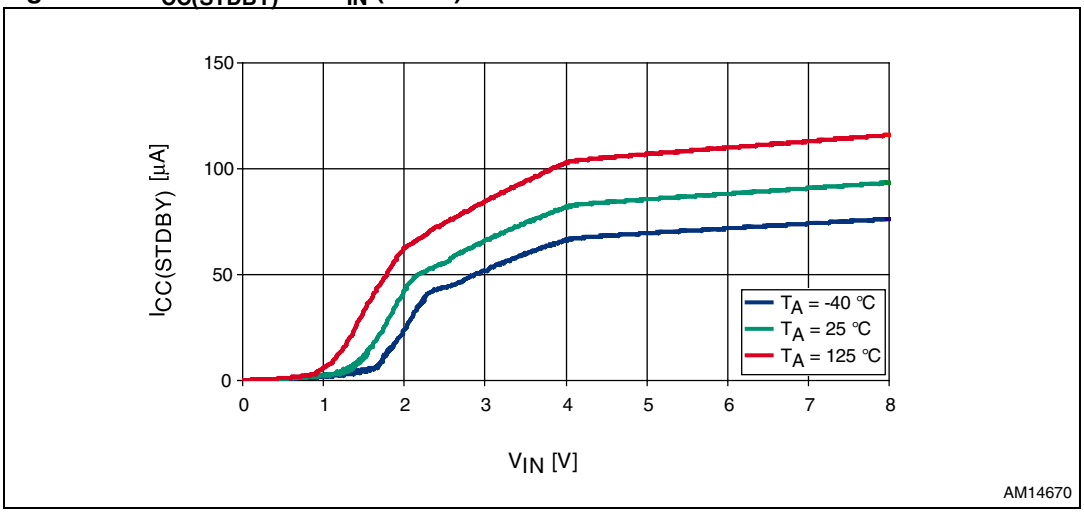


Figure 25. V_{OVLO} vs. temperature

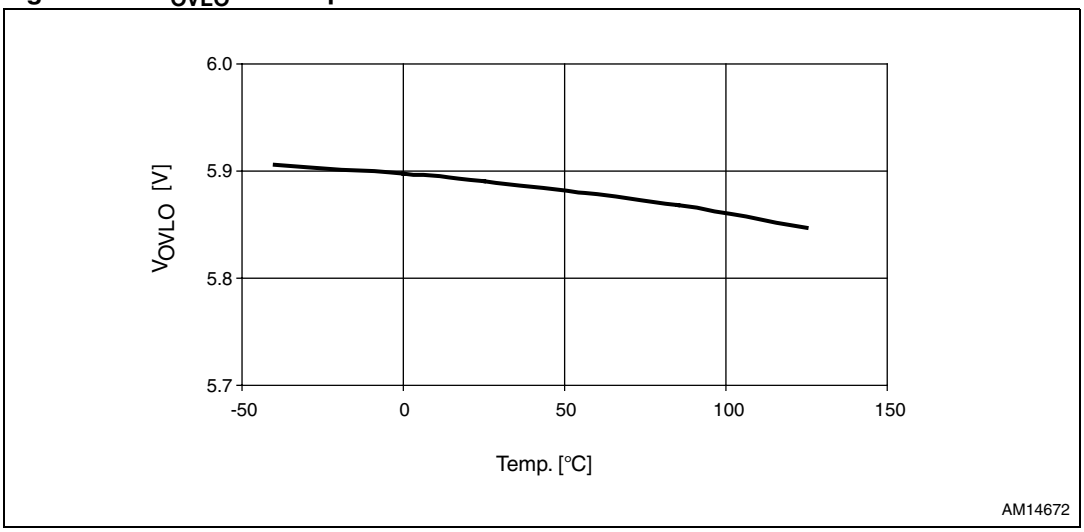


Figure 26. V_{UVLO} vs. temperature

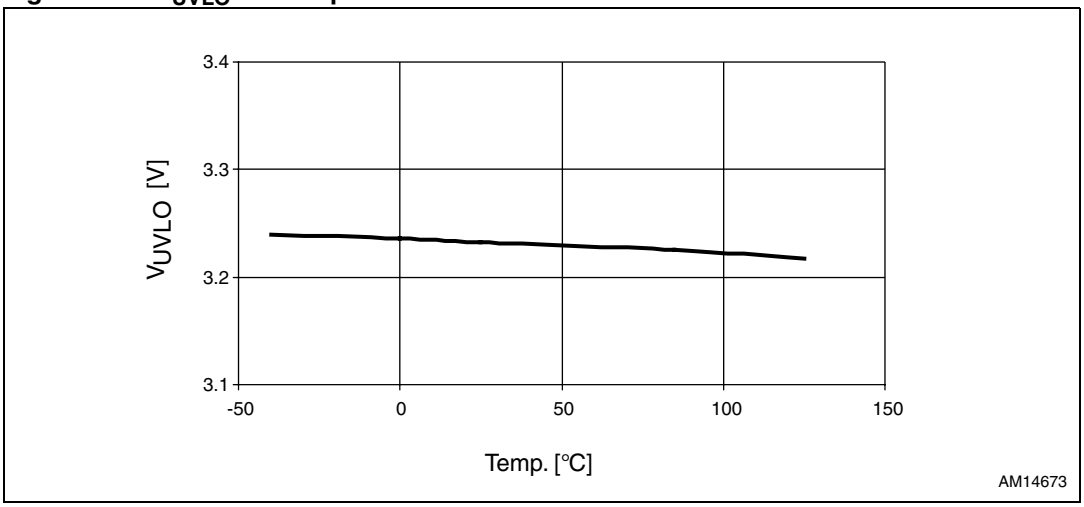


Figure 27. $V_{OL(\overline{FLT})}$ vs. temperature at $I_{SINK(\overline{FLT})}$ = 5 mA, V_{IN} = 5 V

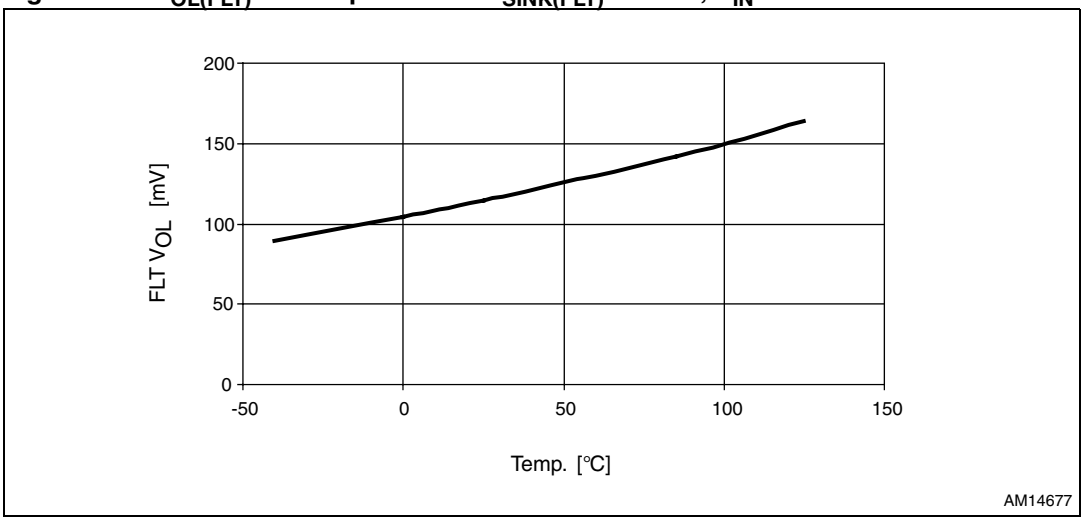


Figure 28. $R_{DS(on)}$ vs. temperature at 5 V, 1 A

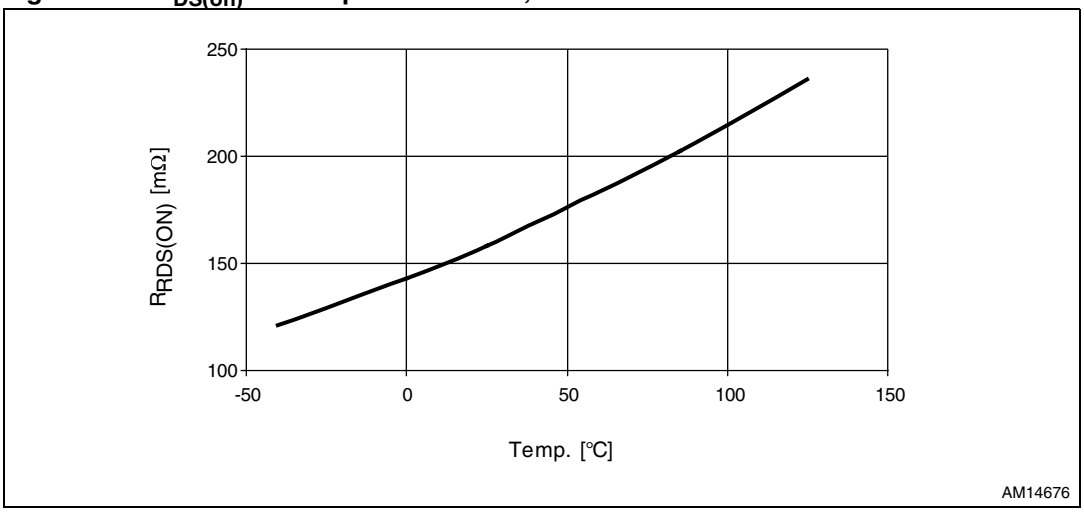


Figure 29. $V_{IL(\overline{EN})}$ vs. temperature

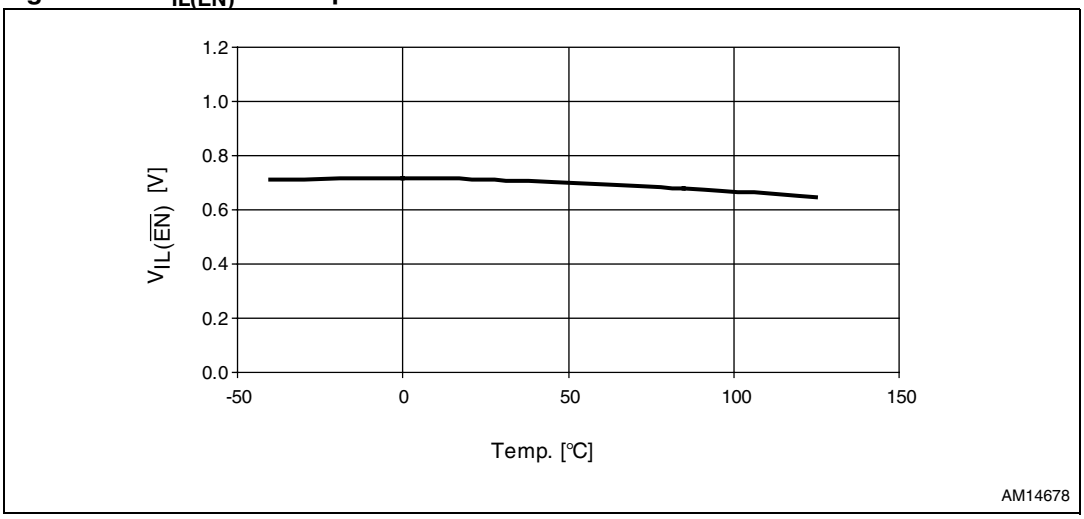


Figure 30. $V_{IH(\overline{EN})}$ vs. temperature

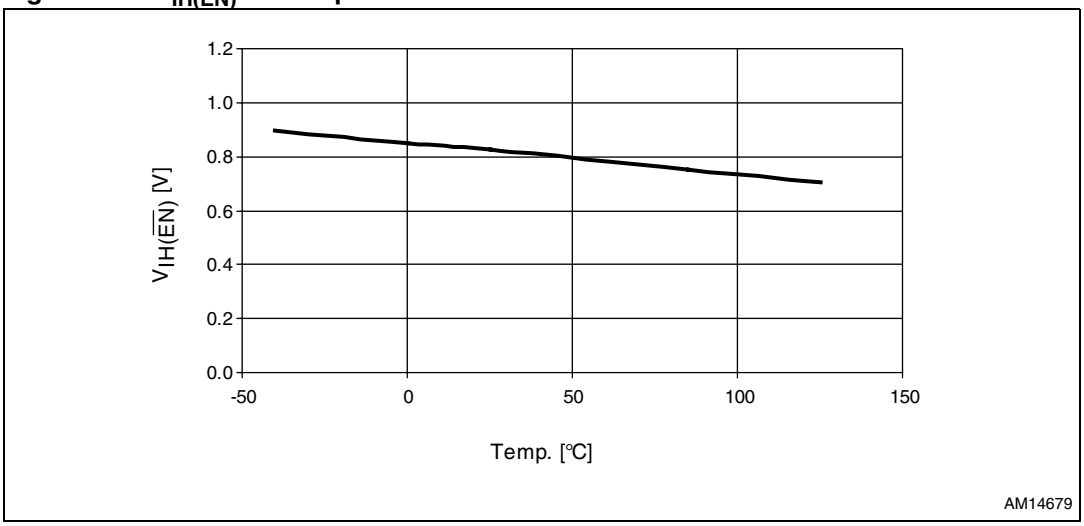


Figure 31. $I_{(\overline{EN})}$ vs. V_{IN} at $V_{(\overline{EN})}$ = 5 V

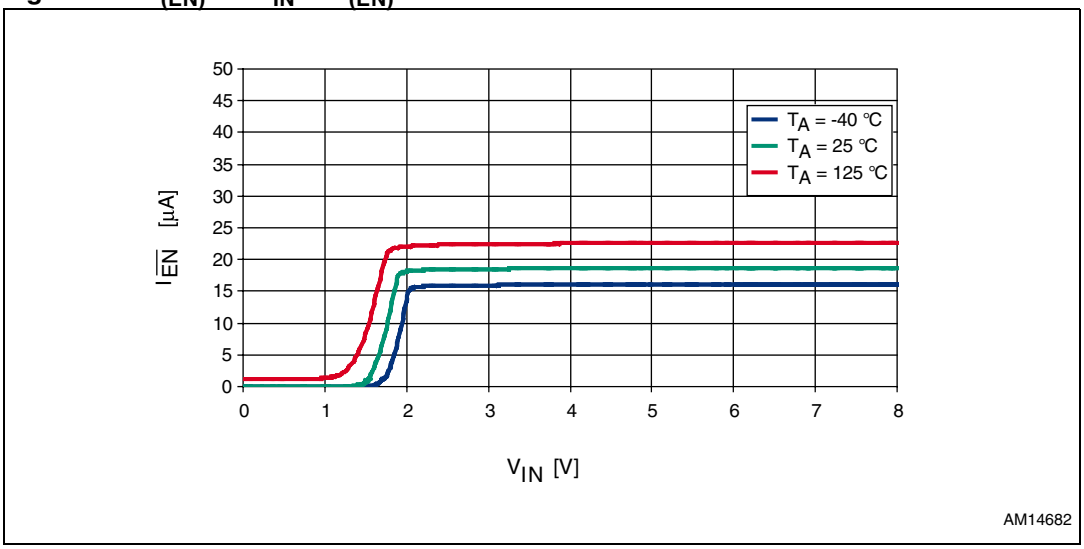


Figure 32. $R_{PD(\overline{EN})}$ vs. temperature at $V_{(\overline{EN})}$ = V_{IN} = 5 V

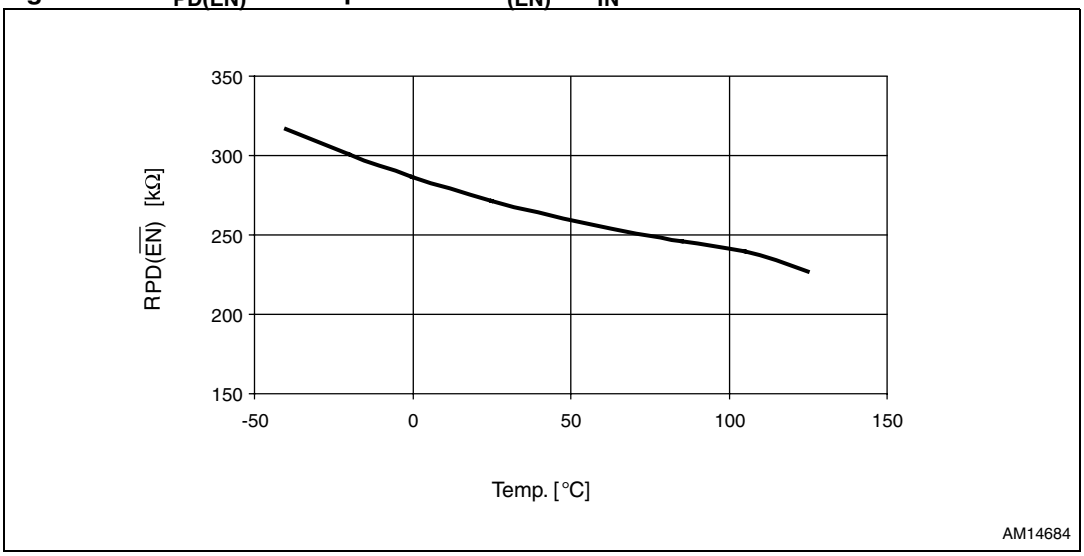


Figure 33. t_{on} vs. temperature

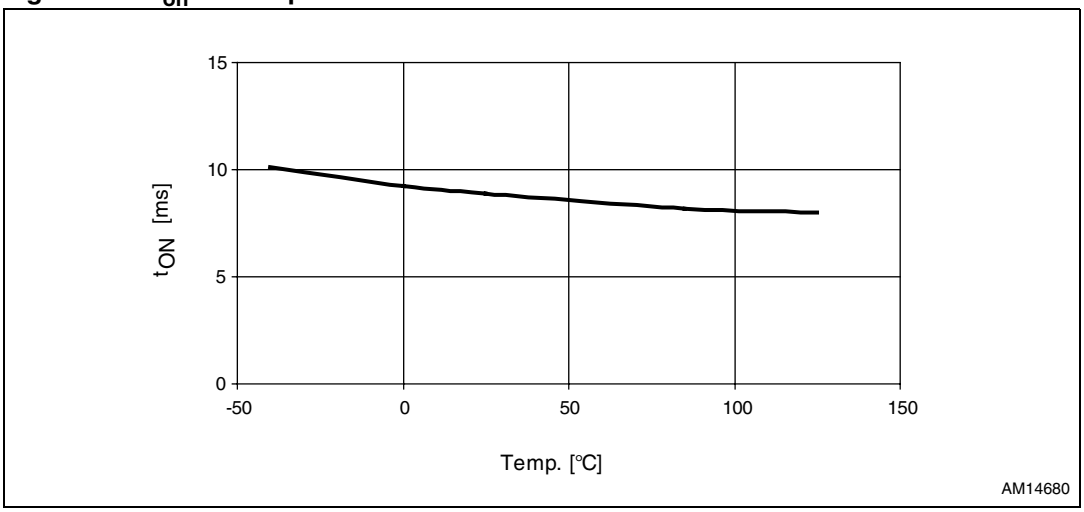
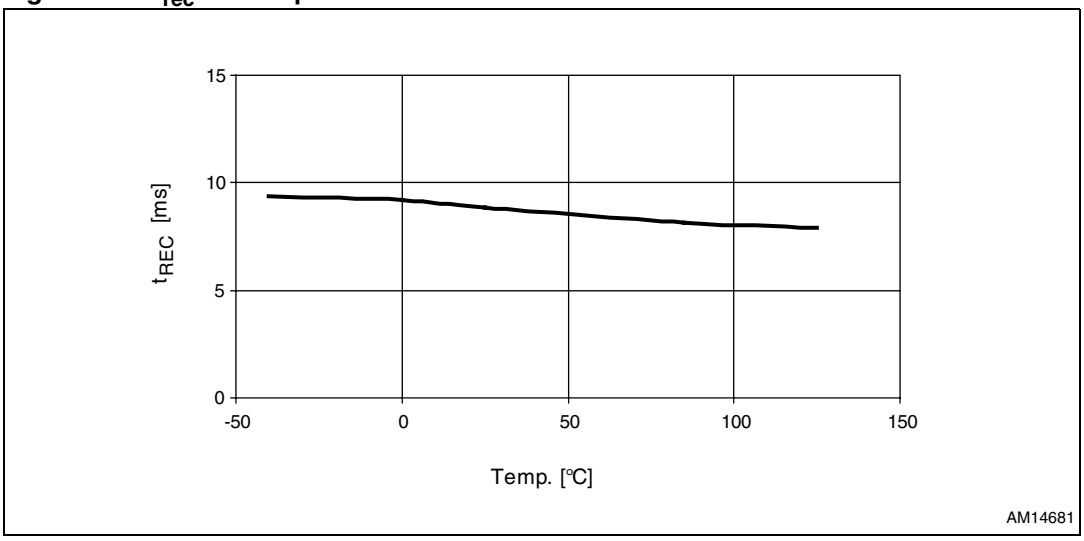


Figure 34. t_{rec} vs. temperature



6 Maximum rating

Stressing the device above the rating listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Section 3 on page 10* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant documentation.

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{IN} off)		-55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
T_J	Operating junction temperature range (internally limited to T_{off})		-40 to 150	°C
V_{IN}	IN pin input voltage		-0.3 to 30	V
V_{OUT}	OUT pin input/output voltage		-0.3 to 12	V
V_{IO}	Input/output voltage (other pins)		-0.3 to 7	V
I_{LOAD}	Load current (IN to OUT)	$T_A \leq 50$ °C	2000	mA
		$T_A = 85$ °C	1500	mA
$I_{REVERSE}$	Reverse diode current (OUT to IN)		500	mA
$I_{SINK(\overline{FLT})}$	$\overline{FLT}$ pin sink current		15	mA
V_{ESD}	ESD withstand voltage (IEC 61000-4-2, IN pin only)(2)		±15 (air), ±8 (contact)	kV
	Human body model (HBM), model = 2(3)		2000	V
	Machine model (MM), model = B(4)		200	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. System-level value (see typical application circuit, C1 ≥ 1 µF low ESR ceramic capacitor).
3. Human body model, 100 pF discharged through a 1.5 kΩ resistor according to the JESD22/A114 specification.
4. Machine model, 200 pF discharged through all pins according to the JESD22/A115 specification.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance (junction-to-ambient)	59(1)	°C/W
R_{thJC}	Thermal resistance (junction-to-case)	5.9	°C/W

1. The package was mounted on a 4-layer JEDEC test board with 2 thermal vias connecting from the thermal land to the first buried plane. The 4-layer PCB (2S2P) was constructed based on JESD 51-7 specifications and vias based on JESD 51-5.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in *Table 5* are derived from tests performed under the measurement conditions summarized in *Table 4*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Value	Unit
Input voltage (V_{IN})	5	V
Ambient operating temperature (T_A)	-40 to 85	°C
Junction operating temperature (T_J)	-40 to 125	°C
Logical input rise and fall times	5	ns

Table 5. DC and AC characteristics

Symbol	Description	Test condition(1)	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage range		V_{UVLO}		28	V
V_{UVLO}	Input undervoltage lockout threshold (V_{IN} rising)	Option T Option U Option V	2.5 2.8 3.1	2.7 3.0 3.25	2.9 3.2 3.4	V
$V_{HYS(UVLO)}$	Undervoltage lockout hysteresis(2)			100		mV
V_{OVLO}	Overvoltage lockout threshold	V_{IN} raises OVLO threshold, option A	5.25	5.375	5.50	V
		V_{IN} raises OVLO threshold, option B	5.30	5.50	5.70	
		V_{IN} raises OVLO threshold, option C	5.71	5.90	6.10	
		V_{IN} raises OVLO threshold, option D	5.70	6.02	6.40	
		V_{IN} raises OVLO threshold, option E	6.20	6.40	6.60	
		V_{IN} raises OVLO threshold, option F	6.60	6.80	7.00	
		V_{IN} raises OVLO threshold, option G	7.00	7.20	7.40	
$V_{HYS(OVLO)}$	Input overvoltage hysteresis		30	60	90	mV
$R_{DS(on)}$	IN to OUT resistance	$V_{(\overline{EN})}$ = 0 V, V_{IN} = 5 V, I_{LOAD} = 0.5 A		165	280	mΩ
I_{CC}	Operating current	$V_{(\overline{EN})}$= 0 V, I_{LOAD} = 0 A		140	210	µA
$I_{CC(STDBY)}$	Standby current	$V_{(\overline{EN})}$ = 5 V, I_{LOAD} = 0 A		80	120	
$V_{OL(\overline{FLT})}$	$\overline{FLT}$ output low level voltage	V_{IN} > V_{OVLO}, $I_{SINK(\overline{FLT})}$ = 5 mA		350	800	mV
$I_{L(\overline{FLT})}$	$\overline{FLT}$ output leakage current	$V_{\overline{FLT}}$ = 5 V		0.1	2	µA
$V_{IL(\overline{EN})}$	$\overline{EN}$ low level input voltage				0.4	V

Table 5. DC and AC characteristics (continued)

Symbol	Description	Test condition(1)	Min.	Typ.	Max.	Unit
$V_{IH(\overline{EN})}$	$\overline{EN}$ high level input voltage		1.2			V
$R_{PD(\overline{EN})}$	$\overline{EN}$ internal pull-down resistor(3)	V_{IN} > 2.5 V, $V_{(\overline{EN})}$ = 5 V	100	250	400	kΩ
Timing parameters						
t_{on}	Startup delay(4)	Time measured from V_{IN} > V_{UVLO} to V_{OUT} = 0.3 V (no load on the output).		8		ms
t_{off}(5)	Output turn-off time	Time measured from V_{IN} > V_{OVLO} to V_{OUT} ≤ 0.3 V. V_{IN} increasing from 5.0 V to 8.0 V at 3.0 V/µs, R_{LOAD} = 5 Ω, C_{LOAD} = 0.			1	µs
t_{dis}(5)	Disable time	Time measured from $V_{(\overline{EN})}$ ≥ 1.2 V to V_{OUT} < 0.3 V, R_{LOAD} = 5 Ω, C_{LOAD} = 0.		1	5	
t_{rec}	Recovery delay from UVLO, OVLO, or thermal shutdown(4)	Time measured to V_{OUT} = 0.3 V (no load on the output)		8		ms
Thermal shutdown						
T_{off}	Thermal shutdown threshold temperature			140	150	°C
$T_{HYS(off)}$	Thermal shutdown hysteresis			20		°C

1. Test conditions described in *Table 4* (except where noted).
2. Hysteresis of 60 mV typ. available upon request.
3. Version without pull-down resistor or with permanently connected pull-down resistor available upon request.
4. Delays of 16, 32, and 64 ms available upon request.
5. Guaranteed by design. Not tested in production.

8 Application information

8.1 Calculating the power dissipation

The worst case power dissipation of the STBP112 internal power MOSFET can be calculated using the following formula:

Equation 1

$P_D = I_{LOAD}^2 \times R_{DS(on)(max)}$,

where I_{LOAD} is the load current and $R_{DS(on)(max)}$ is the maximum value of MOSFET resistance.

Example 1

V_{IN} = 5 V, R_{LOAD} = 5 Ω, $R_{DS(on)(max)}$ = 280 mΩ

$I_{LOAD} = V_{IN} / (R_{DS(on)(max)} + R_{LOAD}) = 5 / (5 + 0.280) = 0.95$ A

$P_D = 0.95^2 \times 0.28 = 0.25$ W

The power dissipation of the reverse diode in powering accessories mode can be estimated as $P_D = (V_{OUT} - V_{IN}) \times I_{REVERSE} \approx 0.7 \times I_{REVERSE}$.

8.2 Calculating the junction temperature

The maximum junction temperature for given power dissipation, ambient temperature, and thermal resistance junction-to-ambient can be calculated as:

Equation 2

$T_J = T_A + 1.15 \times P_D \times R_{thJA} = T_A + 1.15 \times I_{LOAD}^2 \times R_{DS(on)(max)}) \times R_{thJA}$,

where T_J is junction temperature, T_A is given ambient temperature, 1.15 is a derating factor, and R_{thJA} is a junction-to-ambient thermal resistance, depending on PCB design. The junction temperature may not exceed 125 °C (see *Table 4*) to stay within the specified range.

Maximum allowed MOSFET current for ambient temperature T_A = 85 °C and various R_{thJA} values are listed in *Figure 9 on page 14*.

Example 2

For conditions listed in the previous example, with a well designed PCB (ensuring R_{thJA} = 59 °C/W) and T_A = 85 °C, the maximum junction temperature is:

Equation 3

$T_J = 85 + 1.15 \times 0.25 \times 59 = 102$ °C,

which is a safe value (below 125 °C).

8.3 PCB layout recommendations

- Input capacitor C1 should be located as close as possible to the STBP112 device. It should be a low-ESR ceramic capacitor. Also the protective resistors R_{FLT} and R_{EN} (if used) should be located close to the STBP112 (see *Figure 4 on page 9*).
- For good thermal performance, it is preferred to couple the STBP112 exposed thermal pads with the PCB ground plane. In most designs, this requires thermal vias between the copper pads on the PCB and the ground plane.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 35. Package outline for TDFN 8-lead (2 x 2 x 0.75 mm)

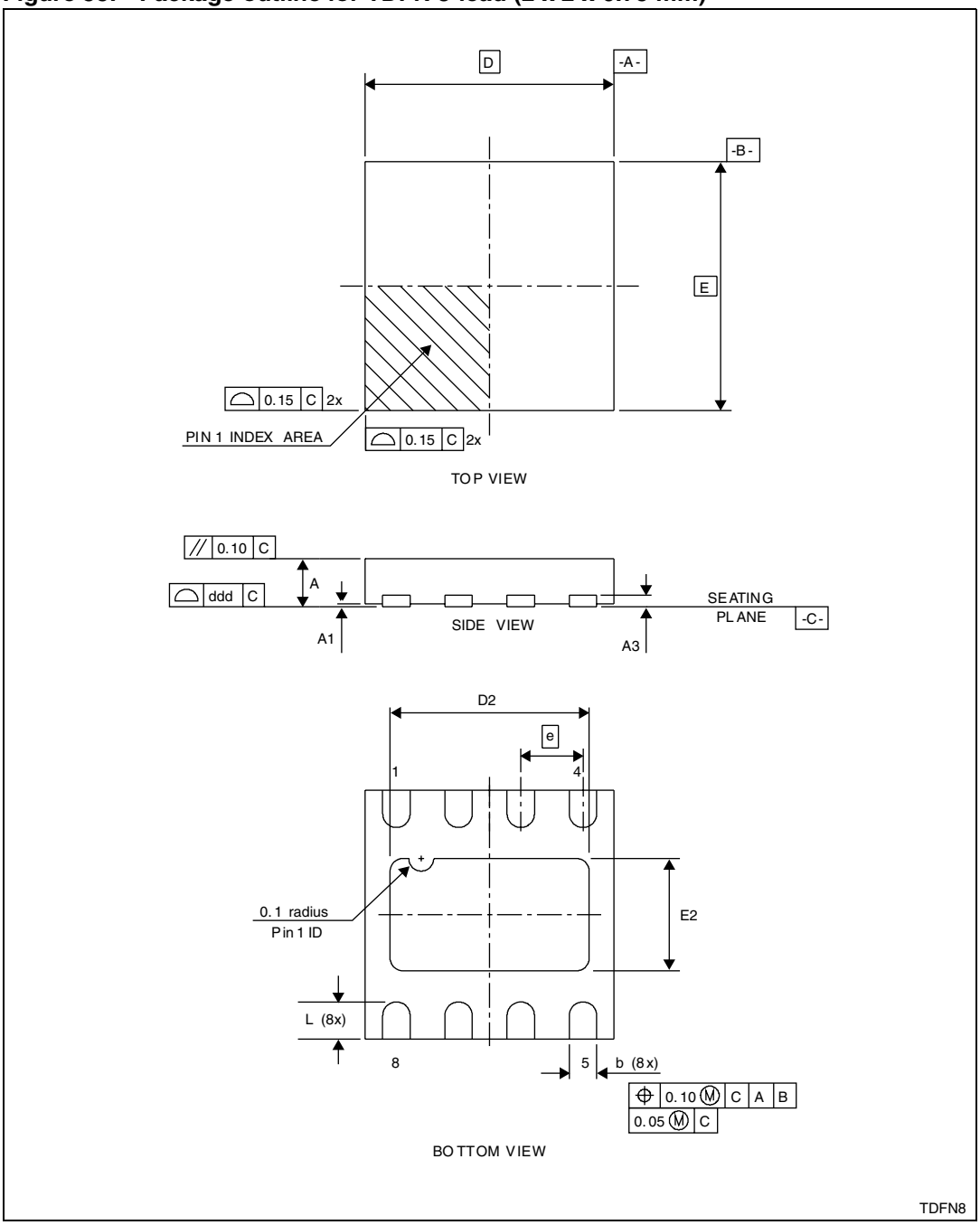


Table 6. Package mechanical dimensions for TDFN 8-lead (2 x 2 x 0.75 mm)(1)

Symbol	Dimensions					
	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.75	0.70	0.80	0.030	0.028	0.031
A1	0.02	0.00	0.05	0.001	0.000	0.002
A3 REF	0.20	—	—	0.008	—	—
b	0.25	0.20	0.30	0.010	0.008	0.012
D BSC	2.00	—	—	0.079	—	—
D2	1.60	1.45	1.70	0.063	0.057	1.067
E BSC	2.00	—	—	0.079	—	—
E2	0.90	0.75	1.00	0.035	0.030	0.039
e	0.50	—	—	0.020	—	—
L	0.30	0.25	0.35	0.012	0.010	0.014
ddd(2)	—	—	0.08	—	—	0.003
N(3)	8			8		

1. Controlling dimension: millimeters.
2. Lead coplanarity should not exceed 0.08 mm.
3. N is the total number of terminals.

10 Tape and reel information

Figure 36. Tape and reel

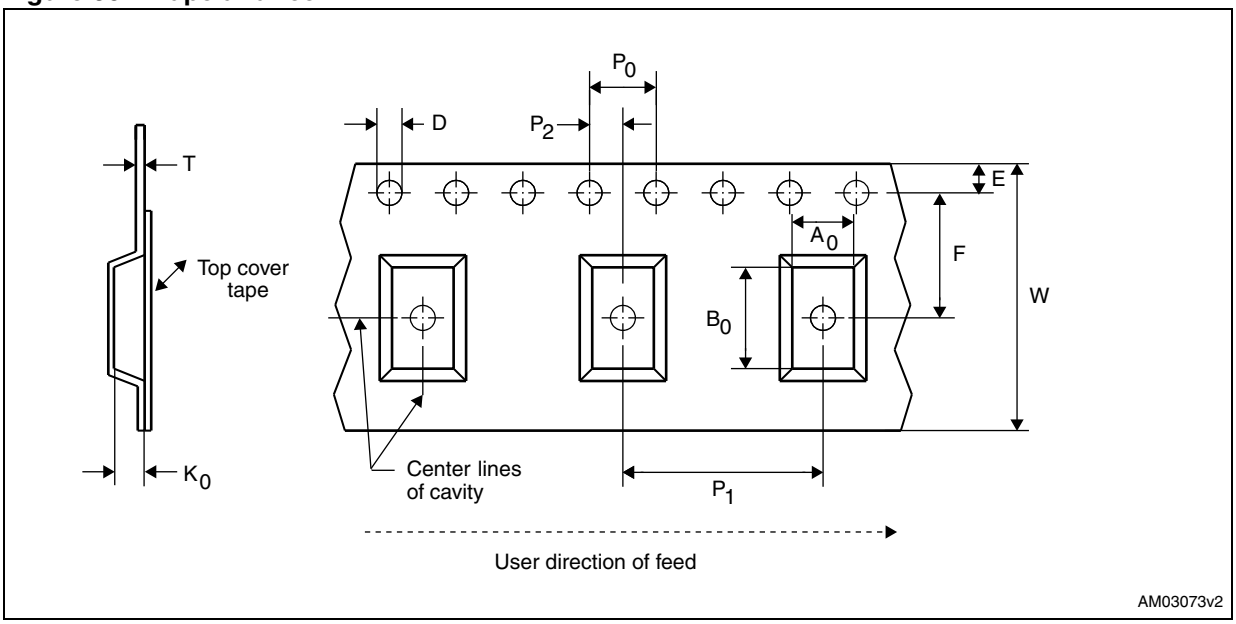


Table 7. Carrier tape dimensions

Tape size	W	D	E	P0	P2	F
8	8.00 +0.30 / -0.10	1.50 +0.10 / -0.0	1.75 ± 0.1	4.00 ± 0.10	2.00 ± 0.10	3.50 ± 0.05

Table 8. Further tape and reel information

Package code	W	A0	B0	K0	P1	T	Bulk qty.	Reel diameter
2 x 2 mm TDFN 8-lead	8	2.30 ± 0.05	2.30 ± 0.05	1.00 ± 0.05	4.00 ± 0.10	0.250 ± 0.05	3000	7

Figure 37. Reel dimensions

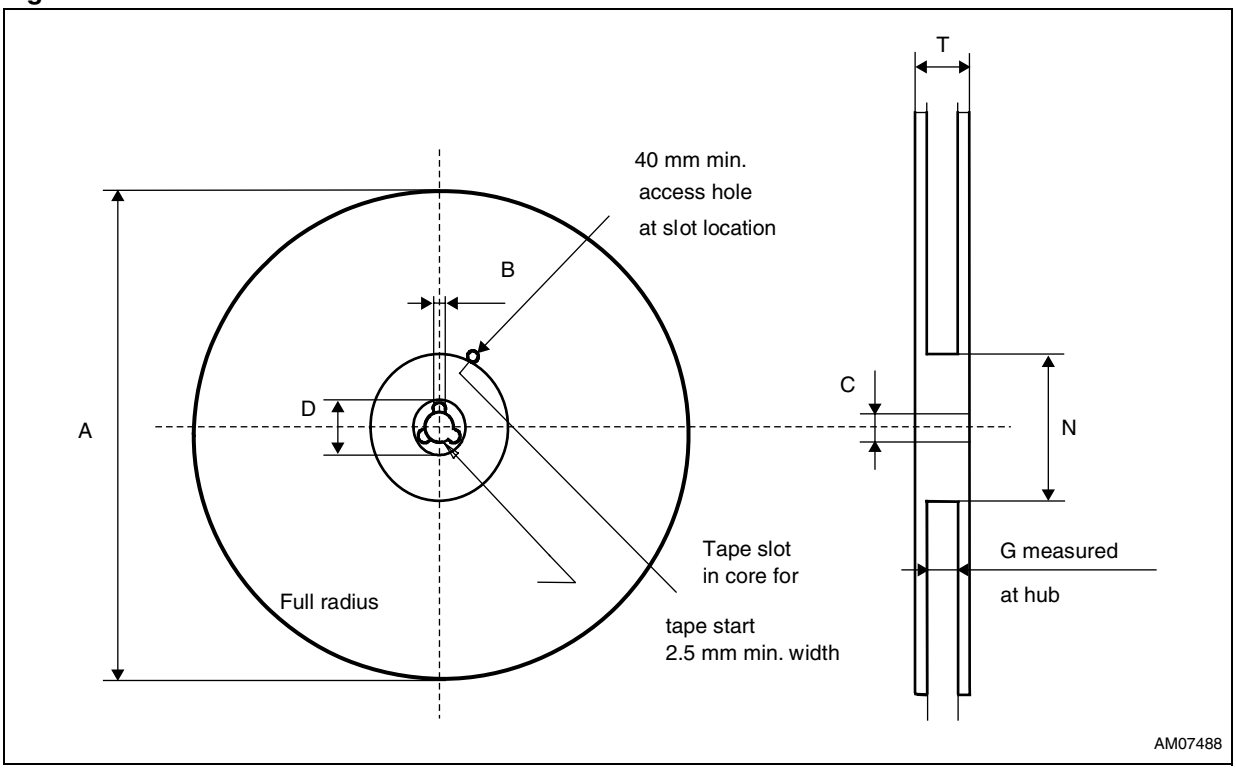


Table 9. Reel dimensions

Tape size	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inch)	1.5	13 ± 0.2	20.2	60	8.4 +2 / -0	14.4

Figure 38. Tape trailer/leader

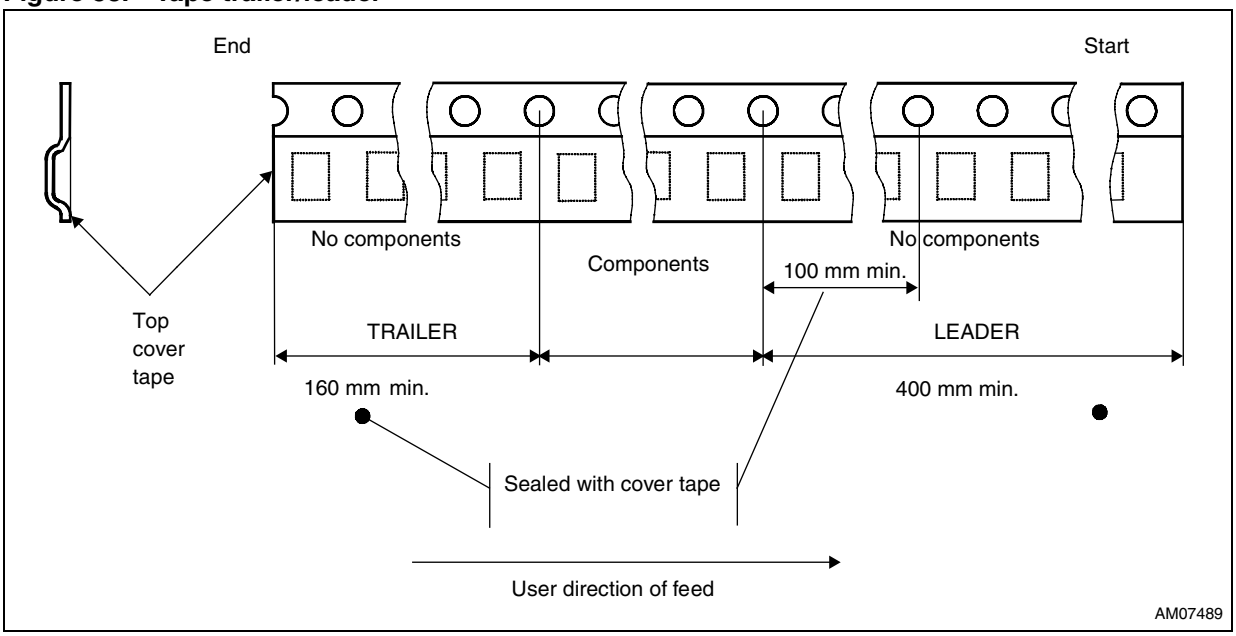
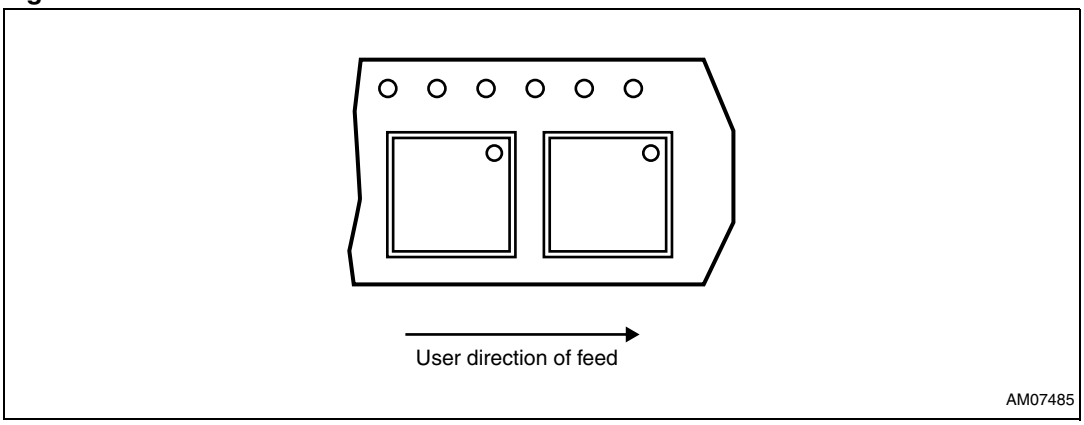


Figure 39. Pin 1 orientation



Note: Drawings are not to scale.

All dimensions are in mm, unless otherwise noted.

11 Part numbering

Table 10. Ordering information scheme

STBP112	A	T	DJ	6	F

Device type

STBP112

Overvoltage threshold

A = 5.375 V

B = 5.50 V

C = 5.90 V

D = 6.02 V

E = 6.40 V

F = 6.80 V

G = 7.20 V

Undervoltage threshold

T = 2.70 V

U = 3.00 V

V = 3.25 V

Package

DJ = TDFN8 2 x 2 x 0.75 mm

Temperature range

6 = -40 to +85 °C

Shipping method

F = ECOPACK® package, tape and reel

Note: Please check device version availability on www.st.com. Please contact local ST sales office for new device version request.

12 Package marking information

Table 11. Marking description

Part number[1], [2]	Overvoltage threshold (V)	Undervoltage threshold (V)	Topside marking
STBP112ATxxxx	5.375	2.70	12A
STBP112BTxxxx	5.50	2.70	12B
STBP112CTxxxx	5.90	2.70	12C
STBP112DTxxxx	6.02	2.70	12D
STBP112ETxxxx	6.40	2.70	12E
STBP112FTxxxx	6.80	2.70	12F
STBP112GTxxxx	7.20	2.70	12H
STBP112AUxxxx	5.375	3.00	12K
STBP112BUxxxx	5.50	3.00	12L
STBP112CUxxxx	5.90	3.00	12M
STBP112DUxxxx	6.02	3.00	12N
STBP112EUxxxx	6.40	3.00	12P
STBP112FUxxxx	6.80	3.00	12Q
STBP112GUxxxx	7.20	3.00	12R
STBP112AVxxxx	5.375	3.25	12T
STBP112BVxxxx	5.50	3.25	12U
STBP112CVxxxx	5.90	3.25	12V
STBP112DVxxxx	6.02	3.25	12W
STBP112EVxxxx	6.40	3.25	12X
STBP112FVxxxx	6.80	3.25	12Y
STBP112GVxxxx	7.20	3.25	12Z

1. Please check device version availability on www.st.com. Please contact local ST sales office for new device version request.
2. Currently available part numbers are marked bold in *Table 11*. For other options, or for more information on any aspect of this device, please contact the nearest ST sales office.

13 Revision history

Table 12. Document revision history

Date	Revision	Changes
22-Jun-2012	1	Initial release.
17-Oct-2012	2	Updated *Features* (modified $R_{DS(on)}$). Added *Section : Typical operating characteristics (STBP112CV)* (*Figure 11* to *Figure 34*). Updated *Table 5* (modified typ. $R_{DS(on)}$). Minor corrections throughout document.
07-Dec-2012	3	Updated *Table 11* (STBP112CVxxxx par number marked bold, reformatted Note *1.*, added Note *2.*)

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