AN_65XX_016 JUNE 2011

EMC/EMI Design Guidelines for 71M65XX ICs

Designing a meter for optimum electromagnetic compatibility can be a challenging issue for any design engineer. EMC/EMI testing for metering products involve the following:

- Conduced and Radiated Emissions
- RF Immunity
- Electrostatic Discharge (ESD)
- Electrical Fast transient (EFT)

Successfully passing these tests depends on many factors, such as:

- Schematic design
- PCB design
- Component selection
- Component placement on the PCB
- Input connections of the current sensing elements
- Meter firmware

The methods presented in this document are incorporated into the TERIDIAN Demo Boards enhancing EMI compatibility without affecting accuracy performance of the meter.

Following the recommendations outlined in this document in the initial phase of schematic and PCB design helps generating EMI/EMC compliant designs up front, avoiding potential rework of PCBs.

This document describes the details for EMI/EMC compliance based on 71M65XX Demonstration Boards.

Note: Reference designators are given in a generalized form and do not necessarily relate to the reference designators used on actual TERIDIAN Demo Boards.

Schematic Design Precautions

General Precautions

Unnecessary components such as test points, test headers, and unused interfaces should be removed.

Current Inputs:

71M65XX devices accept three commonly used current sensor inputs such as

a. Current Transformers

b. Current Shunts

c. Rogowski Coils

Displayed and recorded energy under EMI conditions depends on the design of the current and voltage inputs. Improper design may lead to erroneous display of energy, especially in cases where loads are disconnected, as required by some test standards.

The input signal conditioning circuits depend on the current sensors used and are described in detail in the following sections.

Current Transformers

Figure 1shows the suggested input signal conditioning circuit.

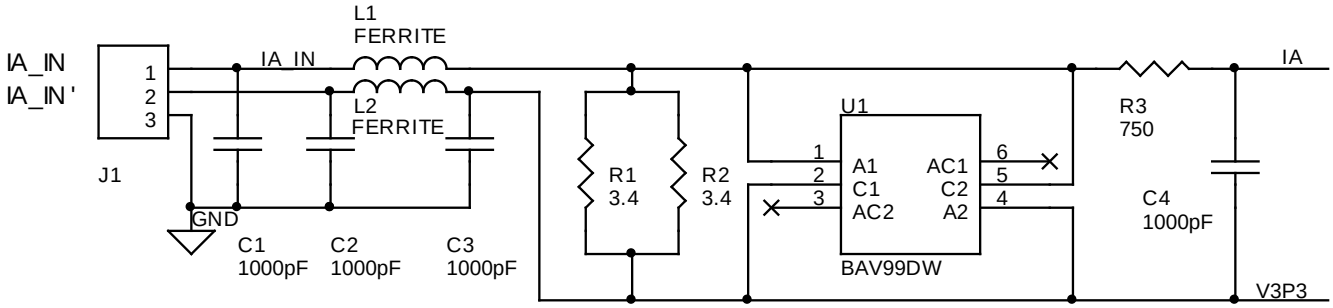

Figure 1: CT Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. The combination of R3 and C4 provides a low pass filter for differential signals with cutoff frequency of around 212kHz.
3. Connector J1 has a third pin provision (some Demo Boards use only two of those pins). Connect pin3 of J1 to the shield of the CT cable if needed.
4. The combination of C2, L2, and C3 eliminates high-frequency noise spikes on the analog reference, V3P3.

Current Shunt

Figure 2 shows the suggested input signal conditioning circuit for Current Shunt inputs.

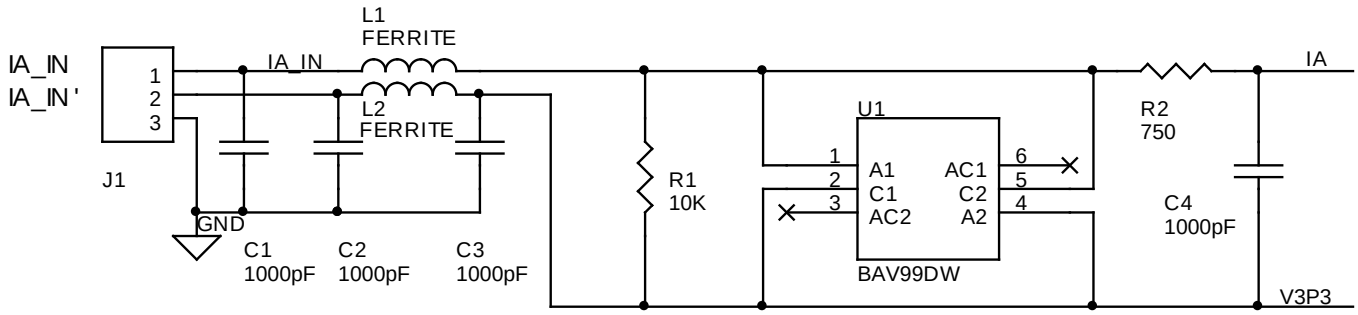

Figure 2: Current Shunt Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. Generally, the Current Shunt interface to 71M651X and 71M652X Demo Boards involves a four-wire connection. Two of the wires connect to J1 as shunt inputs for the current sensing circuit. The other two wires tied to one side of the shunt provide additional neutral connections.
2. L1 and L2 are ferrite beads that provide 600Ω impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
3. R3 and C1 provide a low pass filter for differential signals. Depending on the length of the cable harness used to hook up the current shunt, the value of the capacitor C1 may vary.
4. Connector J3 has a third pin provision to accommodate for the connection to the shield of the Shunt cable to connect to the digital ground to prevent high frequency noise entering through the Shunt metal plate and the sensor cables.
5. C2, L2 and C3 form a Pi-filter that eliminates high-frequency noise spikes on the analog reference, V3P3.
6. R1 acts as a damping resistor in parallel with the current shunt to minimize EMI noise.

Note: Some EMI suppression components are not available on the 4-Layer 71M6511 Demo Board.

Rogowski Coil

Figure 3 shows the suggested input signal conditioning circuit for Rogowski coils.

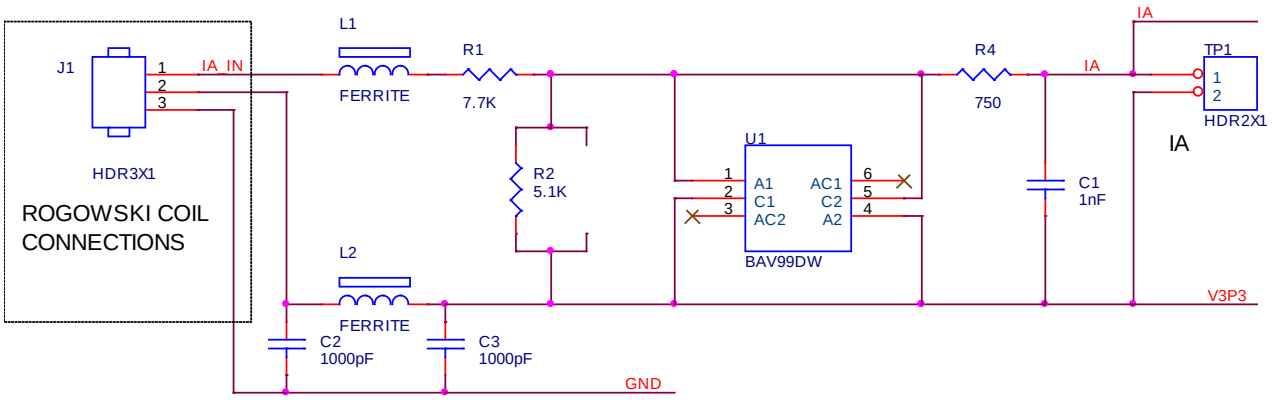

Figure 3: Rogowski Coil Input Signal Processing Circuit

Key precautions recommended for passing EMC/EMI testing for the input signal conditioning circuit:

1. L1 and L2 are Ferrite beads that provide 600-Ohm impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. R4 and C1 provide a low pass filter for differential signals with cutoff frequency of around 212kHz.
3. Connector J1 has a third pin provision to accommodate the connection of the cable shield if there is a necessity to use shielded cable. If used, the shield needs to be connected to digital ground.
4. C2, L2 and C3 form a Pi-filter that eliminates high-frequency noise spikes on the analog reference, V3P3.

Sensor Wiring

The following precautions apply to sensor wiring:

1. Sensor wires may be shielded. This applies especially to sensor wiring used in the Shunt Resistor configuration. Inside the shield, the wires should be twisted (STP).
2. If used, shields for sensor wiring should be terminated to DGND. Some Demo Boards have provisions for connecting the shield wire.
3. If shielding is not desired, unshielded twisted wire (UTP) pairs may be used.
4. Sensor wires should be kept as short as possible.
5. Ferrites may be used on sensor wiring to prevent common-mode noise.

Voltage Inputs (CT Mode)

Figure 4 shows a typical voltage input circuit. Key precautions are:

1. L1 is a Ferrite bead that provides 600-Ohm impedance for common mode signals above 100MHz (e.g. TDK MMZ2012S601A).
2. R1+R2+R3+R4 and C2 provide a low pass filter for differential signals.
3. The highest value of the resistor ladder (in this case R1) should be placed directly at the voltage input. This will result in the highest voltage drop. Consequently, the voltages at R2, R3, etc. will be in a safer range, and precautions for leakage or arching need only be taken for R1.
4. C1 filters noise on the Neutral connection. C1 appears as C14 on many Demo Boards.

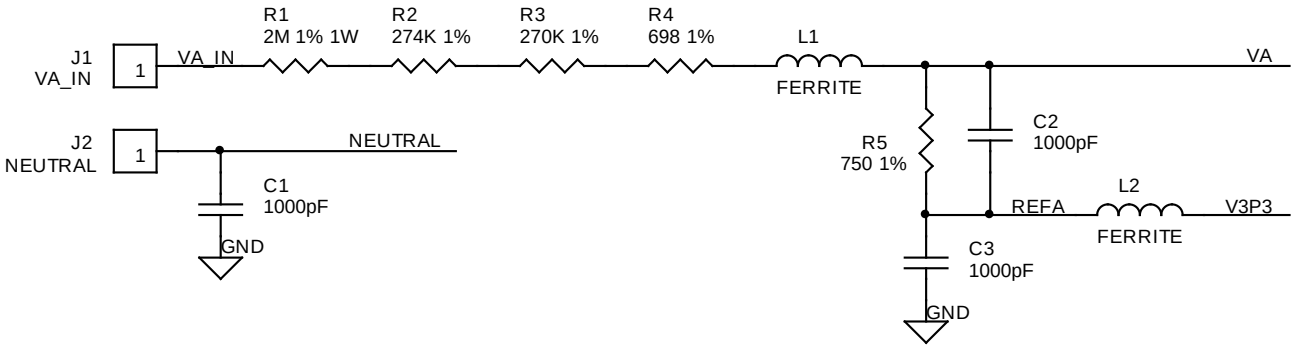

Figure 4: Voltage Input Circuit for CT

Voltage Inputs (Current Shunt Mode)

Figure 5 shows the recommended voltage input circuit when using a current shunt.

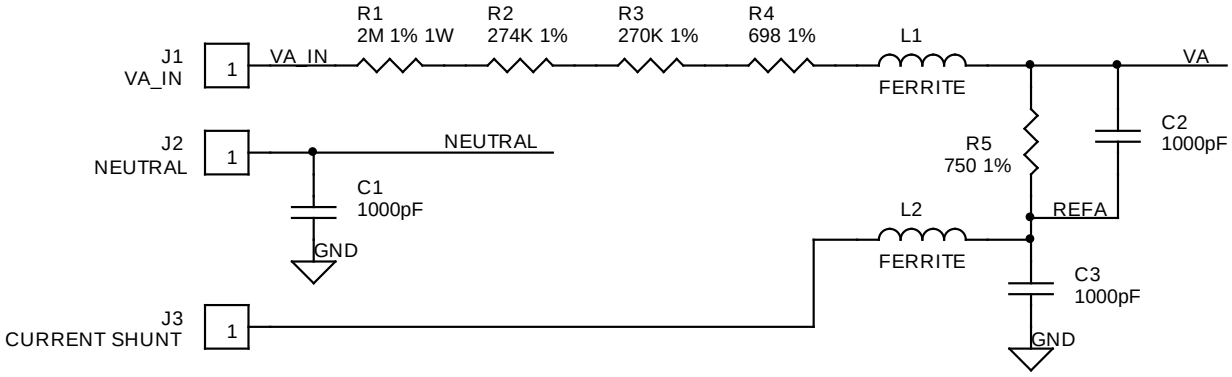

Figure 5: Voltage Input Circuit for Current Shunt Mode

Attach one of the two wires coming from the Neutral side of the current shunt to J3. This J3 connection is typically JP17 pin 2 on the Demo Board schematic. L2 and C3 minimize EMI noise entering through this connection.

Power Supply Circuit

Figure 6 shows the standard power supply circuit (power supply with capacitive coupling) used in the TERIDIAN Demo Boards. In general, power supplies using transformers will provide better results in EMC/EMI testing.

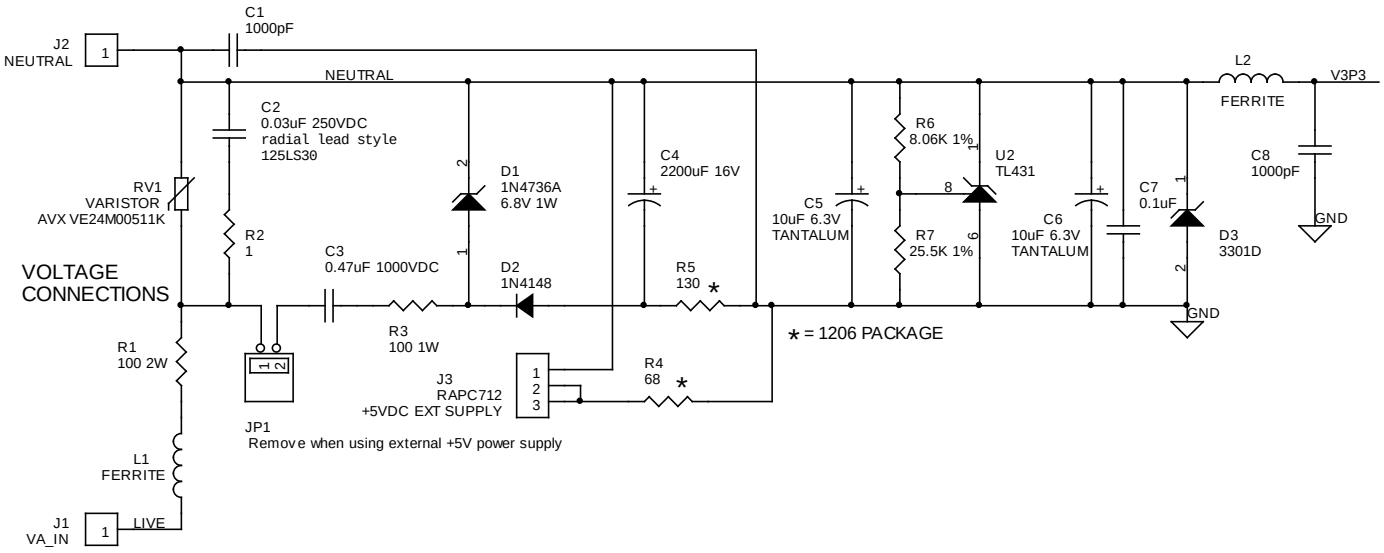

Figure 6: Power Supply Circuit

Key precautions for the power supply circuit are:

1. The Ferrite bead L2 at the V3P3 output prevents high frequency noise.
2. A TVS (Transient Voltage Suppressor, D3) is added to clamp the V3P3 supply voltage to 3.3V. This device may be a bi-directional clamping device to prevent high voltage peaks into the circuit, e.g. the SEMTECH UCLAMP3301D.
3. The resistor R1 is added in series to the varistor (MOV) to limit the surge current. This resistor will cause a voltage drop that helps protecting both the varistor and the meter circuitry. The resistor may be a flameproof 10Ω type rated 3W to 5W.
4. The high-voltage capacitor C2 is added in parallel to the varistor to suppress high-frequency noise. The series resistor R2 (1Ω) is used to dampen oscillations that may occur due to the effective impedance of the power supply.
5. C7 and C8 suppress high-frequency noise.
6. Improved EFT immunity is achieved by replacing C5 and C6 with ceramic type capacitors of values between 10uF to 47uF (even though most Demo Boards utilize a Tantalum capacitor).

Voltage Inputs for Current Shunt Mode

Figure 7 shows the circuit to be used when a 71M65X1 Board is operated in current shunt mode. When using the Demo Boards, JP17 is left open and one of the three wires coming from the line side of the current shunt will connect to JP17, pin 2. C3 and L2 have been added for noise protection of this signal. Capacitor C2 in Figure 7 appears as C14 on the Demo Boards.

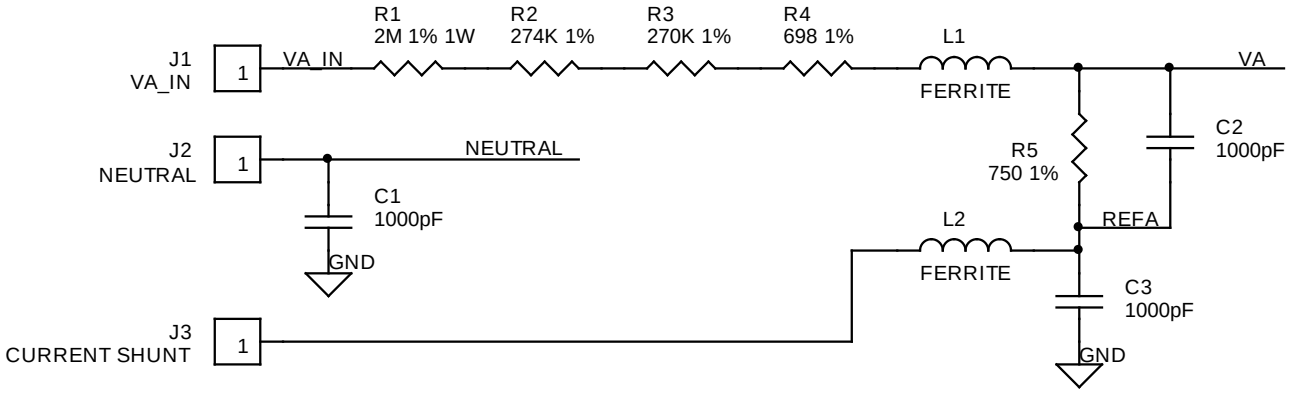

Figure 7: Voltage Input Circuit for Current Shunt Mode

Reset Circuit (71M651X)

The 71M651X does not require an external reset circuit for normal operation. The device incorporates internal power monitoring capability, and connecting the RESETZ pin to V3P3 eliminates device resets due to EFT events. The RESETZ pin of the 71M651X can pick up noise when not properly terminated. Long traces leading to the RESETZ pin must be avoided.

Figure 8 shows a circuit that can be used for experimental or prototyping boards that may need a reset push button. R2, R3, and SW1 should be omitted for production meters.

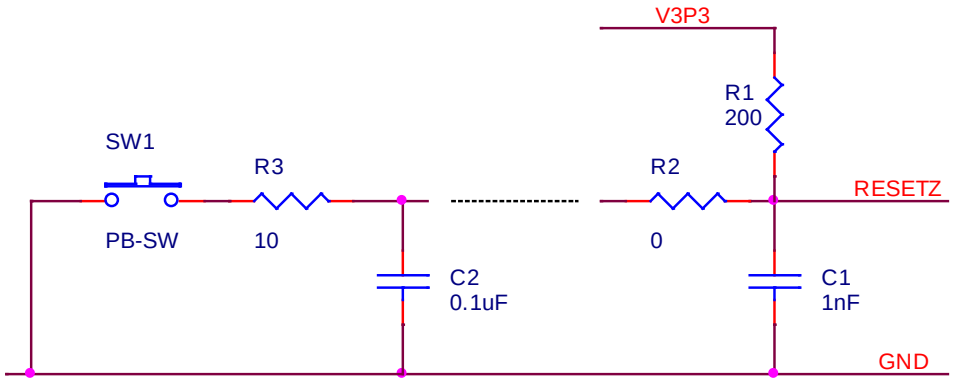

Figure 8: 71M651X Reset Circuit

It is beneficial to terminate the RESETZ signal very close to the 71M651X chip with a strong pull-up resistor and a small capacitor (R1 and C1 in Figure 8). If the reset pushbutton cannot be located right at the chip, another resistor (R2) should be provided between the RESETZ net and the switch. Removing this resistor will separate the switch from the RESETZ pin to ensure proper function in severe EMI/EMC environments.

Reset Circuit (71M652X)

The RESET pin of the 71M652X chips can pick up noise when not properly terminated. Long traces leading to the RESET pin must be avoided. If a reset button is required (prototypes, test units) it should be connected as shown in Figure 9.

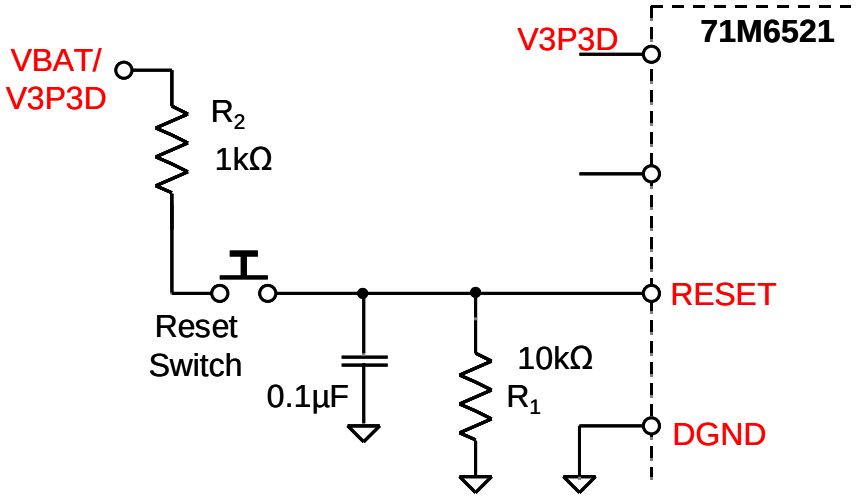

Figure 9: 71M652X Reset Circuit with Reset Button

A more rigid connection suitable for units deployed in the field is shown in Figure 10.

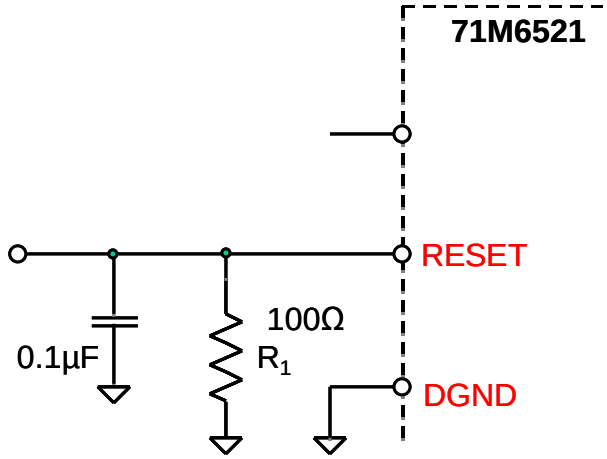

Figure 10: 71M652X Reset Circuit

PB Circuit (71M652X)

The PB pin can be used to provide alternate display functions when supported by firmware. The circuitry to be used for the push button is identical the reset circuit shown above. The same precautions apply to the PB circuit. If the PB function is not required, the PB pin should be connected to ground.

Emulator/Programmer Interface (71M651X)

The E_RTS pin demands the same attention that is paid to the RESETZ and RESET pins. Long traces leading to the E_RTS pin must be avoided. A capacitor to ground close to the E_RST pin at the chip should be added.

The other emulator signals have to be pulled up, as shown in Figure 11

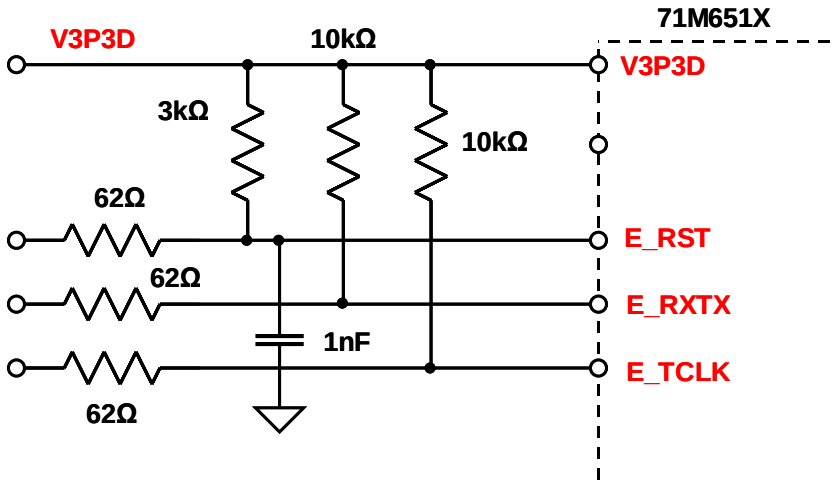

Figure 11: 71M651X Emulator Interface

Emulator/Programmer Interface (71M652X)

In a 71M652X-based design, the E_RST, E_RXTX, and E_TCLK pins may be used to drive segments. In this case it is not practical to connect pull-up resistors sine these would interfere with the LCD segment drive function. An alternative way of protection against EMI is to use a 22pF capacitor to ground for each emulator signal, as shown in Figure 12.

The direct connection from ICE_E to the emulator connector is not required for EMI, but it helps prepare the board for use with the TFP-2 programmer.

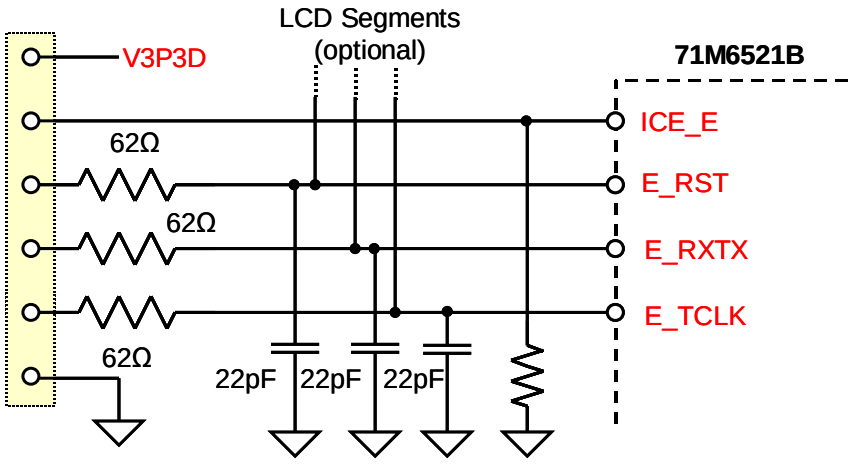

Figure 12: 71M652X Emulator Interface

ICE_E, Emulator Enable (71M652X)

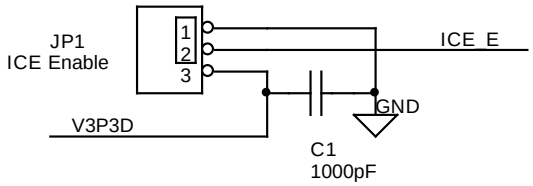

Figure 13: ICE_E Circuit

The ICE_E pin of the 71M652x can be sensitive to RF noise if the header pins are connected by long signal traces to the ICE_E pin (see Figure 13). Components JP1 and C1 should be located adjacent to the device pin.

V1 Circuit (71M651X)

V1 is the power fault input to the 71M651X IC. It can pick up noise when not properly terminated. Any disturbance reaching this pin (e.g. from sensors connected to V3P3) can potentially drive the IC into reset. Long traces leading to the V1 pin must be avoided.

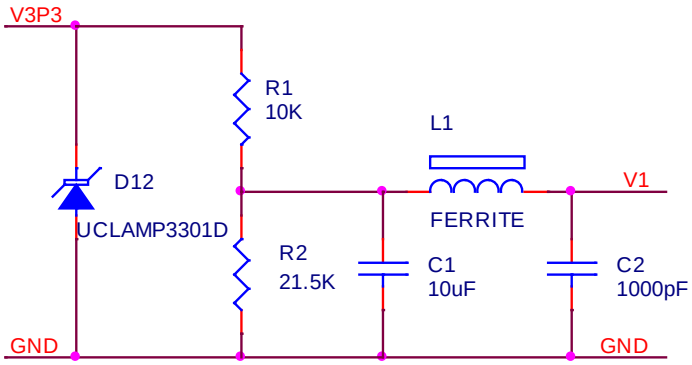

Figure 14: V1 Circuit (71M651X)

V1 should be decoupled with a 10µF tantalum capacitor to ground and held close to 2.5VDC, e.g. by a voltage divider of 10kΩ/21.5kΩ. The capacitor C2 (in Figure 14), in conjunction with the ferrite L1, helps eliminating high-frequency noise. Adjusting V1 too low can have the effect that short sags of the V1 voltage could drive the IC into reset.

V1 Circuit (71M652X)

V1 is the power fault input to the 71M652X IC and provides a means to disable the hardware watchdog timer for debugging and code programming purposes. It can pick up noise when not properly terminated. Any disturbance reaching this pin (e.g. from sensors connected to V3P3) can potentially drive the IC into battery mode. Long traces leading to the V1 pin must be avoided. With proper layout, the circuit for V1 can be simplified to contain only three resistors, as shown in Figure 15.

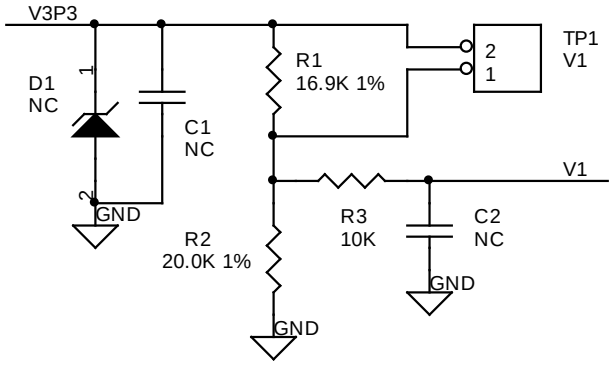

Figure 15: V1 Circuit (71M652X), NC = no connection

When the voltage at the V1 pin falls below +1.6V the device enters its power down mode. When the voltage at the V1 pin is V3P3 (install jumper at TP1) the internal hardware watchdog timer is disabled. It is important to adjust the voltage at V1 to lower than 3.3V – 400mV in order to activate the hardware watchdog timer (WDT). Recommended values are 16.9kΩ for R1 and 20.0kΩ for R2. These values adjust V1 to 1.8VDC when Vin = 3.3V.

Locate components R3 and C2 adjacent to the device pin. C2 is shown as not installed but is recommended as a provisional noise filter. Usage of additional components is dependent on the printed circuit board routing of the V3P3 signal.

The R1 and R2 component values are selected to provide a prompt response to a loss of line power. C4 (2200uF) shown in the power supply circuit provides sufficient holding power to allow the 71M652x to transition to battery power, if available.

TX/RX Pins

The RX pin should be terminated as shown in Figure 16.

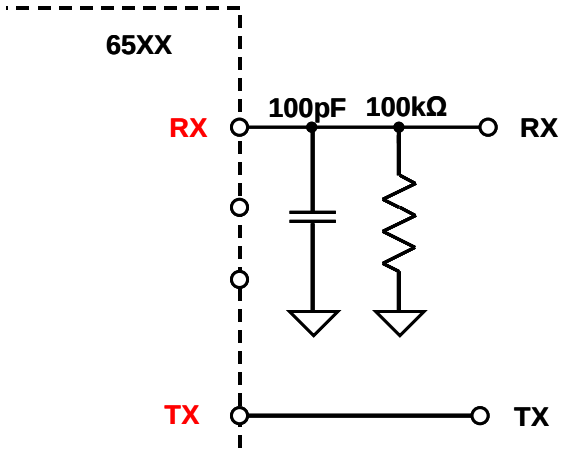

Figure 16: RX Pin

Optical Interface

The pins of the optical interface, when used, should be connected as shown in Figure 17.

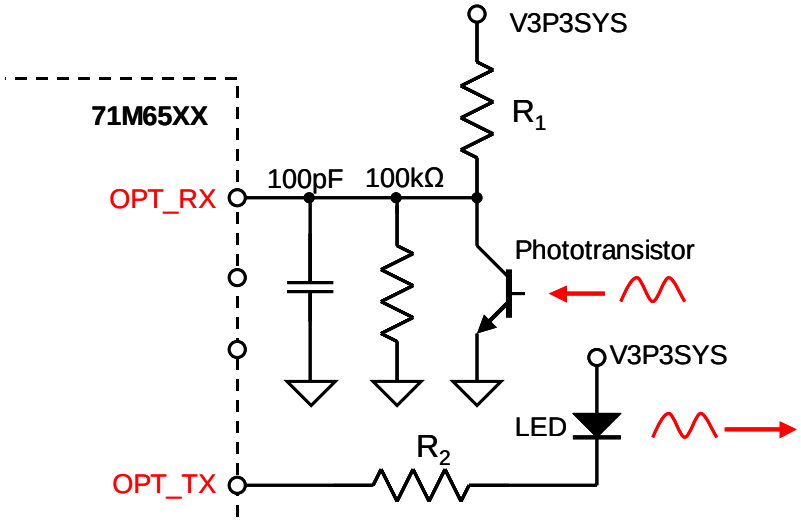

Figure 17: Optical Interface

Other IC Signal Pins

All signals from and to the 71M65XX IC have to be carefully examined for EMI susceptibility. Careful termination helps to defeat unwanted resets or false readings caused by RF fields or EFT events.

The precautions for the other pins for the 71M65XX IC are as follows:

1. Signal input pins (**IA, IB, IC, VA, VB, VC**): All unused current and voltage inputs should be tied to V3P3.
2. A 10µF tantalum capacitor should be used between the **V3P3A** pin of the IC and ground. It should be mounted as close as possible to the 71M65XX IC (C18 on the 71M651X Demo boards)
3. The **VREF** pin should not be connected. The 71M6521 Demo Board includes a test point only for debugging purposes.
4. Any unused pins should be terminated as closely to the IC as possible.
5. A 0.1µF capacitor should be placed between the **V2P5** pin and ground. This improves the operation of the internal regulator used to generate 2.5VDC from 3.3VDC by reducing ripple.
6. Pins **OPT_TX** and **OPT_RX**, when not used, should be tied to V3P3.
7. The **CKTEST/SEG19** pin of the 71M652X can be terminated with 22pF if unused as the clock signal for external circuitry.
8. Unused SSI/segment pins (71M651X) should be disabled on the Demo Boards by removing the resistors R112-R116.
9. When no battery is used, the **VBAT** pin should be tied to V3P3.
10. The **V3** pin on the 71M6513, if not used, should be left floating or tied to VREF. The V3 interrupt should be disabled.
11. Connect the **X4MHZ** and **TEST** pins (71M652X) directly to ground.

General Layout Precautions

The most successful layouts use four layers, with the two internal layers being ground and V3P3. If two-layer boards are used, the layout has to be designed very carefully, and the following rules have to be observed:

1. Component placement is very critical, especially for the signals/pins such as XIN/XOUT, V1, 4MHZ, RESET/RESETZ, ICE_E, and TEST. Components associated with these pins should be placed as close to the IC as possible. The shorter the traces, the better.
2. The integrity of the ground plane is very important to protect the digital inputs such as RESETZ/RESET, V1, RX, ICE_E, PB, TEST, and 4MHZ. Pull-up, pull-down resistors, and bypass capacitors attached to these pins should be placed close to the IC and their ground contacts should be connected directly to a solid ground plane.
3. It is helpful to keep the high-voltage and low-voltage sections of the board clearly separated.
4. One side of the board should be reserved for a ground layer, while the other side should be used for routing. Voids in the ground layer should be minimized. If interruptions in the ground layer must be made to allow for traces, these interruptions should be bridged by copper structures on the opposing layer.
5. Ground and V3P3 traces should be widened (using copper pour techniques) to become virtual planes. Naturally, it is impossible to route a 2-layer board with continuous copper planes. However, ground and V3P3 structures can be placed on both sides of the board and then “stitched” together with free vias, creating good connectivity for both V3P3 and ground.
6. Ground and V3P3 nets should have star points close to the 71M65XX IC. These star points should be connected by a bulk capacitor (10µF or more). This capacitor works better if it is a ceramic type and if it is placed closely to the V3P3 and GND start points.
7. The V3P3A plane for measurement should be wide enough to act as a stable reference for the measurement signals. The wider the V3P3A copper structure is, the better the measurement performance of the meter will be. All V3P3 structures should come together at a star point close to the V3P3A pin of the IC.
8. The crystal should be positioned as close as possible to the 71M65XX IC and rotated properly to make the traces short. No other traces should cross the traces between the IC and the crystal on the other side of the board. The parallel resistor implemented in some Demo Boards is not needed. It is a good measure to place a separate ground structure underneath the crystal.
9. Slots cut into the PCB should be used for isolation where high-voltage signals are located close to low-voltage signals. This maintains separation between high-voltage signals without using too much board space and prevents arching or leakage currents when the PCB surface is not perfectly clean.
10. Analog input traces running parallel should be separated by grounded guard traces.
11. Avoid running clock traces like XIN/XOUT, E_TCLK and sensitive traces like E_RST in parallel.
12. Avoid using sockets for components.

71M651X Layout Precautions

1. For a good example of a 71M6511 two-layer board, examine the 71M6511 2-Layer Demo Board (see Figure 19 and Figure 20).
2. It is unrelated to EMI (but very important none the less) when using the 71M6513 chip, to make sure that no traces or vias are located in the area that is covered by the 5mm x 5mm exposed ground pad (for an example, see Figure 18, showing routing patterns that are not recommended).

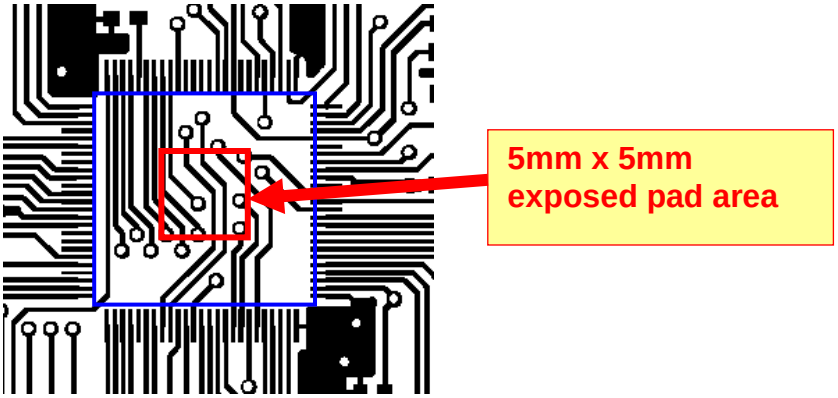

Figure 18: Problematic Routing underneath 71M6513 Chip

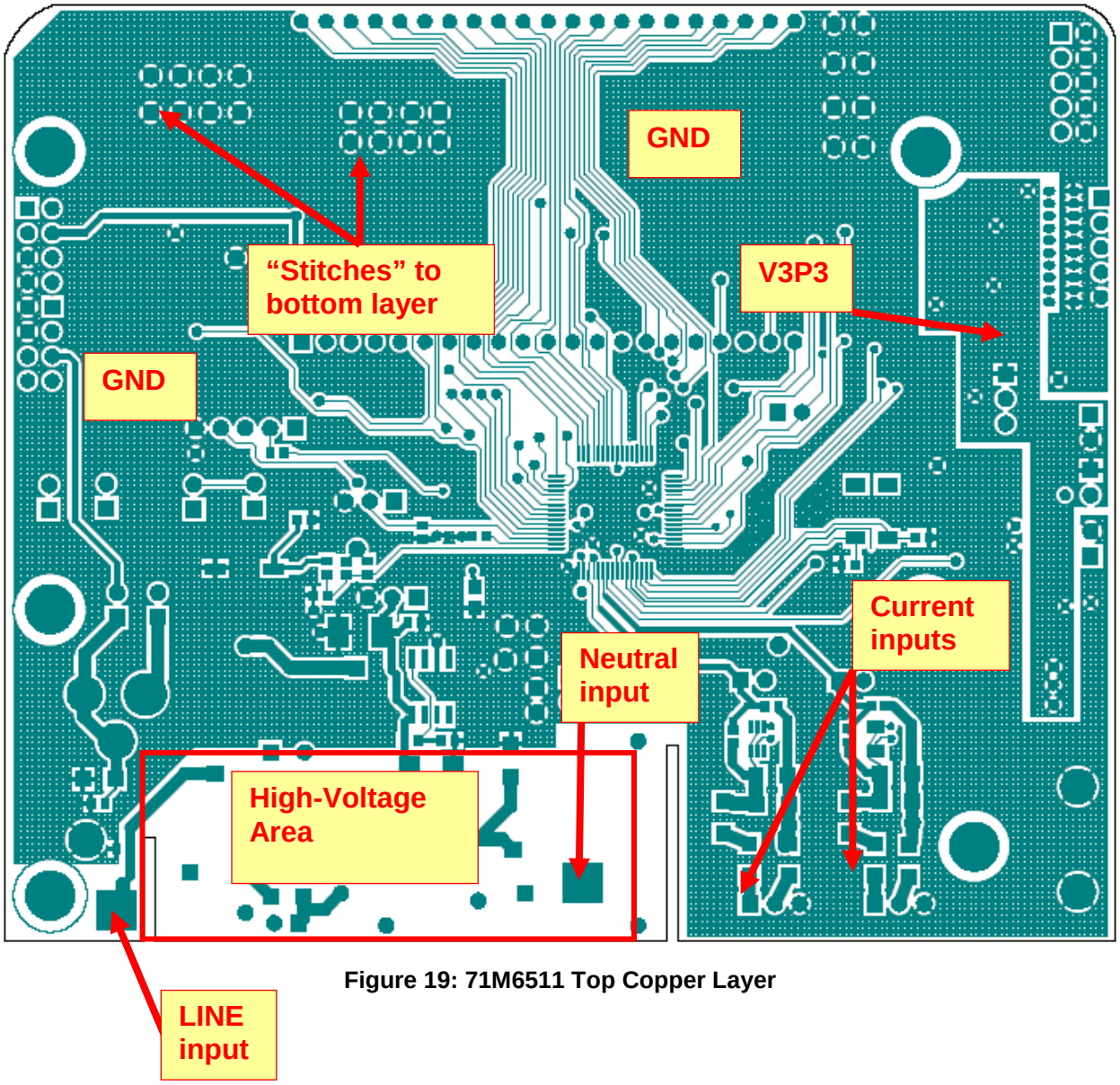

Figure 19: 71M6511 Top Copper Layer

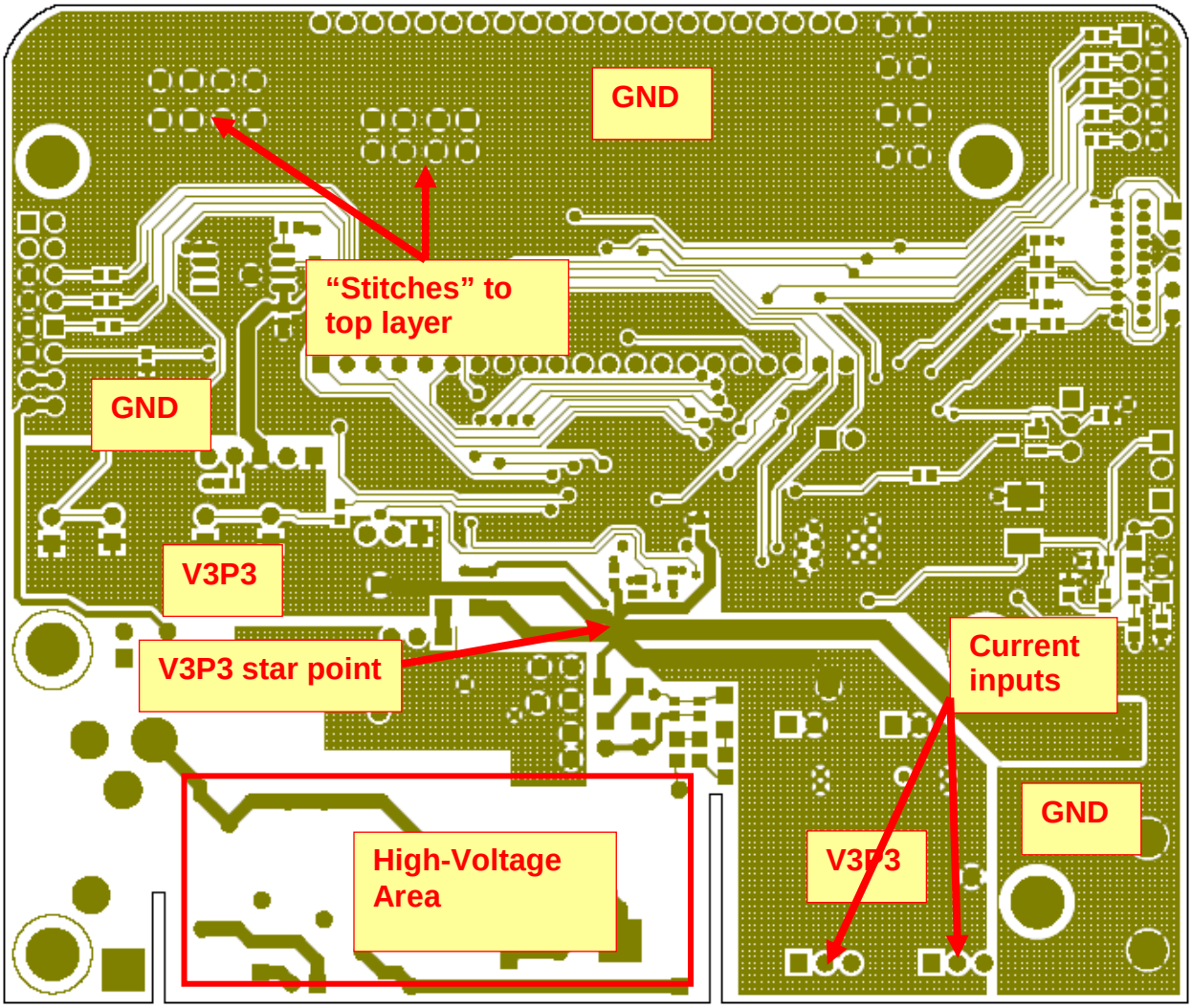

Figure 20: 71M6511 Bottom Copper Layer

71M652X Layout Precautions

The layout precautions for 71M652X-based designs are almost identical to those for 71M651X-based designs. However, special care has to be taken for the V3P3D net, which is an output for the 71M652X IC. It is useful to make the traces attached to V3P3D a larger copper structure.

The ground areas shown on the left and right side of the LCD display in Figure 21 are connected on the bottom layer with a copper structure (shown in red). Figure 21also shows clearly the separation between the V3P3A structures for channel A and channel B current inputs.

Figure 22 shows the bottom copper layer with the ground structures exactly mirroring the V3P3 structures on the top layer.

Unrelated to EMI, the 68-pin version of the 71M6521 incorporates an exposed ground pad on the bottom side of the device. Do not route traces or place vias under the device.

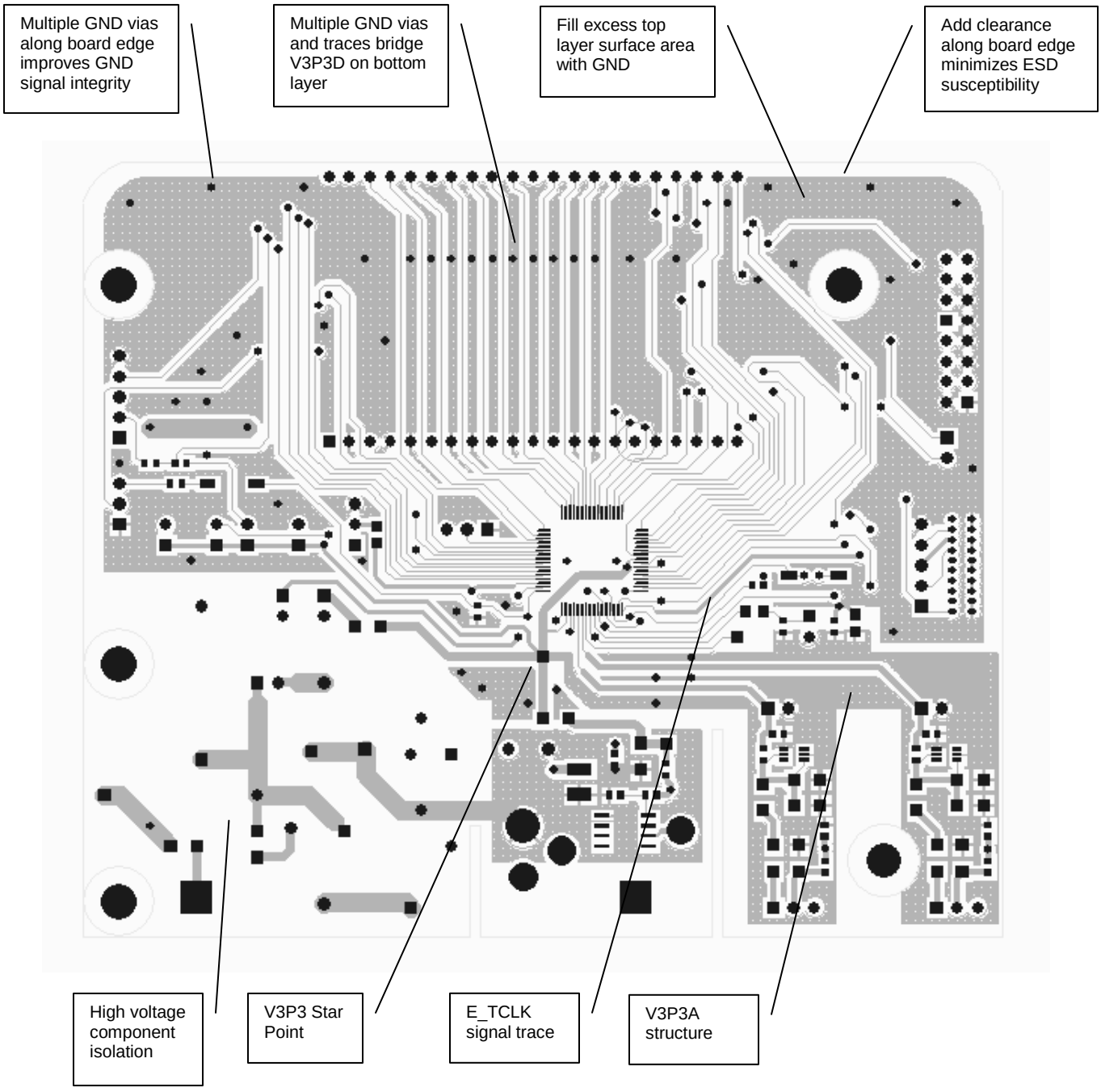

Figure 21: 71M6521 Top Copper Layer

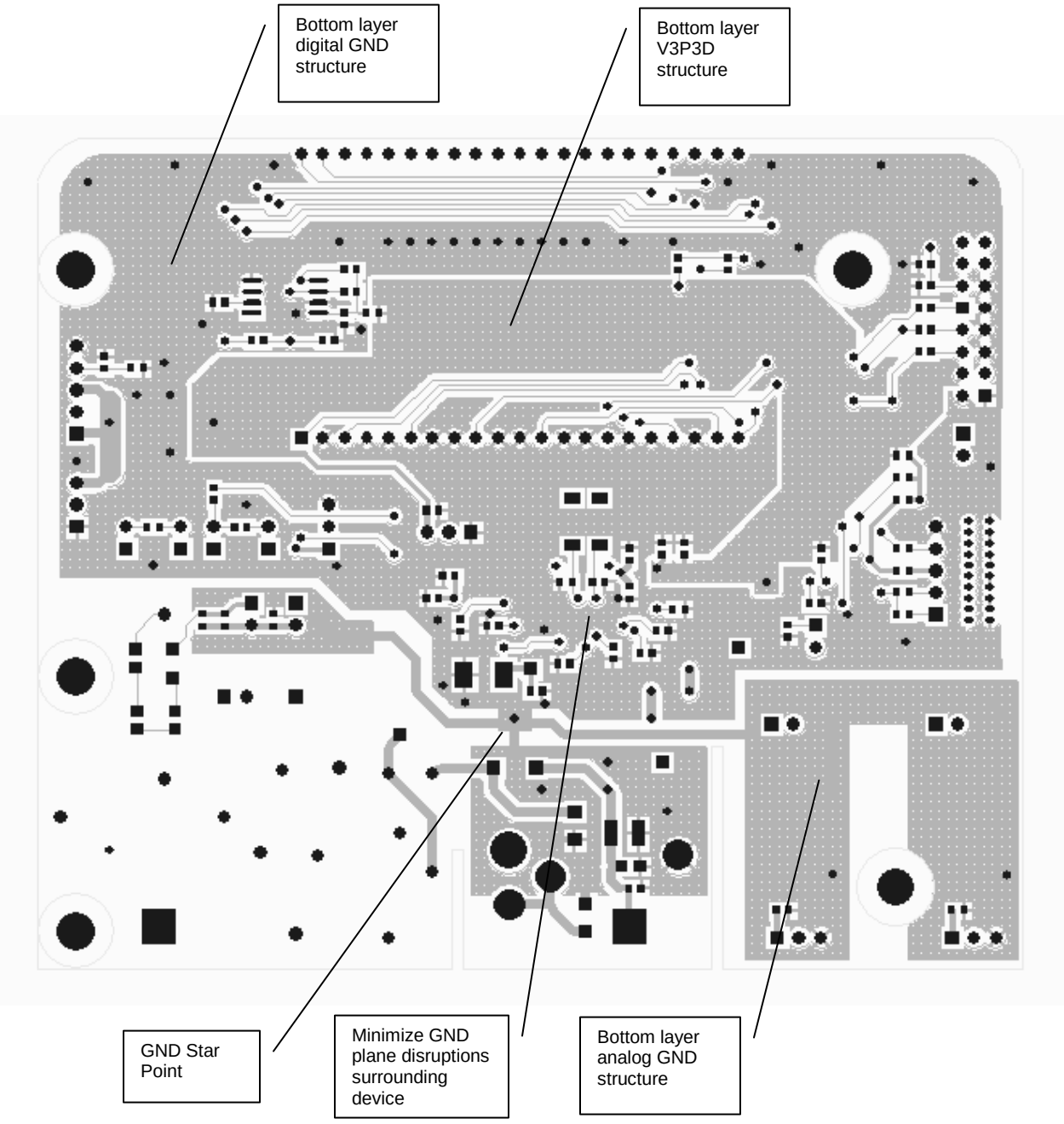

Figure 22: 71M6521 Bottom Copper Layer

External Components

With good schematic design, proper component placement and good layout, external components for EMI suppression should rarely be necessary.

When schematic design and layout rules have been violated, which is frequently the case for prototypes and boards with modifications for test purposes, external components may have to be added to pass EMI/EMC testing, such as ferrites placed around the sensor and other external wiring.

Figure 23 shows an older 71M6511 2-Layer Demo Board modified to pass **30V/m RF** immunity testing.

A large clamp-on ferrite (1) is used for the power-entry cable, and two smaller clamp-on ferrites (2) are attached to the Shunt Resistor wiring. Another small toroid ferrite (3) is attached to the power-entry wire to the board.

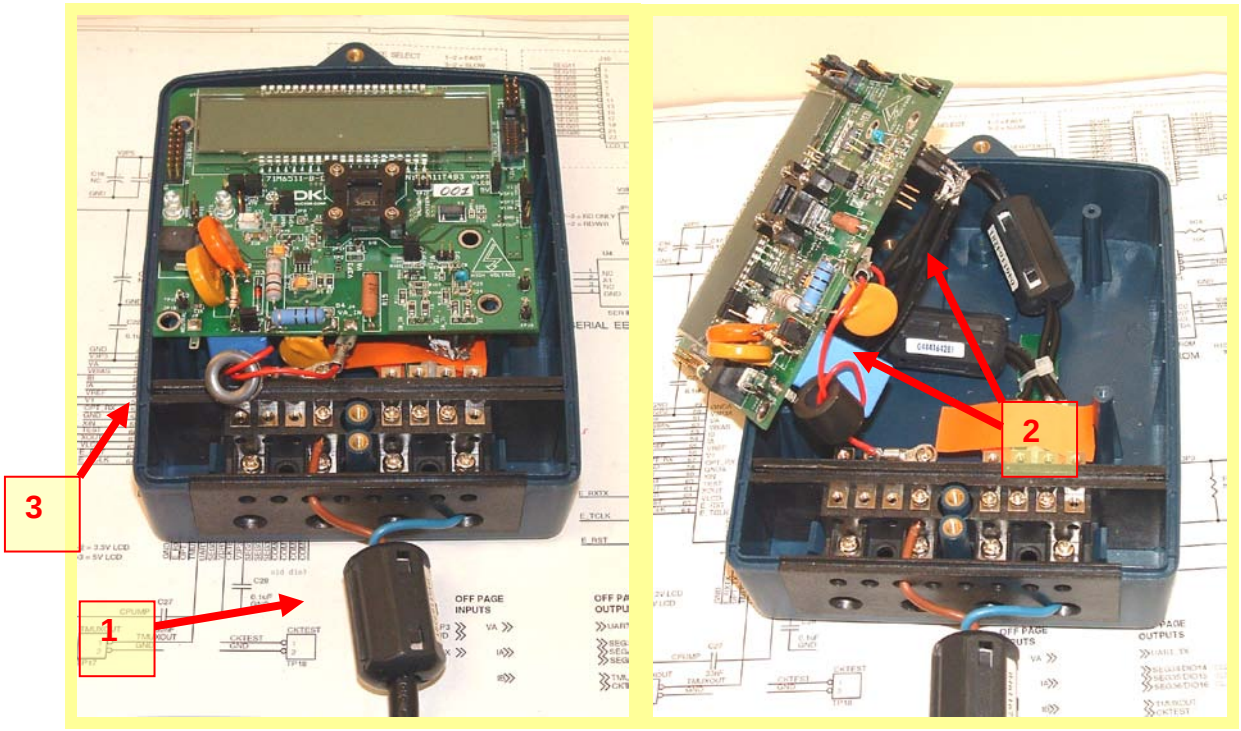

Figure 23: 71M6511 2-Layer PCB with external components

Firmware/Configuration Precautions

1. All unused DIO pins should be configured as outputs. This way no unwanted signals enter the IC.
2. The emulator clock should be disabled (by configuring *ECK_DIS* at I/O RAM 0x2005 Register Bit 5 to 1) so that no 5MHz clock is generated at the emulator port. This prevents any emissions due to the 5MHz clock signal. This also causes the emulator port to be disabled, which may be an issue if the IC has to be re-programmed. A good way to make the IC accessible to emulators and programmers is to set the *ECK_DIS* later than 1000ms after the code starts. This gap in time gives emulators and programmers a chance to react to the reset signal.
3. The RTM clock output should be disabled (by configuring *CKOUT_DIS* to 1) when no Real-Time monitoring is performed with the production version of the firmware.
4. The TMUXOUT output pin should be disabled by setting *TMUX* = 0.
5. Dummy interrupt service routines containing a RETI instruction should be placed at all locations pointed to by unused interrupt vectors.
6. All interrupt service routines (ISRs) should be as short as possible and should be minimized for memory manipulation operations.