

# ESD Protection Diode

## Micro-Packaged Diodes for ESD Protection



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

## ESD9X3.3ST5G Series, SZESD9X3.3ST5G Series

The ESD9X Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space is at a premium.

### Specification Features:

- Low Clamping Voltage
- Small Body Outline Dimensions:  
0.039" x 0.024" (1.0 mm x 0.60 mm)
- Low Body Height: 0.017" (0.43 mm) Max
- Stand-off Voltage: 3.3 V – 12 V
- Low Leakage
- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000-4-2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices

### Mechanical Characteristics:

**CASE:** Void-free, transfer-molded, thermosetting plastic  
Epoxy Meets UL 94 V-0

**LEAD FINISH:** 100% Matte Sn (Tin)

**MOUNTING POSITION:** Any

**QUALIFIED MAX REFLOW TEMPERATURE:** 260°C

Device Meets MSL 1 Requirements

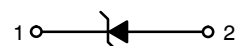
### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±30 ±30	kV
ESD Voltage Per Human Body Model Per Machine Model		16 400	kV V
Total Power Dissipation on FR-5 Board (Note 1) @ T <sub>A</sub> = 25°C	P <sub>D</sub>	150	mW
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Second Duration)	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



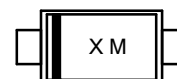
PIN 1. CATHODE  
2. ANODE

SCALE 8:1



SOD-923  
CASE 514AB

MARKING  
DIAGRAM



X = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
ESD9XxxST5G	SOD-923 (Pb-Free)	8000/Tape & Reel
SZESD9XxxST5G	SOD-923 (Pb-Free)	8000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the table on page 2 of this data sheet.

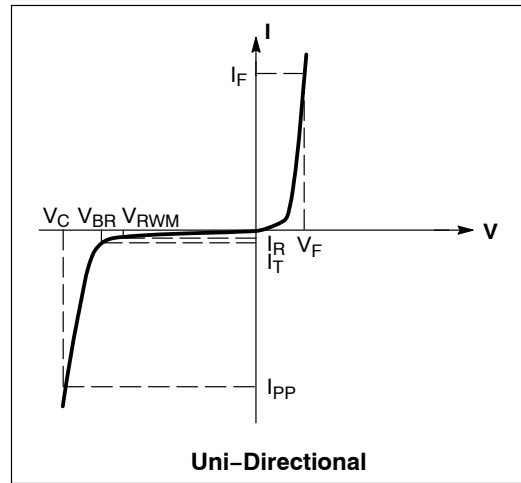
# ESD9X3.3ST5G Series, SZESD9X3.3ST5G Series

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Max. Capacitance @ $V_R = 0$ and $f = 1$ MHz

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted, $V_F = 1.1$ V Max. @ $I_F = 10$ mA for all types)

Device*	Device Marking	$V_{RWM}$ (V)	$I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)	$I_T$	Max $I_{PP}$ (A) (Note 3)	$V_C$ (V) @ Max $I_{PP}$ (Note 3)	$P_{pk}$ (W) (8 x 20 $\mu\text{s}$ )	C (pF)	$V_C$
		Max	Max	Min	mA		Max	Typ	Typ	Per IEC61000-4-2 (Note 4)
ESD9X3.3ST5G	A	3.3	2.5	5.0	1.0	9.8	10.4	102	80	Figures 1 and 2 (Note 5)
ESD9X5.0ST5G	B	5.0	1.0	6.2	1.0	8.7	12.3	107	65	
ESD9X7.0ST5G	5**	7.0	0.1	7.5	1.0	4.0	25	100	65	
ESD9X12ST5G	C	12	1.0	13.5	1.0	5.9	23.7	140	30	

\* Include SZ-prefix devices where applicable.

\*\*Rotated 270 degrees.

- $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .
- Surge current waveform per Figure 5.
- For test procedure see Figures 3 and 4 and Application Note AND8307/D.
- ESD9X5.0ST5G shown below. Other voltages available upon request.

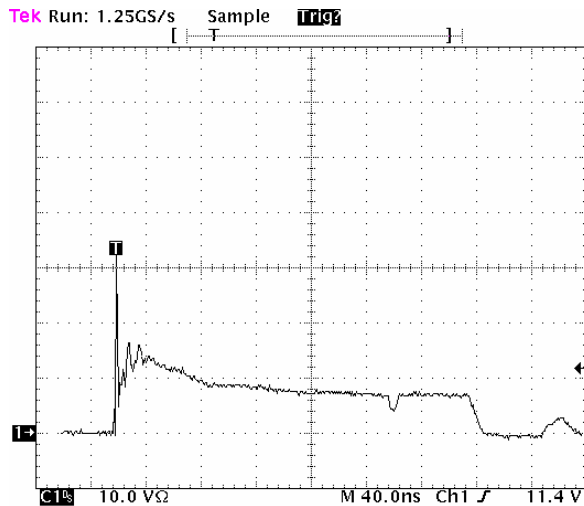


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

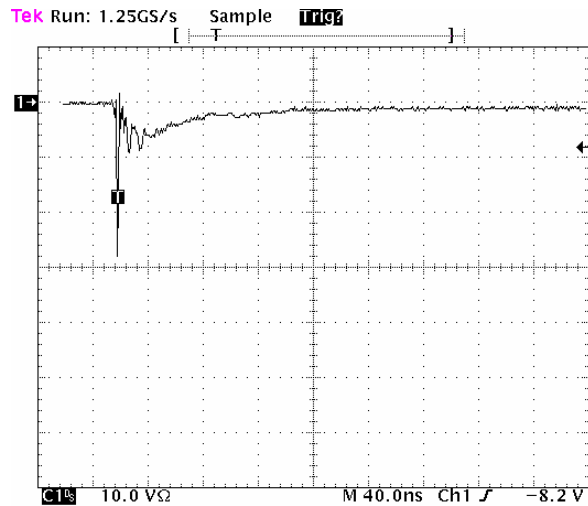


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

# ESD9X3.3ST5G Series, SZESD9X3.3ST5G Series

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 3. IEC61000-4-2 Spec

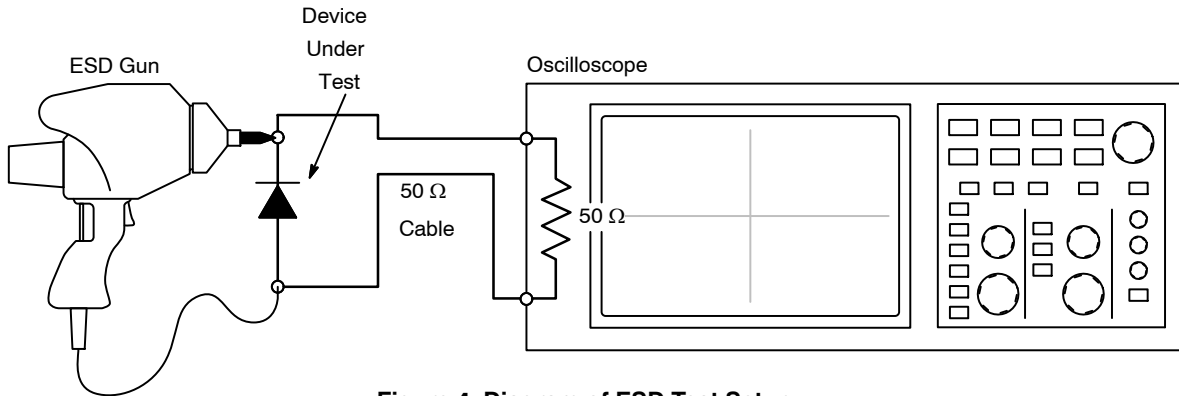


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

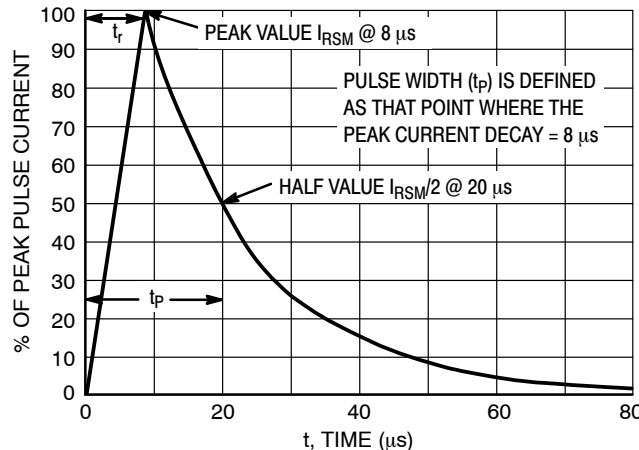
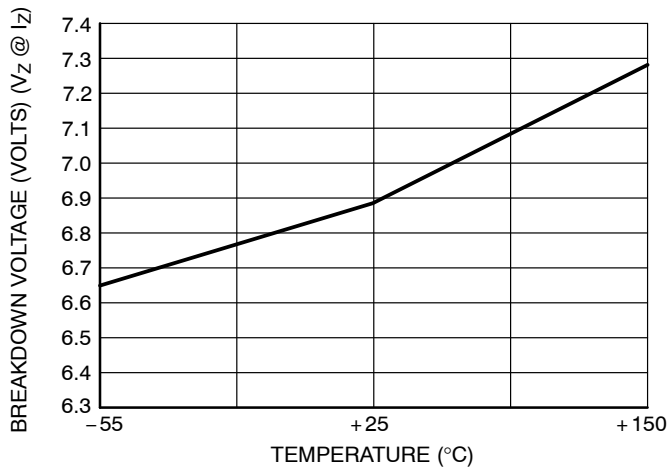


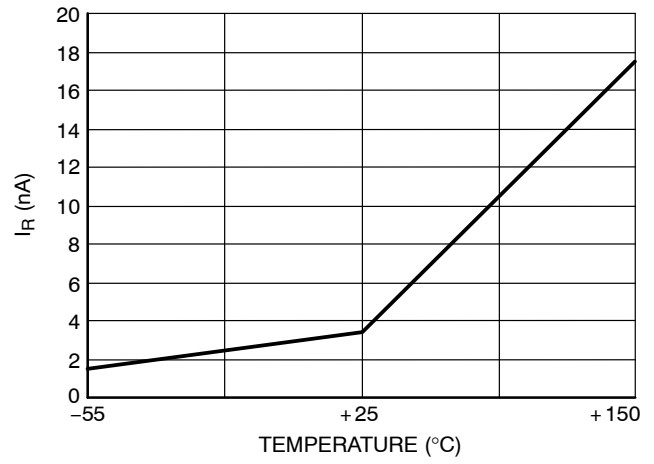
Figure 5. 8 x 20 μs Pulse Waveform

# ESD9X3.3ST5G Series, SZESD9X3.3ST5G Series

## TYPICAL CHARACTERISTICS



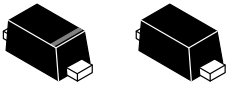
**Figure 6. Typical Breakdown Voltage versus Temperature**



**Figure 7. Typical Leakage Current versus Temperature**

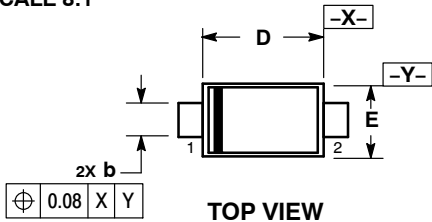
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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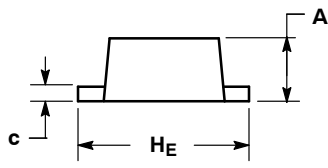


STYLE 1    STYLE 2

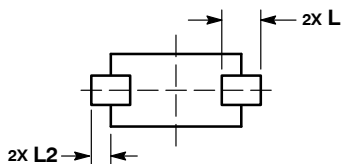
SCALE 8:1



TOP VIEW

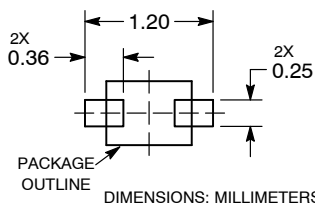


SIDE VIEW



BOTTOM VIEW

### SOLDERING FOOTPRINT\*



SOD-923  
CASE 514AB  
ISSUE D

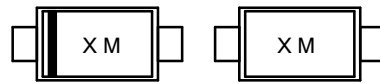
DATE 03 SEP 2020

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSION L WILL NOT EXCEED 0.30mm.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H <sub>E</sub>	0.95	1.00	1.05	0.037	0.039	0.041
L	0.19 REF			0.007 REF		
L2	0.05	0.10	0.15	0.002	0.004	0.006

### GENERIC MARKING DIAGRAM\*



STYLE 1

STYLE 2

X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:  
PIN 1. CATHODE (POLARITY BAND)  
2. ANODE

STYLE 2:  
NO POLARITY

See Application Note AND8455/D for more mounting details

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>SOD-923, 1.0X0.6X0.37, MAX HEIGHT 0.40</b>	<b>PAGE 1 OF 1</b>

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