IntelliMAX™ 28 V, Over-Voltage, Over-Current Protection Load Switch with Adjustable Current-Limit Control

ON Semiconductor®

www.onsemi.com

FPF2495B

WLCSP9 1.22x1.22x0.581
CASE 567SU

Description

The FPF2495B advanced load−management switch targets applications requiring a highly integrated solution. It disconnects loads powered from the DC power rail (<6 V) with stringent off−state current targets and high load capacitances (<100 μF). The FPF2495B consists of a slew−rate controlled low−impedance MOSFET switch (100 mΩ maximum) and integrated analog features. The slew−rate controlled turn−on characteristic prevents inrush current and the resulting excessive voltage droop on power rails. FPF2495B has over−voltage protection and over−temperature protection.

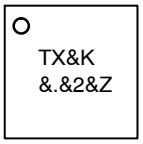
The FPF2495B has a Reverse−Current Blocking (RCB) function that obstructs unwanted reverse current from V_{OUT} to V_{IN} during OFF states. The exceptionally low off−state current drain (<2 μA maximum) facilitates compliance with standby power requirements. The input voltage range operates from 2.5 V to 5.5 V_{DC} to support a wide range of applications in consumer, optical, medical, storage, portable, and industrial−device power management. Switch control is managed by a logic input (active HIGH) capable of interfacing directly with low−voltage control signal / General−Purpose Input / Output (GPIO) without an external pull−down resistor.

The device is packaged in advanced, fully “green” compliant, 1.22 mm x 1.22 mm, Wafer−Level Chip−Scale Package (WLCSP).

Features

- V_{IN}: 2.5 V~5.5 V
- 28 V Absolute Ratings at V_{OUT}
- Current Capability: 2.8 A
- Adjustable Current Limit: 0.05 A ~ 2.5 A (Typ.)
  - 0.1 A~2.5 A with 10% Accuracy
  - < 0.1 A with 15% Accuracy
- R_{ON}: Typ. 70 mΩ & Max. 100 mΩ at 5 V_{IN} and 1 A I_{OUT}
- Output OVP: Min. = 5.6 V, Typ. = 5.8 V, Max. = 6 V
- No Output Discharge During Off State
- Open−Drain OCP on FLAGB
- Thermal Shutdown
- Under−Voltage Lockout (UVLO)
- Reverse−Current Blocking (RCB) during OFF
- Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements
- ESD Protected:
  - Human Body Model: >2 kV
  - Charged Device Model: >2.5 kV
  - IEC 61000−4−2 Air Discharge: >15 kV
  - IEC 61000−4−2 Contact Discharge: >8 kV

MARKING DIAGRAM



TX	= ON Semiconductor Logo = Specific Device Code
&K	= Lot Code
&2	= Numeric Date Code
&Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

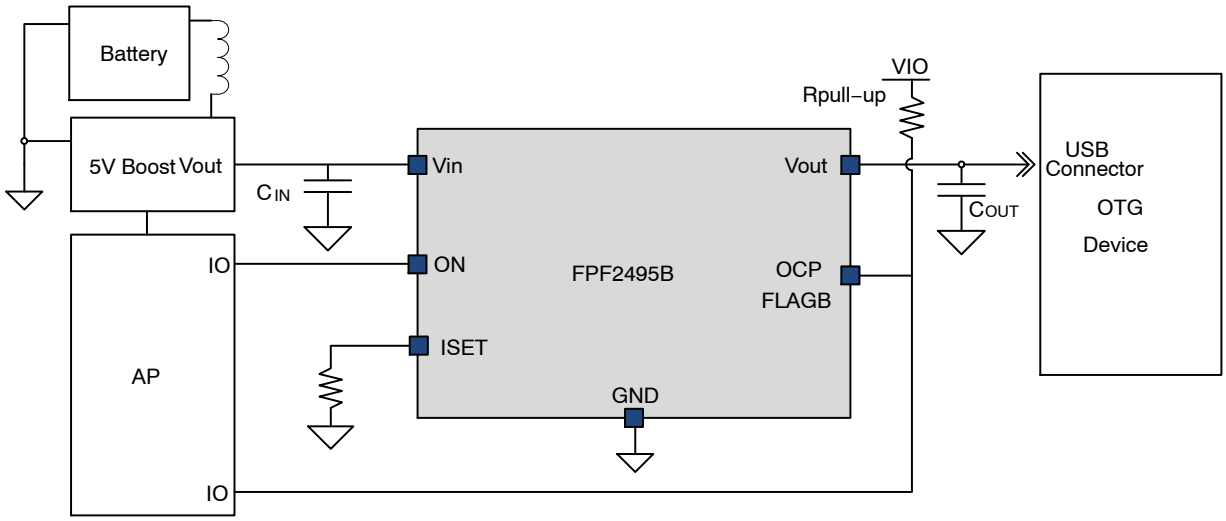
Applications

- Smart Phones, Tablet PCs
- Storage, DSLR, and Portable Devices

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method	Top Mark
FPF2495BUCX	−40 to 85°C	9−Ball, WLCSP, 3x3 Array, 0.4 mm Pitch, Back Side Lamination	Tape & Reel	TX

Application Diagram



1. C_{IN} and C_{OUT} capacitors recommended for improvement of device stability.

Figure 1. Typical Application

Functional Block Diagram

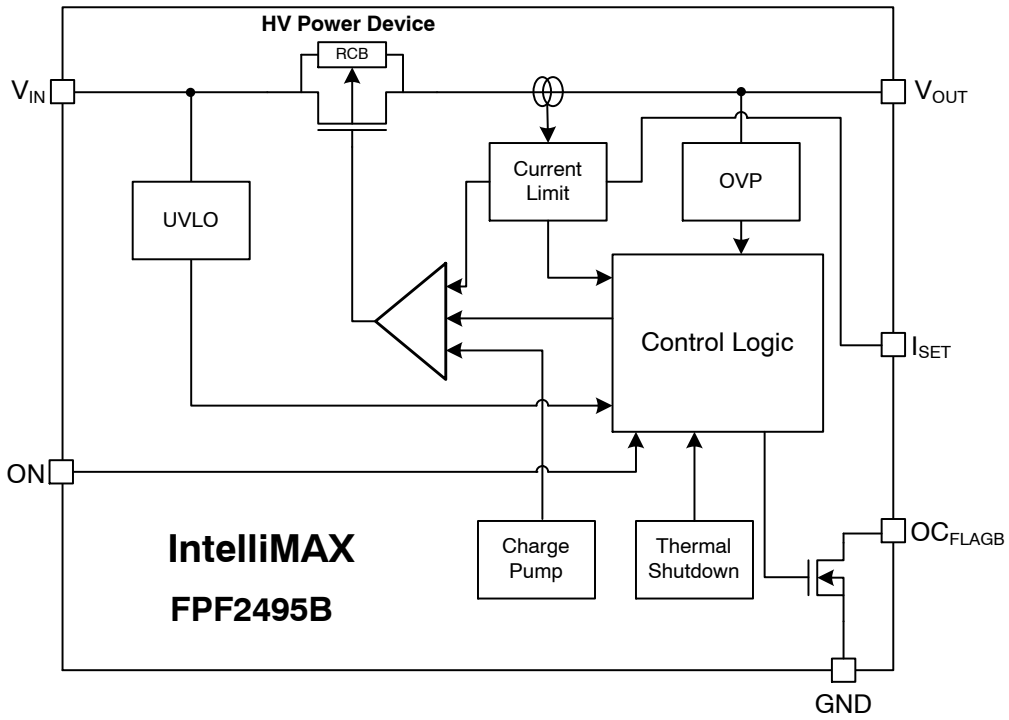


Figure 2. Functional Block Diagram

Pin Configurations

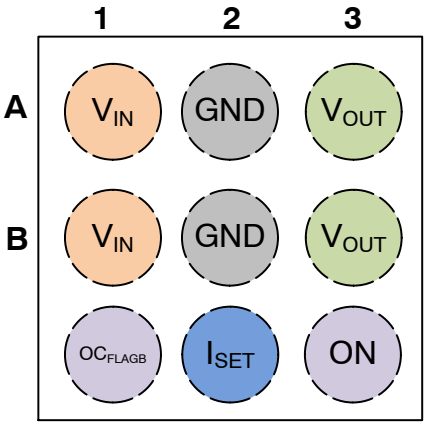


Figure 3. Pin Assignments (Top View)

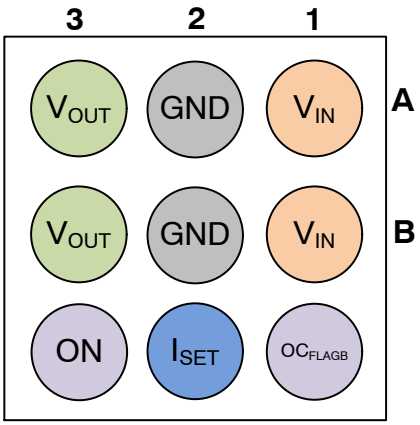


Figure 4. Pin Assignments (Bottom View)

PIN DESCRIPTION

Pin #	Name	Description		
A3, B3	V_{OUT}	**Switch Output**		
A1, B1	V_{IN}	**Supply Input**: Input to the power switch		
A2	GND	**Ground** (true device ground)		
B2				
C3	ON	**ON/OFF Control Input**: Active HIGH – GPIO compatible	Logic HIGH	Switch Enable
			Logic LOW	Switch Disable
C1	OC_{FLAGB}	**Fault Output**: Active LOW, open−drain output that indicates an input over current. External pull−up resistor to V_{CC} is required.		
C2	I_{SET}	**Current Limit Set Input**: A resistor from ISET to ground sets the current limit for the switch.		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters		Min.	Max.	Unit
V_{PIN}	V_{OUT} to GND, V_{OUT} to V_{IN}		−0.3	28.0	V
	ON, V_{IN}, FLAGB, I_{SET} to GND		−0.3	6.0	
I_{SW}	Maximum Continuous Switch Current (Note 1)			2.8	A
t_{PD}	Total Power Dissipation at T_A = 25°C			1.0	W
T_J	Operating Junction Temperature		−40	+150	°C
T_{STG}	Storage Junction Temperature		−65	+150	°C
θ_{JA}	Thermal Resistance, Junction−to−Ambient (1−inch Square Pad of 2 oz. Copper)			95 (Note 2)	°C/W
				110 (Note 3)	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114	2.0		kV
		Charged Device Model, JESD22−C101	2.5		
	IEC61000−4−2 System Level	Air Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	15.0		
		Contact Discharge (V_{IN}, V_{ON}, V_{OUT} to GND)	8.0		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Junction Temperature = 85°C.

2. Measured using 2S2P JEDEC std. PCB.
3. Measured using 2S2P JEDEC PCB cold plate method.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameters	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN} = 2.5 to 5.5 V, T_A = −40 to +85°C; typical values are at V_{IN} = 5 V and T_A = 25°C.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
BASIC OPERATION						
V_{IN}	Input Voltage		2.5		5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON} = GND, V_{OUT} = Open		1	2	μA
$I_{SD(OFF)}$	Shutdown Current	V_{IN} = 5.5 V, V_{OUT} = 0 V, V_{ON} = GND		0.1	4.0	μA
I_Q	Quiescent Current	I_{OUT} = 0 mA		65	100	μA
R_{ON}	On Resistance	V_{IN} = 5.0 V, I_{OUT} = 1 A		70	100	mΩ
		V_{IN} = 3.7 V, I_{OUT} = 1 A		75	105	
R_{ON}	On Resistance[6]	V_{IN} = 5.0 V, I_{OUT} = 1.5 A		70		mΩ
V_{IH}	ON Input Logic HIGH Voltage	V_{IN} = 2.5 V to 5.5 V	1.15			V
V_{IL}	ON Input Logic LOW Voltage	V_{IN} = 2.5 V to 5.5 V			0.65	V
V_{IL_FLAG}	FLAGB Output Logic LOW Voltage	V_{IN} = 5 V, I_{SINK} = 10 mA		0.1	0.2	V
		V_{IN} = 2.5 V, I_{SINK} = 10 mA		0.15	0.30	
I_{FLAGB_LK}	FLAGB Output HIGH Leakage Current	V_{IN} = 5 V, Switch On			1	μA
I_{ON}	On Input Leakage	V_{ON} = 0 V to V_{IN}			1.0	μA
R_{ON_PD}	Pull−Down Resistance at ON Pin	V_{IN} = 2.5~5.5 V, V_{ON} = HIGH, T_A = −40 to 85°C		14		MΩ
OVER−VOLTAGE PROTECTION						
V_{OV_TRIP}	Output OVP Lockout	V_{OUT} Rising Threshold	5.50	5.80	6.00	V
		V_{OUT} Falling Threshold		5.50		
OUT_{HYS}	Output OVP Hysteresis	V_{OUT} Falling Threshold		0.3		V
t_{OVP}	OVP Response Time[6]	I_{OUT} = 0.5 A, C_L = 1 μF, T_A = 25°C, V_{OUT} from 5.5 V to 6.0 V	1		4[6]	μs
OVER−CURRENT PROTECTION						
I_{LIM}	Current Limit	V_{IN} = 5 V, R_{SET} = 20000 Ω, V_{OUT} = 1.68 to 5 V with 15% Accuracy (Note 4)	42	50	58	mA
		V_{IN} = 5 V, R_{SET} = 2100 Ω, V_{OUT} = 1.68 to 5 V with 10% Accuracy (Note 4)	450	500	550	
		V_{IN} = 5 V, R_{SET} = 1070 Ω, V_{OUT} = 1.68 to 5 V with 10% Accuracy (Note 4)	900	1000	1100	
V_{UVLO}	Under−Voltage Lockout	V_{IN} Increasing		2.4		V
		V_{IN} Decreasing		2.2		
V_{UVLO_HYS}	UVLO Hysteresis			200		mV
I_{RCB}	RCB Current	V_{ON} = 0 V, V_{OUT} = 5.5 V,		7		μA
t_{HOCP}	Hard Over−Current Response Time	Moderate Over−Current Condition, $I_{OUT} \geq I_{LIM}$, V_{OUT} = 0 V		6		μs

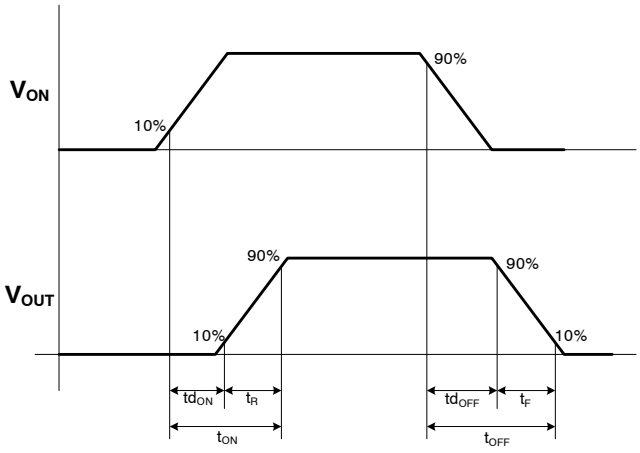
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted; V_{IN} = 2.5 to 5.5 V, T_A = −40 to +85°C; typical values are at V_{IN} = 5 V and T_A = 25°C.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Unit
OVER−CURRENT PROTECTION						
t_{OCP}	Over−Current Response Time	Moderate Over−Current Condition, $I_{OUT} \geq I_{LIM}$ $V_{OUT} \leq V_{IN}$		7		μs
t_{OC_FLAG}	Over−Current Flag Response Time	When Over−Current Occurs to Flag Pulling LOW		8		ms
TSD	Thermal Shutdown	Shutdown Threshold		150		°C
		Return from Shutdown		130		
		Hysteresis		20		
DYNAMIC CHARACTERISTICS						
t_{DON}	Turn−On Delay (Note 5, 6)	V_{IN} = 5 V, R_L = 100 Ω, C_L = 1 μF, T_A = 25°C, R_{SET} = 2040 Ω		0.67		ms
t_R	V_{OUT} Rise Time (Note 5, 6)			0.69		ms
t_{ON}	Turn−On Time (Note 5, 7)			1.36		ms
t_{DOFF}	Turn−Off Delay (Note 6, 5)			0.01		ms
t_F	V_{OUT} Fall Time (Note 6, 5)			0.22		ms
t_{OFF}	Turn−Off Time (Note 8, 5)			0.23		ms
t_{DON}	Turn−On Delay (Note 6, 9)	V_{IN} = 5 V, R_L = 3.8 Ω, C_L = 10 μF, T_A = −40 to 85°C, R_{SET} = 634 Ω		0.65	0.78	ms
t_R	V_{OUT} Rise Time (Note 6, 9)			0.65	0.82	ms
t_{ON}	Turn−On Time (Note 7, 9)			1.3	1.6	ms
t_{DOFF}	Turn−Off Delay (Note 6, 9)			4	10	μs
t_F	VOUT Fall Time (Note 6, 9)			76	120	μs
t_{OFF}	Turn−Off Time (Note 8, 9)			80	130	μs

4. Characterization based on 1% tolerance resistor.
5. This parameter is guaranteed by design and characterization; not production tested.
6. $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 5 below.
7. $t_{ON} = t_R + t_{DON}$.
8. $t_{OFF} = t_F + t_{DOFF}$.
9. This parameter is guaranteed by design.

TIMING DIAGRAM



where:

t_{DON} = Delay On Time
t_R = V_{OUT} Rise Time
t_{ON} = Turn−On Time
t_{DOFF} = Delay Off Time
t_F = V_{OUT} Fall Time
t_{OFF} = Turn Off Time

Figure 5. Timing Diagram

OPERATION AND APPLICATION DESCRIPTION

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into discharge load capacitor; a capacitor must be placed in between the V_{IN} and GND pins. A high−value capacitor on C_{IN} can be used to reduce the voltage drop in high−current applications.

Output Capacitor

An output capacitor should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUT} below GND when the switch is on. This capacitor also prevents reverse inrush current from creating a voltage spike that could damage the device in the case of a V_{OUT} short.

Fault Reporting

Upon the detection of an over−current, OC_FLAGB signal the fault by activating LOW.

Current Limiting

The current limit ensures that the current through the switch does not exceed the maximum set value, while not limiting the minimum value. The current at which the part's limit is adjustable through the selection of the external resistor connected to the ISET pin. Information for selecting the resistor is found in the section below. The device acts as a constant−current source when the load draws more than the maximum value set by the device until thermal shutdown occurs. The device recovers if the die temperature drops below the threshold temperature.

Under−Voltage Lockout (UVLO)

The under−voltage lockout turns the switch off if the input voltage drops below the lockout threshold. With the ON pin active, the input voltage rising above the UVLO threshold releases the lockout and enables the switch.

Reverse−Current Blocking

The reverse−current blocking feature protects the input source against current flow from output to input when the load switch is off.

Thermal Shutdown

The thermal shutdown protects the die from internally or externally generated excessive temperature. During an over−temperature condition, the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

Setting Current Limit

The current limit is set with an external resistor connected between the I_{SET} and GND pins. The resistor is selected using Table 1. Resistor tolerance of 1% or less is recommended.

Table 1. CURRENT LIMIT SETTINGS BY RSET (Note10)

$R_{SET}\Omega$	Min. Current Limit (mA)	Typ. Current Limit (mA)	Max. Current Limit (mA)
420	2250	2500	2750
469	2025	2250	2475
528	1800	2000	2200
604	1570	1750	1920
680	1350	1500	1650
866	1125	1250	1375
1070	900	1000	1100
1200	810	900	990
1330	720	800	880
1500	630	700	770
1740	540	600	660
2100	450	500	550
2320	405	450	495
2550	360	400	440
2940	315	350	385
3400	270	300	330
4020	225	250	275
4990	180	200	220
6490	135	150	165
9530	90	100	110
20000	42	50	58

10. Table values based on 1% tolerance resistor.
11. For 50 mA setting, tolerance is ±15% with 1%.

If current limit is not used it is OK for the I_{SET} pin to be connected with GND, but the maximum current must be less than the maximum current capability of 2.8 A.

BOARD LAYOUT

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance may have on normal and short−circuit operation. Using wide traces for VIN, VOUT, GND helps minimize parasitic electrical effects along with minimizing the case−to−ambient thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C

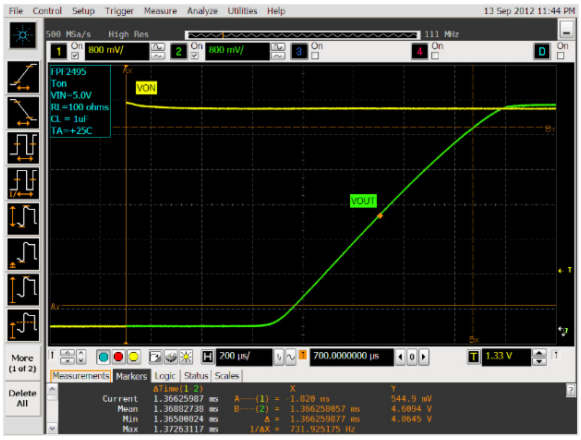


Figure 1. t_{ON} Response

Figure 2. OVP Response (Increase V_{OUT} to OVP Trip Point)

Figure 3. OC_FLAGB Response Time (Toggle R_{LOAD} from High to Low Resistance)

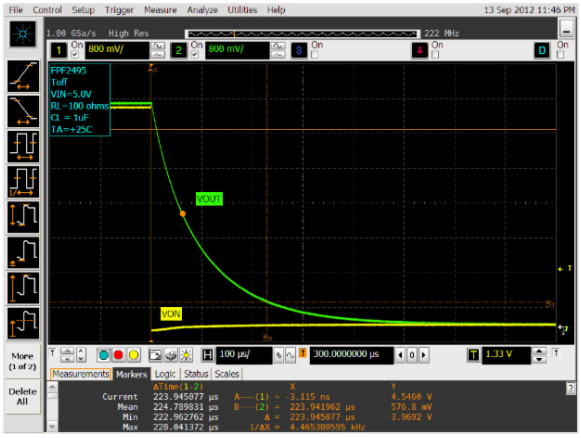


Figure 4. t_{OFF} Response

Figure 5. t_{OCP} Response Time

PRODUCT−SPECIFIC DIMENSIONS

Parts	D	E	X	Y
FPF2495BUCX	1220 μm ±30 μm	1220 μm ±30 μm	210 μm	210 μm

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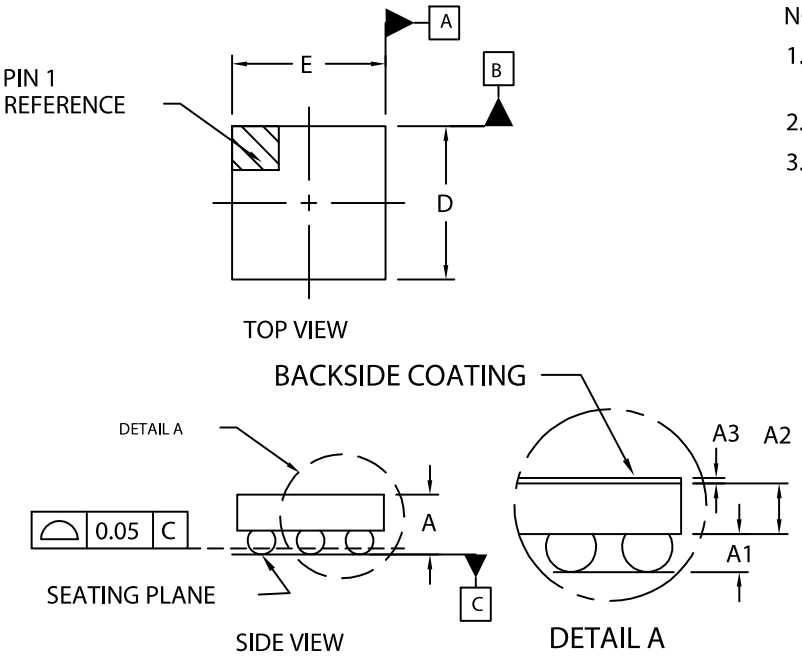
CASE 567SU
ISSUE A

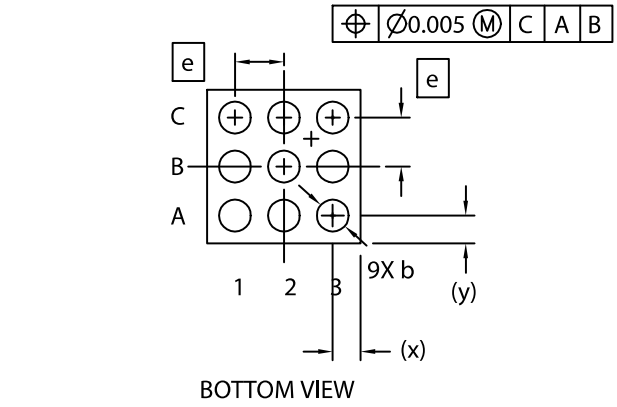
DATE 22 APR 2020

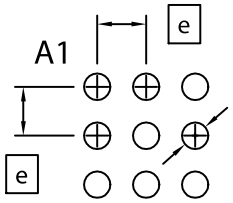


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.543	0.581	0.619
A1	0.183	0.203	0.223
A2	0.338	0.353	0.368
A3	0.022	0.025	0.028
b	0.240	0.260	0.280
D	1.19	1.22	1.25
E	1.19	1.22	1.25
e	0.40 BSC		
x	0.195	0.210	0.225
y	0.195	0.210	0.225





Ø0.215 COPPER PAD (BOTTOM)

RECOMMENDED MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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