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**ON Semiconductor®**

Si4542DY

30V Complementary PowerTrench® MOSFET

General Description

This complementary MOSFET device is produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

• DC/DC converter

• Power management

### Features

• **Q1**: **N-Channel**

  6 A, 30 V $R_{DS(on)} = 28$ mΩ @ $V_{GS} = 10V$

  $R_{DS(on)} = 35$ mΩ @ $V_{GS} = 4.5V$

• **Q2**: **P-Channel**

  −6 A, −30 V $R_{DS(on)} = 32$ mΩ @ $V_{GS} = -10V$

  $R_{DS(on)} = 45$ mΩ @ $V_{GS} = -4.5V$

SO-8

Pin 1
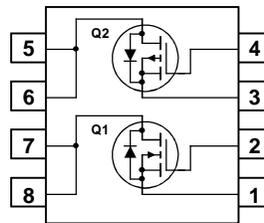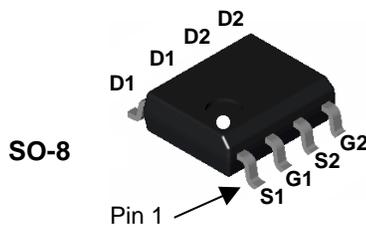
Absolute Maximum Ratings $T_A = 25°C$ unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		30	−30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	6	−6	A
	- Pulsed		20	−20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1.2		
		(Note 1c)	1		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +175		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
4542	Si4542DY	13"	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV$_{DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = −250 µA	Q1 Q2	30 −30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = −250 µA, Referenced to 25°C	Q1 Q2		23 −21		mV/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = −24 V, V_{GS} = 0 V	Q1 Q2			1 −1	µA
I$_{GSS}$	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±20 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
V$_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = −250 µA	Q1 Q2	1 −1	1.5 −1.7	3 −3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = −250 µA, Referenced to 25°C	Q1 Q2		−4 4		mV/°C
R$_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 10 V, I_D = 6 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 5 A	Q1		19 32 25	28 48 35	mΩ
		V_{GS} = −10 V, I_D = −6 A V_{GS} = −10 V, I_D = −6 A, T_J = 125°C V_{GS} = −4.5 V, I_D = −5 A	Q2		21 29 30	32 51 45	
I$_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V V_{GS} = −10 V, V_{DS} = −5 V	Q1 Q2	20 −20			A
g$_{FS}$	Forward Transconductance	V_{DS} = 15 V, I_D = 6 A V_{DS} = −10 V, I_D = −6 A	Q1 Q2		18 16		S
Dynamic Characteristics							
C$_{iss}$	Input Capacitance	Q1 V_{DS} = 15 V, V_{GS} = 0 V,	Q1 Q2		830 1540		pF
C$_{oss}$	Output Capacitance	f = 1.0 MHz Q2	Q1 Q2		185 400		pF
C$_{rss}$	Reverse Transfer Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		80 170		pF

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
t$_{d(on)}$	Turn-On Delay Time	Q1 V_{DS} = 15 V, I_D = 1 A,	Q1 Q2		6 13	12 24	ns
t$_r$	Turn-On Rise Time	V_{GS} = 10V, R_{GEN} = 6 Ω	Q1 Q2		10 22	18 35	ns
t$_{d(off)}$	Turn-Off Delay Time	Q2 V_{DS} = −15 V, I_D = −1 A,	Q1 Q2		18 47	29 75	ns
t$_f$	Turn-Off Fall Time	V_{GS} = −10 V, R_{GEN} = 6 Ω	Q1 Q2		5 18	12 30	ns
Q$_g$	Total Gate Charge	Q1 V_{DS} = 15 V, I_D = 7.5 A, V_{GS} = 5 V	Q1 Q2		9 15	13 20	nC
Q$_{gs}$	Gate-Source Charge	Q2	Q1 Q2		2.8 4		nC
Q$_{gd}$	Gate-Drain Charge	V_{DS} = −10 V, I_D = −6 A, V_{GS} = −5V	Q1 Q2		3.1 5		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1			1.3	A
			Q2			−1.3	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)	Q1		0.7	1.2	V
		$V_{GS} = 0$ V, $I_S = -1.3$ A (Note 2)	Q2		−0.7	−1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper
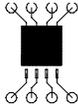
b) 125°C/W when mounted on a .02 in^2 pad of 2 oz copper
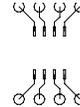
c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

PUBLICATION ORDERING INFORMATION

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