35 GHz to 70 GHz, GaAs, pHEMT, MMIC, Medium Power Amplifier

Data Sheet **HMC1144**

FEATURES

Output power for 1 dB compression (P1dB): 21 dBm typical
Saturated output power (P_{SAT}): 22 dBm typical
Gain: 19 dB typical
Output third-order intercept (IP3): 28 dBm typical
Supply voltage: 4 V at 320 mA
50 Ω matched input/output
Die size: 2.3 mm × 1.8 mm × 0.05 mm

APPLICATIONS

Test instrumentation
Microwave radios and very small aperture terminals (VSATs)
Military and space
Telecommunications infrastructure
Fiber optics

FUNCTIONAL BLOCK DIAGRAM

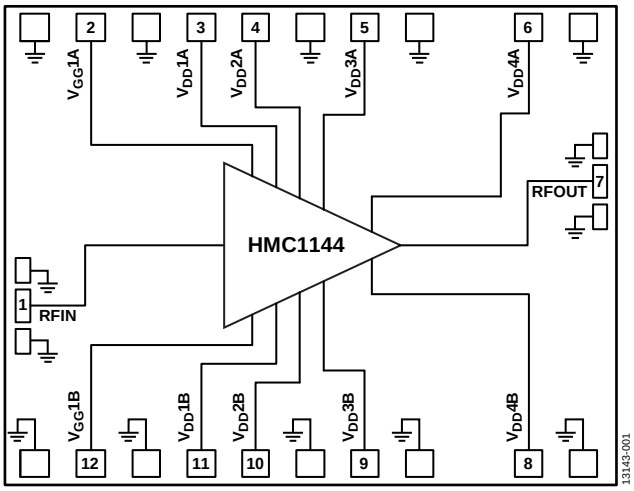

Figure 1.

GENERAL DESCRIPTION

The HMC1144 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 35 GHz to 70 GHz. In the lower band of 35 GHz to 50 GHz, the HMC1144 provides 19 dB (typical) of gain, 28 dBm output IP3, and 19 dBm and 19.5 dBm, respectively, of output P1dB gain compression. In the upper band of 50 GHz to 70 GHz, the HMC1144 provides 19 dB (typical) of gain, 32 dBm output IP3, and 21 dBm of output power at 1 dB gain compression. The HMC1144 requires 320 mA from a 4 V supply. The HMC1144 amplifier inputs/outputs are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of 0.076 mm (3 mil) minimal length.

Rev. C **Document Feedback**

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Added Figure 28; Renumbered Sequentially ... 10
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10/2016—Rev. A to Rev. B

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1/2016—Rev. 0 to Rev. A

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Added Figure 28 to Figure 32; Renumbered Sequentially ... 8

10/2015—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

35 GHz TO 40 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD}1A = V_{DD}2A = V_{DD}3A = V_{DD}4A = 4 V, I_{DD} = I_{DD}1A + I_{DD}2A + I_{DD}3A + I_{DD}4A = 320 mA, unless otherwise stated. Adjust V_{GG}1B from −2 V to 0 V to achieve I_{DD} = 320 mA typical.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			35		40	GHz
GAIN				19		dB
Gain Variation Over Temperature				0.022		dB/°C
RETURN LOSS						
Input				33		dB
Output				16		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB			19		dBm
Saturated Output Power	P_{SAT}			21		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		28		dBm
SUPPLY CURRENT						
Total Supply Current	I_{DD}			320		mA
Total Supply Current vs. V_{DD}						
I_{DD} = 290 mA				4		V
I_{DD} = 320 mA				4		V
I_{DD} = 350 mA				4		V

40 GHz TO 50 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD}1A = V_{DD}2A = V_{DD}3A = V_{DD}4A = 4 V, I_{DD} = I_{DD}1A + I_{DD}2A + I_{DD}3A + I_{DD}4A = 320 mA, unless otherwise stated. Adjust V_{GG}1B from −2 V to 0 V to achieve I_{DD} = 320 mA typical.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			40		50	GHz
GAIN			17	19		dB
Gain Variation Over Temperature				0.023		dB/°C
RETURN LOSS						
Input				35		dB
Output				16		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		17	19.5		dBm
Saturated Output Power	P_{SAT}			21.5		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		28		dBm
SUPPLY CURRENT						
Total Supply Current	I_{DD}			320		mA
Total Supply Current vs. V_{DD}						
I_{DD} = 290 mA				4		V
I_{DD} = 320 mA				4		V
I_{DD} = 350 mA				4		V

50 GHz TO 70 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = V_{DD}1A = V_{DD}2A = V_{DD}3A = V_{DD}4A = 4 V, I_{DD} = I_{DD}1A + I_{DD}2A + I_{DD}3A + I_{DD}4A = 320 mA, unless otherwise stated. Adjust V_{GG}1B from −2 V to 0 V to achieve I_{DD} = 320 mA typical.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			50		70	GHz
GAIN			17	19		dB
Gain Variation Over Temperature				0.016		dB/°C
RETURN LOSS						
Input				22		dB
Output				25		dB
OUTPUT						
Output Power for 1 dB Compression	P1dB		19	21		dBm
Saturated Output Power	P_{SAT}			22		dBm
Output Third-Order Intercept	IP3	Measurement taken at P_{OUT}/tone = 10 dBm		32		dBm
SUPPLY CURRENT						
Total Supply Current	I_{DD}			320		mA
Total Supply Current vs. V_{DD}						
I_{DD} = 290 mA				4		V
I_{DD} = 320 mA				4		V
I_{DD} = 350 mA				4		V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD}1A to V_{DD}4A)	4.5 V
Gate Bias Voltage (V_{GG}1B)	−2 V to 0 V dc
RF Input Power (RFIN)	22 dBm
Channel Temperature	175°C
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 19.2 mW/°C Above 85°C)	1.770 W
Thermal Resistance, θ_{JA} (Channel to Bottom Die)	50.83°C/W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	±125 V, Class 0B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

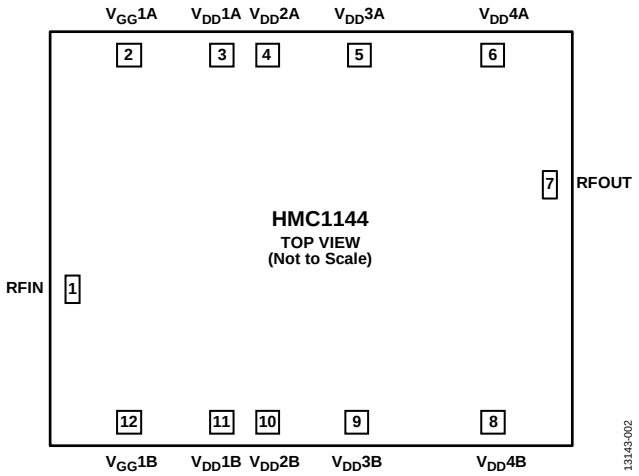

Figure 2. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RFIN	RF Input. This pad is ac-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
2	V_{GG}1A	Gate Control Pad for Alternate Bias Configuration. See Figure 4 for the interface schematic..
3 to 6	V_{DD}1A to V_{DD}4A	Drain Bias Voltage Pads for the Amplifier. External bypass capacitors of 100 pF and 0.1 µF are required. See Figure 5 for the interface schematic.
7	RFOUT	RF Output. This pad is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
8 to 11	V_{DD}4B to V_{DD}1B	Drain Bias Voltage Pads for Alternate Bias Configuration. External bypass capacitors of 100 pF and 0.1 µF are required for decoupling. See Figure 7 for the interface schematic.
12	V_{GG}1B	Gate Control Pad for the Amplifier. External bypass capacitors of 100 pF and 0.1 µF are required. See Figure 8 for the interface schematic.
Die Bottom	GND	Die bottom must be connected to RF/dc ground. See Figure 9 for the interface schematic.

INTERFACE SCHEMATICS

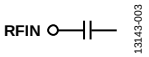

Figure 3. RFIN Interface Schematic

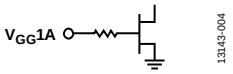

Figure 4. V_{GG}1A Interface Schematic

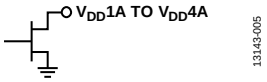

Figure 5. V_{DD}1A to V_{DD}4A Interface Schematic

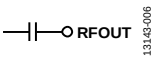

Figure 6. RFOUT Interface Schematic

Figure 7. V_{DD}1B to V_{DD}4B Interface Schematic

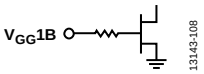

Figure 8. V_{GG}1B Interface Schematic

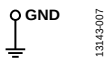

Figure 9. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

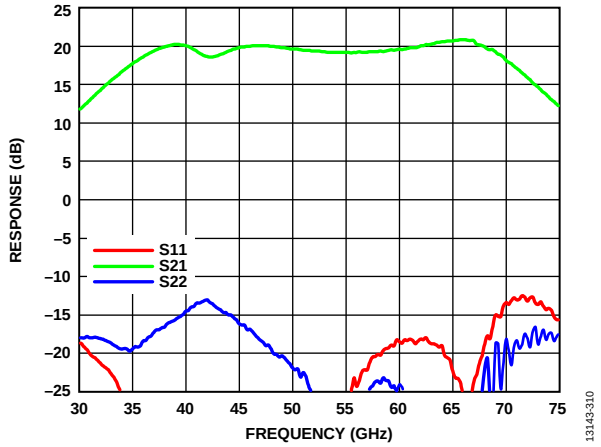

Figure 10. Response Gain and Return Loss vs. Frequency

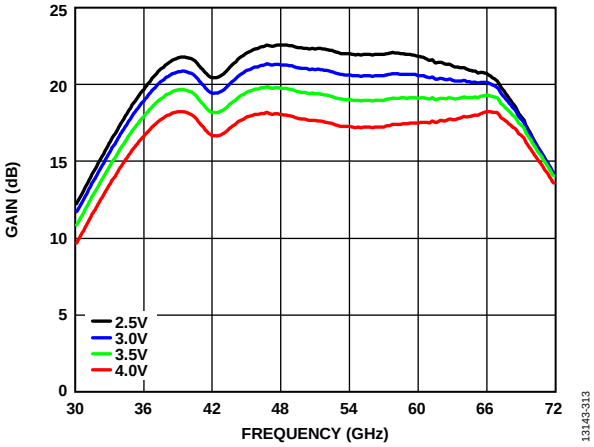

Figure 13. Gain vs. Frequency for Various V_{DD} at I_{DD} = 250 mA

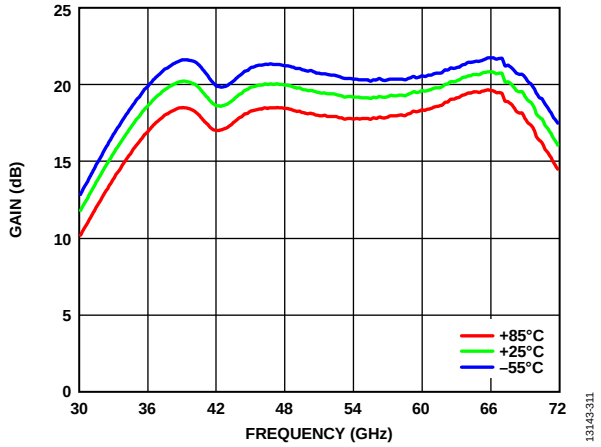

Figure 11. Gain vs. Frequency at Various Temperatures

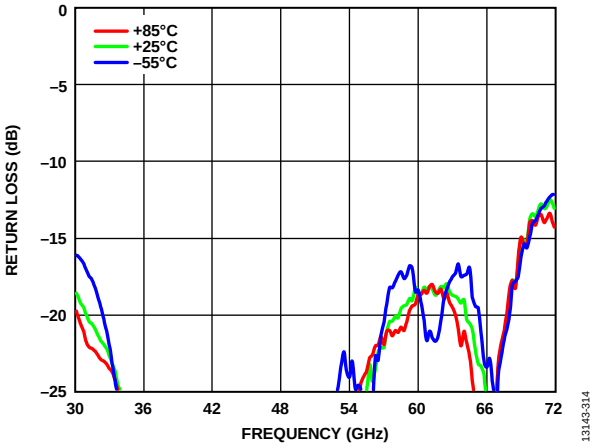

Figure 14. Input Return Loss vs. Frequency at Various Temperatures

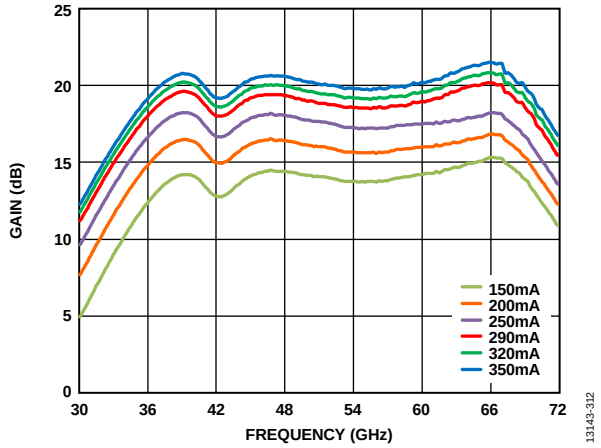

Figure 12. Gain vs. Frequency for Various I_{DD} at V_{DD} = 4 V

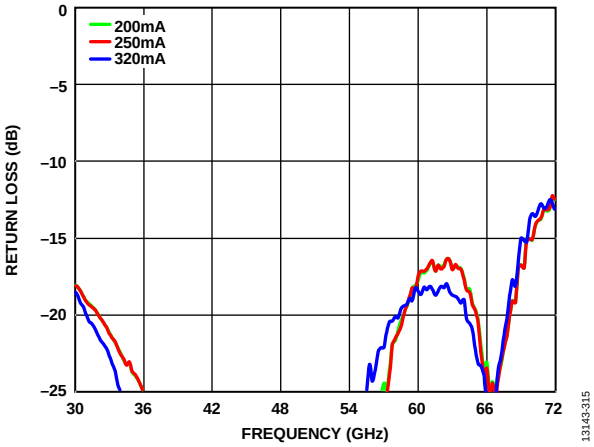

Figure 15. Input Return Loss vs. Frequency for Various I_{DD} at V_{DD} = 4 V

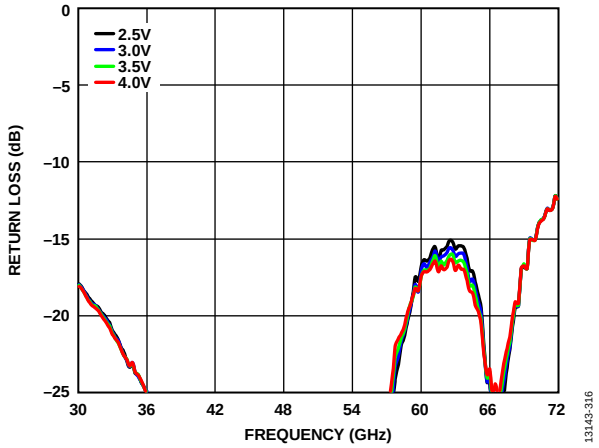

Figure 16. Input Return Loss vs. Frequency for Various V_{DD} at I_{DD} = 250 mA

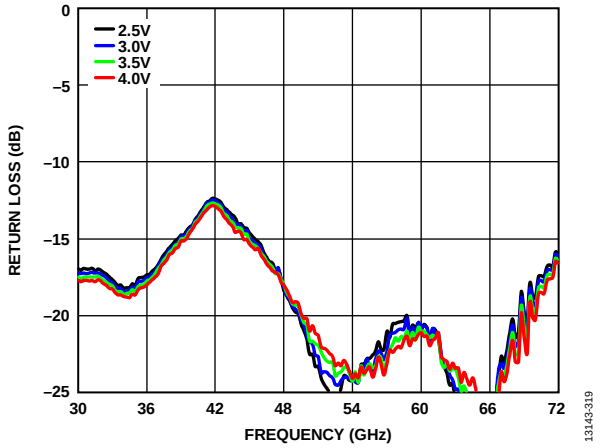

Figure 19. Output Return Loss vs. Frequency for Various V_{DD} at I_{DD} = 250 mA

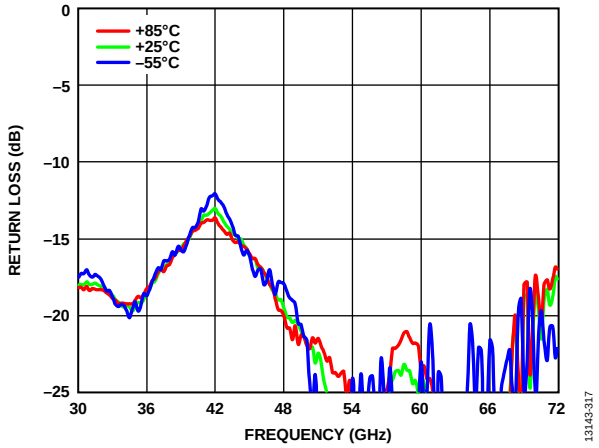

Figure 17. Output Return Loss vs. Frequency at Various Temperatures

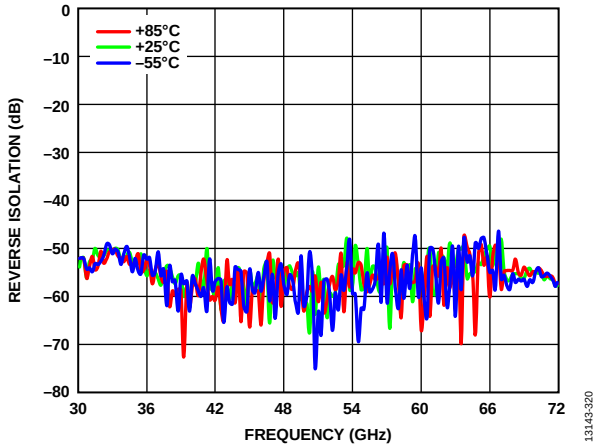

Figure 20. Reverse Isolation vs. Frequency at Various Temperatures

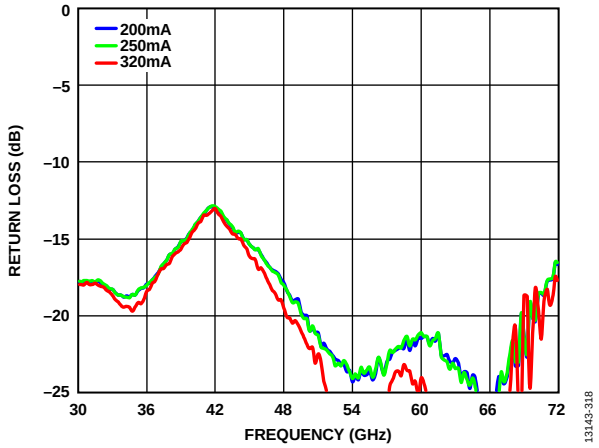

Figure 18. Output Return Loss vs. Frequency for Various I_{DD} at V_{DD} = 4 V

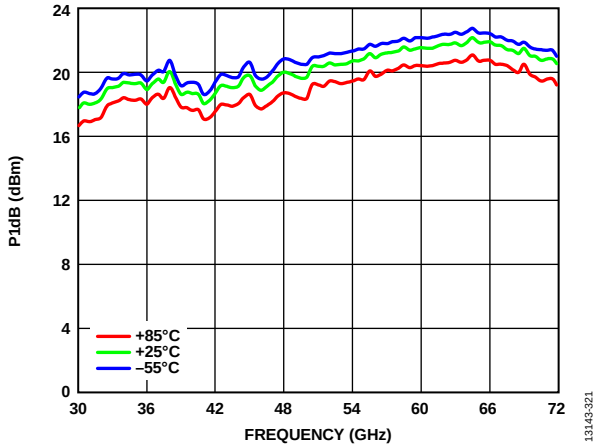

Figure 21. P1dB vs. Frequency at Various Temperatures

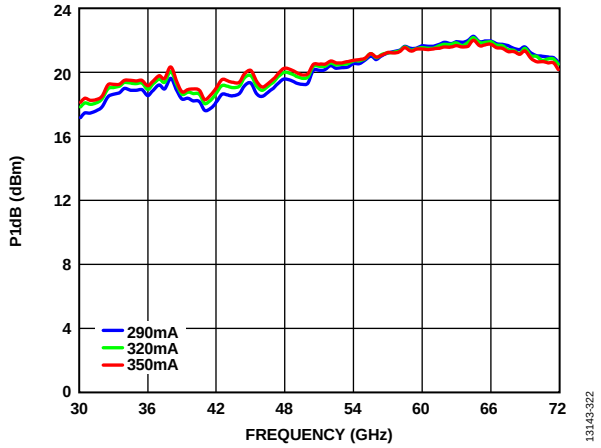

Figure 22. P1dB vs. Frequency for Various I_{DD} at V_{DD} = 4 V

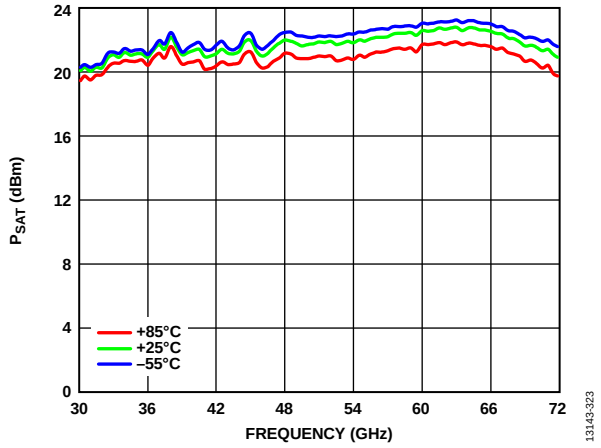

Figure 23. P_{SAT} vs. Frequency at Various Temperatures

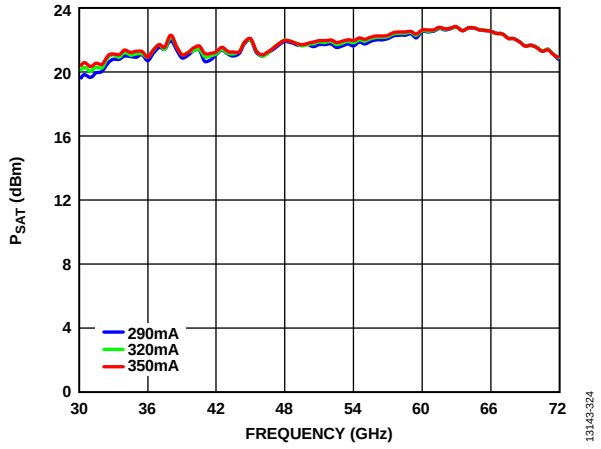

Figure 24. P_{SAT} vs. Frequency for Various I_{DD} at V_{DD} = 4 V

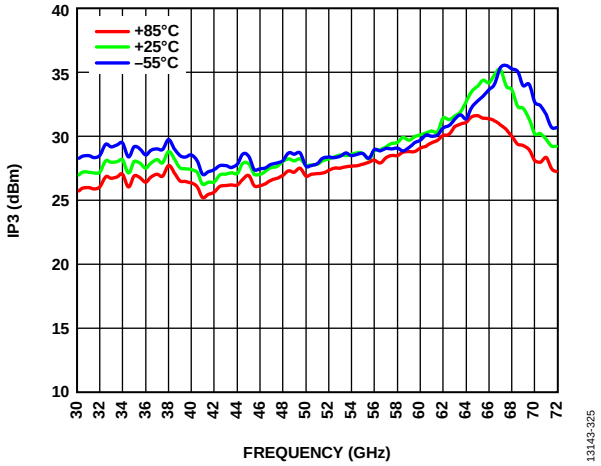

Figure 25. Output IP3 vs. Frequency for Various Temperatures at P_{OUT} = 10 dBm/Tone

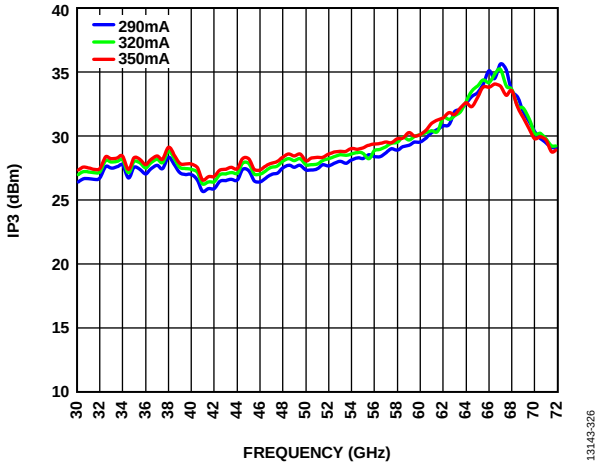

Figure 26. Output IP3 vs. Frequency for Various I_{DD} at P_{OUT} = 10 dBm/tone

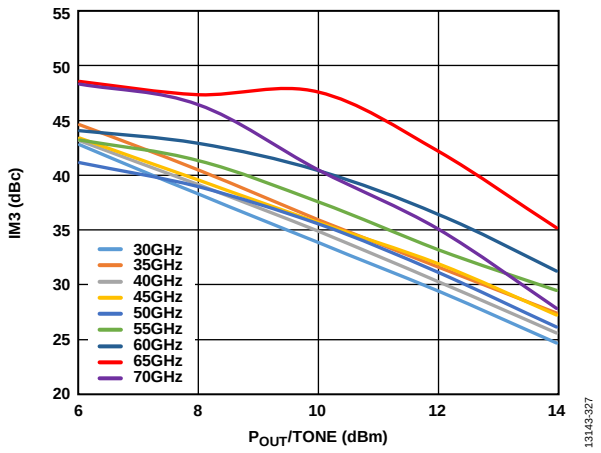

Figure 27. Output Third-Order Intermodulation (IMD3) vs. P_{OUT}/Tone for Various Frequencies at V_{DD} = 4 V, I_{DD} = 320 mA

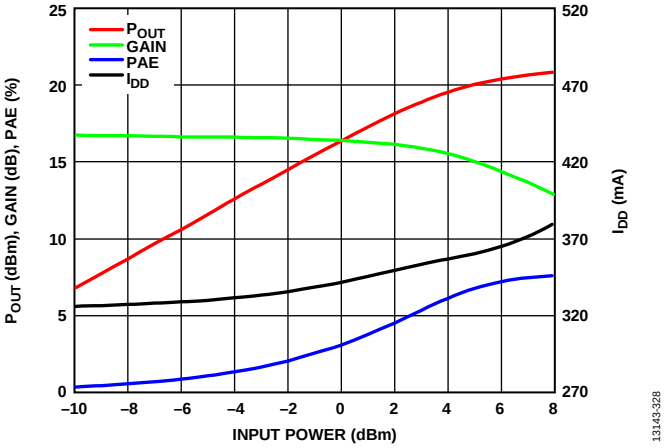

Figure 28. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 35 GHz

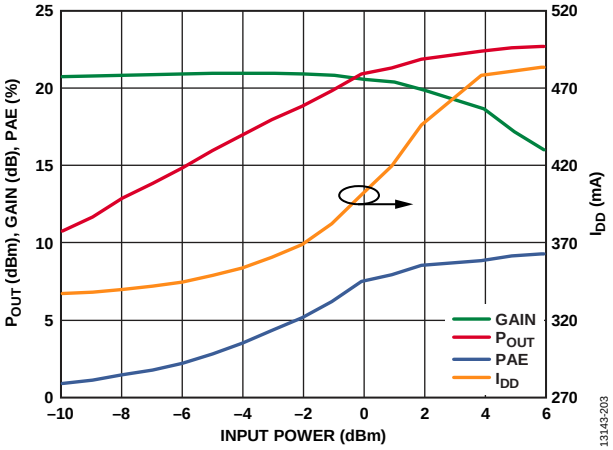

Figure 31. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 65 GHz

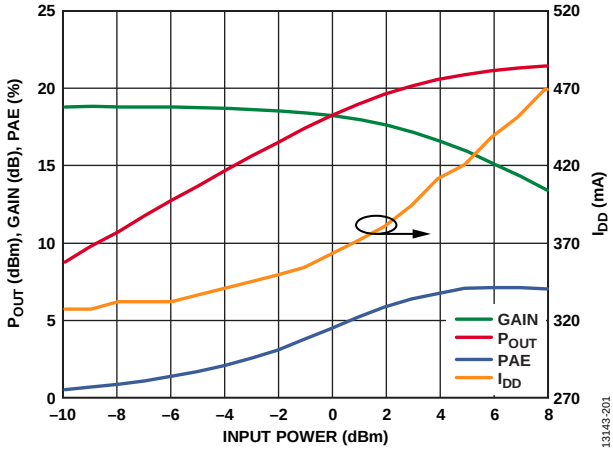

Figure 29. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 45 GHz

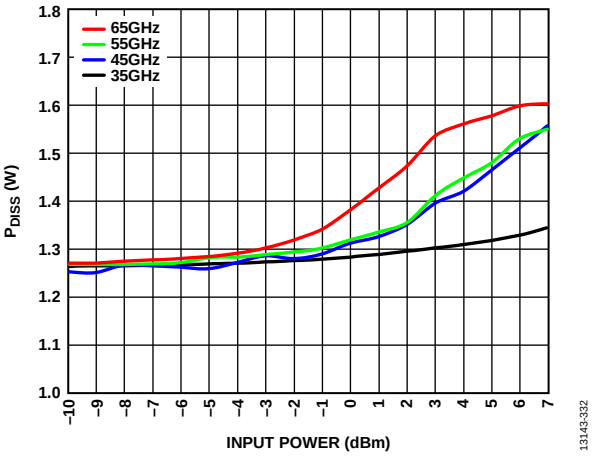

Figure 32. Power Dissipation (P_{DISS}) vs. Input Power at 85°C for Various Frequencies

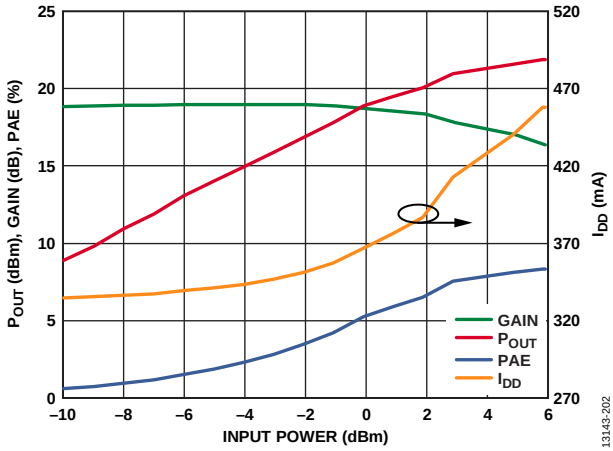

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 55 GHz

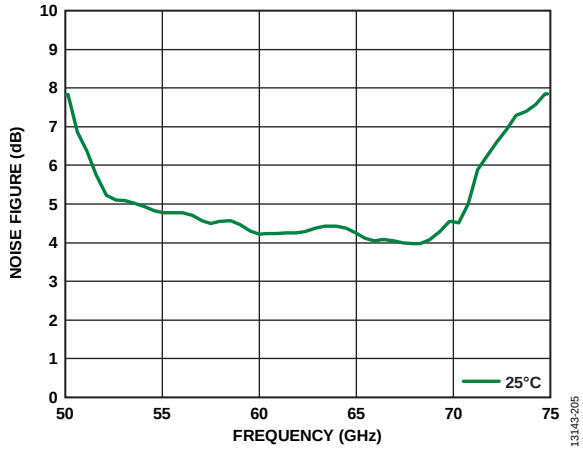

Figure 33. Noise Figure vs. Frequency at 25°C

THEORY OF OPERATION

The architecture of the HMC1144 power amplifier is shown in Figure 34. The HMC1144 uses two cascaded, four-stage amplifiers operating in quadrature between two 90° hybrids. This balanced amplifier approach forms an amplifier with a combined gain of 19 dB and a saturated output power (P_{SAT}) of 22 dBm. The 90° hybrids ensure that the input and output return losses are greater than 15 dB. See the application circuits shown in Figure 38 and Figure 39 for further details on biasing the various blocks.

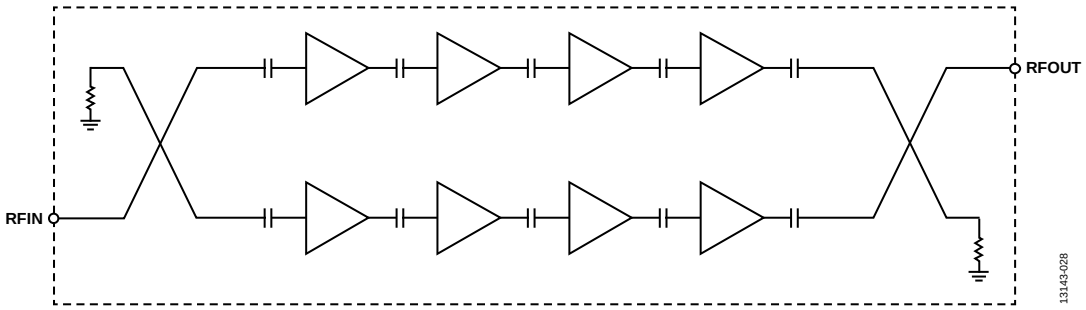

Figure 34. HMC1144 Architecture

APPLICATIONS INFORMATION

The HMC1144 is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for V_{DD}1A through V_{DD}4A and V_{DD}1B through V_{DD}4B (see Figure 38). V_{GG}1B is the gate bias pad for all four gain stages. Apply a gate bias voltage to V_{GG}1B and use capacitive bypassing as shown in Figure 38.

All measurements for this device were taken using the typical application circuit (see Figure 38) and configured as shown in the assembly diagram (see Figure 40).

The following is the recommended bias sequence during power-up:

1. Connect to ground.
2. Set the gate bias voltage to −2 V.
3. Set all the drain bias voltages, V_{DD} = 4 V.
4. Increase the gate bias voltage to achieve a quiescent current, I_{DD} = 320 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltage to −2 V to achieve I_{DD} = 0 mA (approximately).
3. Decrease all of the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

The V_{DD} = 4 V and I_{DD} = 320 mA bias conditions are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown was taken using the recommended bias condition. Operation of the HMC1144 at different bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section. Biasing the HMC1144 for higher drain current typically results in higher P1dB, output IP3, and gain, but at the expense of increased power consumption.

ALTERNATE BIASING CONFIGURATION

It is possible to bias the gate from the north (instead of the south) and bias the drain from the south (instead of the north). Although this alternate bias configuration was not measured during production testing and was evaluated minimally during product validation, it does offer flexibility in cases where it is more convenient to have the gate and drain bias approach the die from a different direction (see Figure 39).

In the alternate bias configuration, capacitive bypassing is required for the V_{GG}1A pad to which the bias voltage is applied, as well as for all eight V_{DD}xA/V_{DD}xB pads.

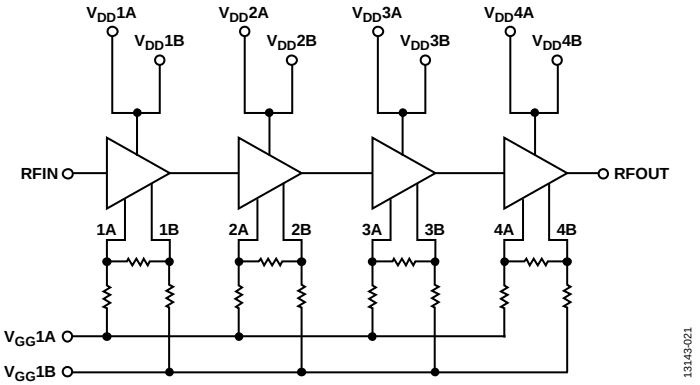

Figure 35. Simplified Block Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω, transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended for bringing the radio frequency to and from the chip (see Figure 36). When using 0.254 mm (10 mil) thick alumina, thin film substrates, raise the die 0.150 mm (6 mil) to ensure that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.05 mm (2 mil) thick die to a 0.150 mm (6 mil) thick, molybdenum (Mo) heat spreader (moly tab), which can then be attached to the ground plane (see Figure 37).

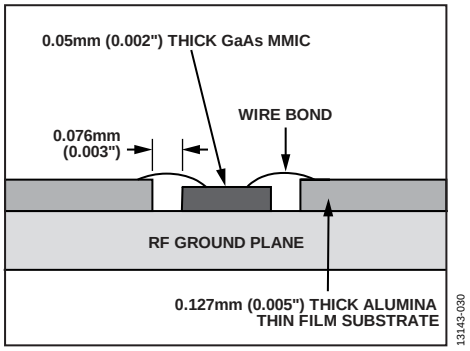

Figure 36. Routing RF Signals

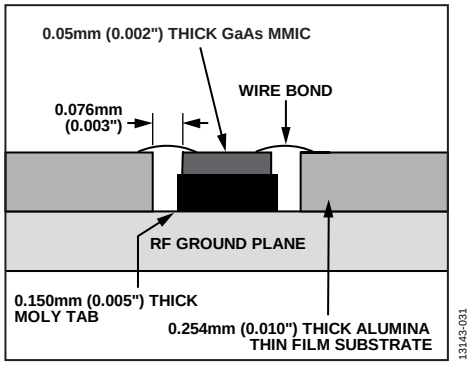

Figure 37. Routing RF Signals Using Moly Tab

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back metallized and can be die mounted with gold (Au) and tin (Sn) eutectic preforms or with electrically conductive epoxy. Ensure that the mounting surface is clean and flat.

When a eutectic die is attached, an 80% gold/20% tin preform is recommended with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, ensure that the tool tip temperature is 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. For attachment, no more than 3 sec of scrubbing is required.

When an epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. Ensure that these bonds are thermosonically bonded with a force of 40 *g* to 60 *g*. DC bonds of 0.001″ (0.025 mm) in diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 *g* to 50 *g* and wedge bonds with a force of 18 *g* to 22 *g*. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

TYPICAL APPLICATION CIRCUIT

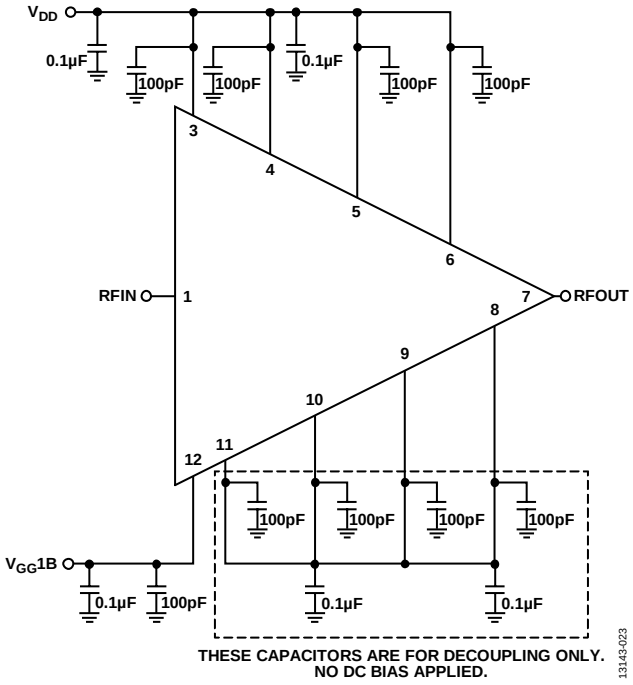

Figure 38. Typical Application Circuit

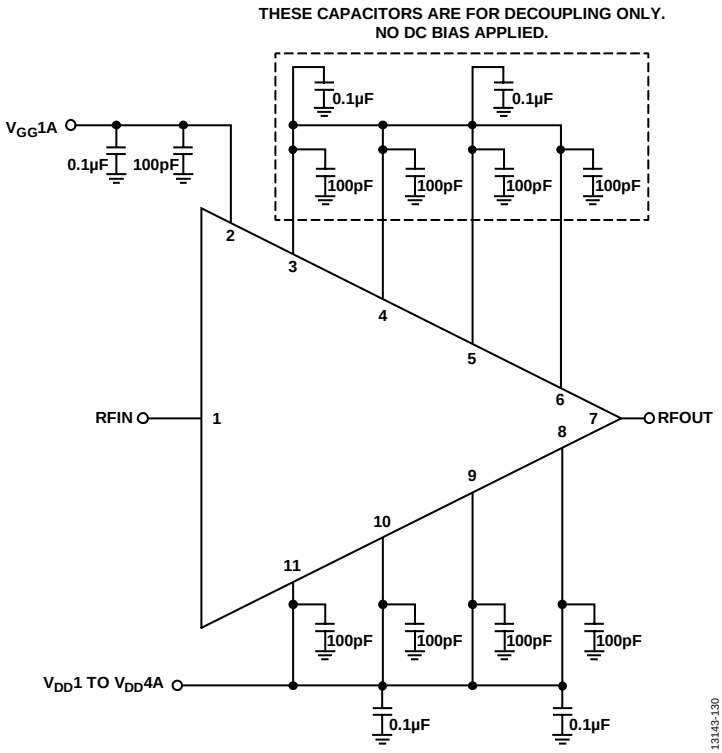

Figure 39. Alternate Bias Application Circuit

ASSEMBLY DIAGRAM

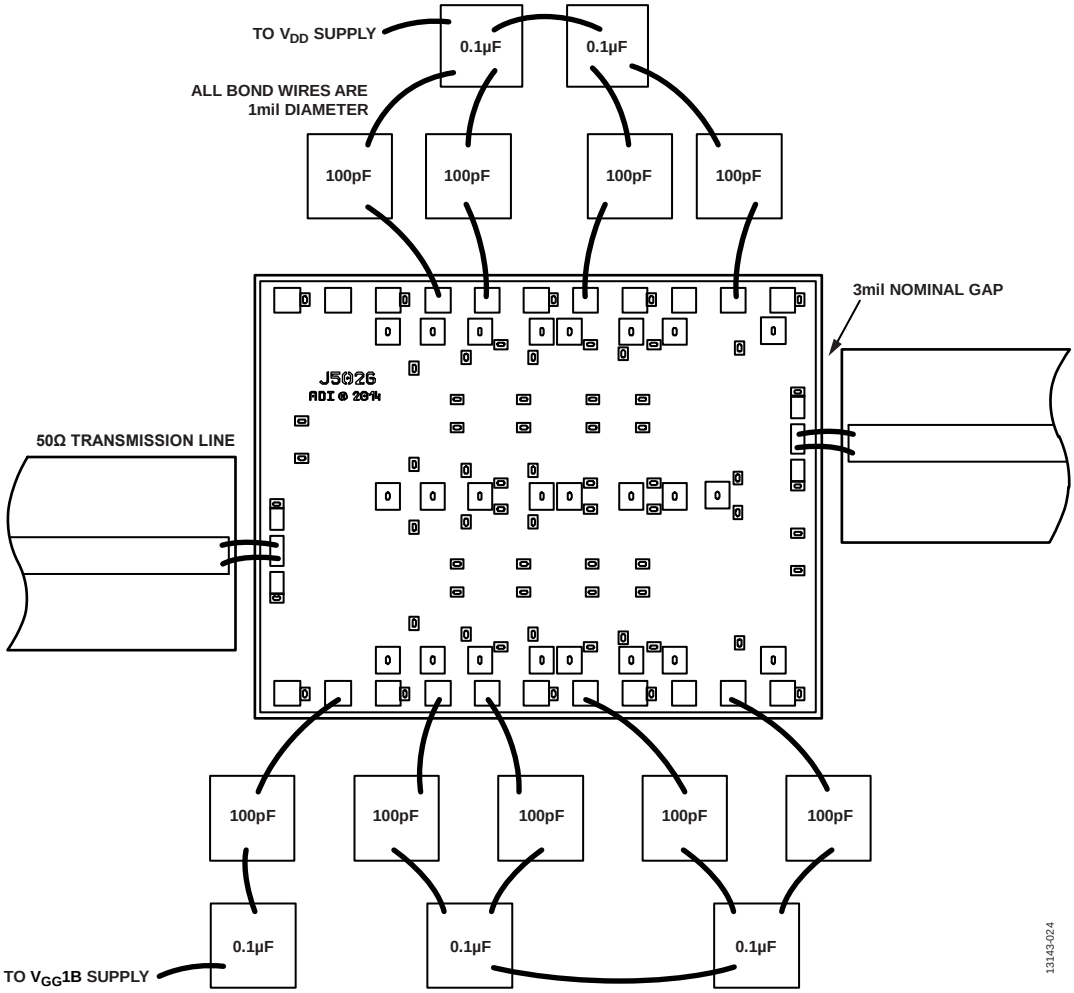

Figure 40. Assembly Diagram

OUTLINE DIMENSIONS

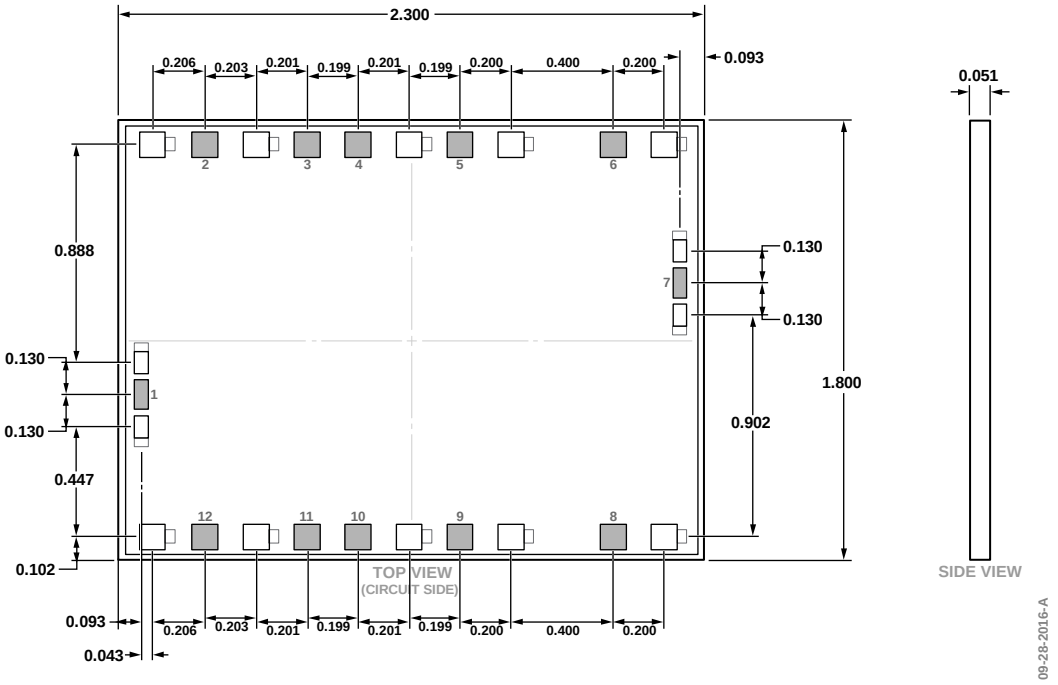

Figure 41. 12-Pad Bare Die [CHIP]
(C-12-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC1144	−55°C to +85°C	12-Pad Bare Die [CHIP]	C-12-2
HMC1144-SX	−55°C to +85°C	12-Pad Bare Die [CHIP]	C-12-2