

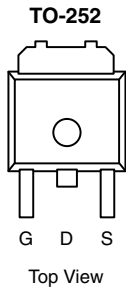


P-Channel 80-V (D-S) 175 °C MOSFET

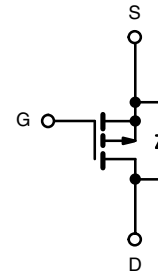
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
- 80	0.0252 at V _{GS} = - 10 V	- 50	55 nC
	0.029 at V _{GS} = - 4.5 V	- 47	

FEATURES

- TrenchFET[®] Power MOSFET



Drain Connected to Tab



P-Channel MOSFET

Ordering Information: SUD50P08-25L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 80	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	- 50 ^a	A	
	T _C = 70 °C	- 42.5 ^a		
	T _A = 25 °C	- 12.5 ^{b, c}		
	T _A = 70 °C	- 10.5 ^{b, c}		
Pulsed Drain Current	I _{DM}	- 40		
Continuous Source-Drain Diode Current	T _C = 25 °C	- 50 ^a		
	T _A = 25 °C	- 6.9 ^{b, c}		
Avalanche Current	L = 0.1 mH	I _{AS}	- 45	
Single-Pulse Avalanche Energy		E _{AS}	101	mJ
Maximum Power Dissipation	T _C = 25 °C	P _D	136	W
	T _C = 70 °C		95	
	T _A = 25 °C		8.3 ^{b, c}	
	T _A = 70 °C		5.8 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 sec	R _{thJA}	15	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	0.85	
			1.1	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 sec.
- Maximum under steady state conditions is 40 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 80			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		- 73		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$				A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -12.5\text{ A}$		0.021	0.0252	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -10.5\text{ A}$		0.024	0.029	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -12.5\text{ A}$		52		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4700		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			235		
Total Gate Charge	Q_g	$V_{DS} = -40\text{ V}, V_{GS} = -10\text{ V}, I_D = -12.5\text{ A}$		105	160	nC
				55	85	
Gate-Source Charge	Q_{gs}	$V_{DS} = -40\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -12.5\text{ A}$		16		
Gate-Drain Charge	Q_{gd}			26		
Gate Resistance	R_g	$f = 1\text{ MHz}$		4		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 3.8\text{ }\Omega$ $I_D \cong -10.5\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		45	70	ns
Rise Time	t_r			220	330	
Turn-Off Delay Time	$t_{d(off)}$			95	145	
Fall Time	t_f			110	165	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -40\text{ V}, R_L = 3.8\text{ }\Omega$ $I_D \cong -10.5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			105	160	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 50	A
Pulse Diode Forward Current ^a	I_{SM}				- 40	
Body Diode Voltage	V_{SD}	$I_S = -10.5\text{ A}$		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		55	85	ns
Body Diode Reverse Recovery Charge	Q_{rr}			110	165	nC
Reverse Recovery Fall Time	t_a			37		ns
Reverse Recovery Rise Time	t_b			18		

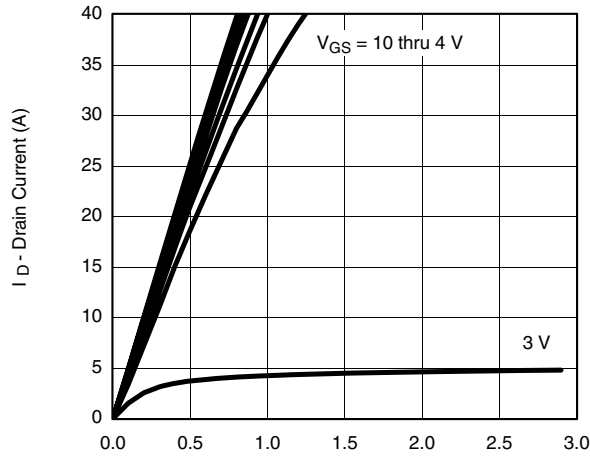
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

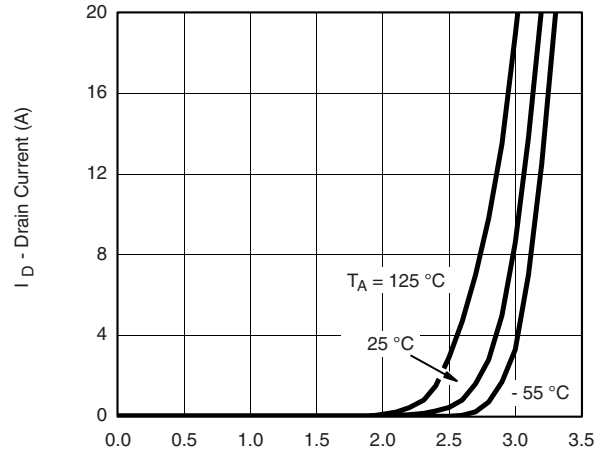
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



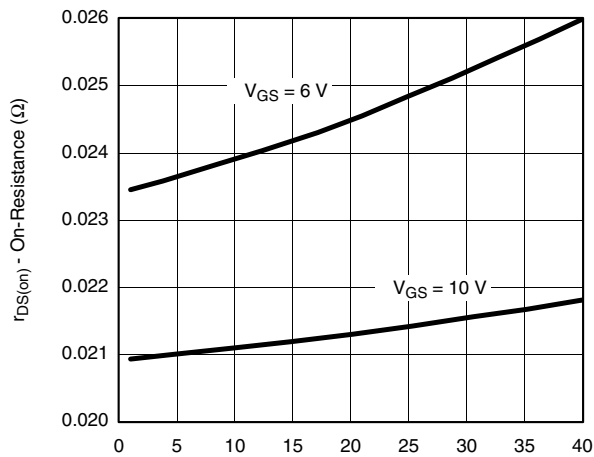
TYPICAL CHARACTERISTICS 25 °C unless noted



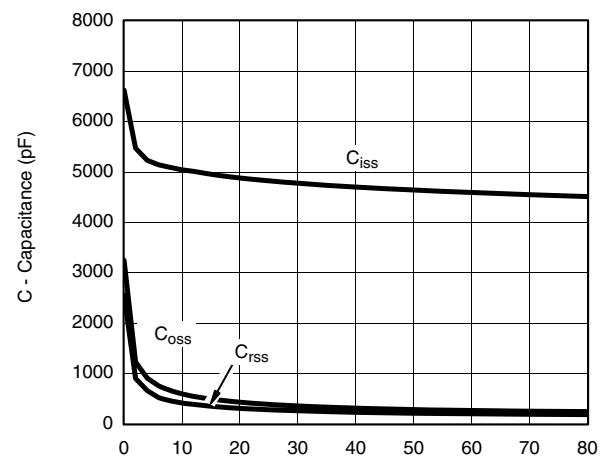
Output Characteristics



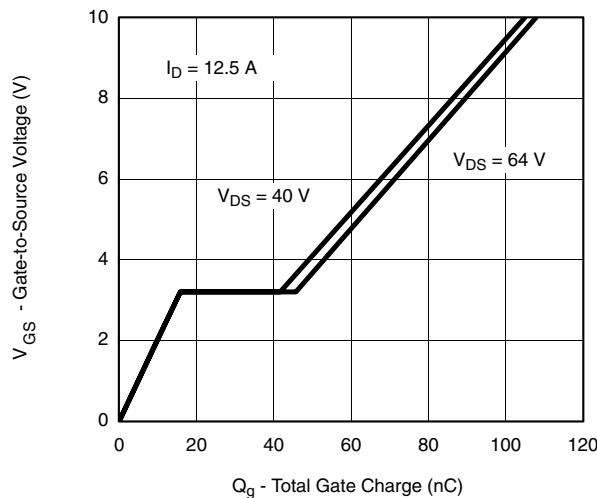
Transfer Characteristics



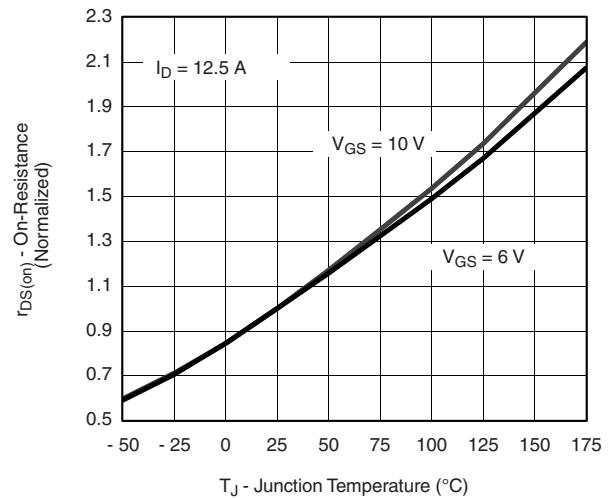
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



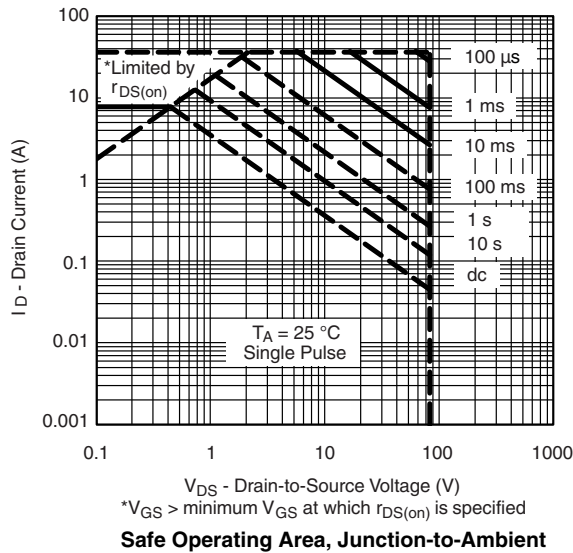
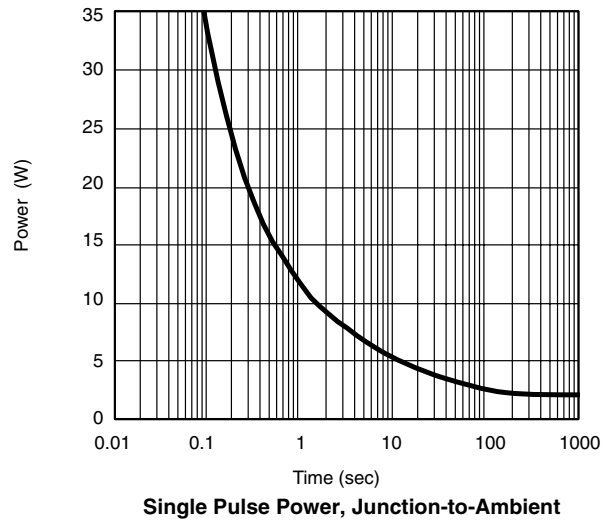
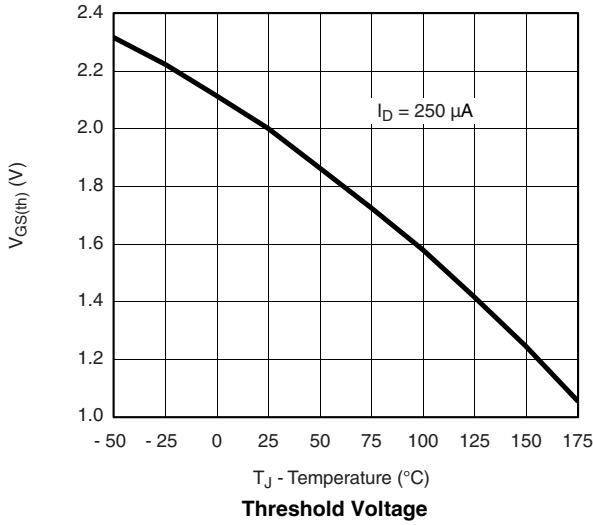
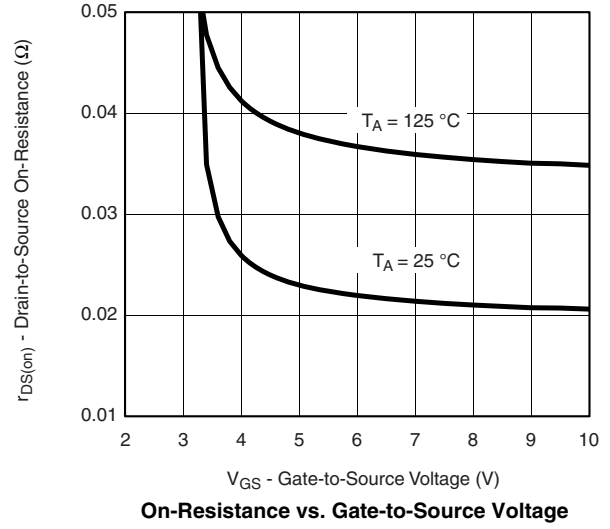
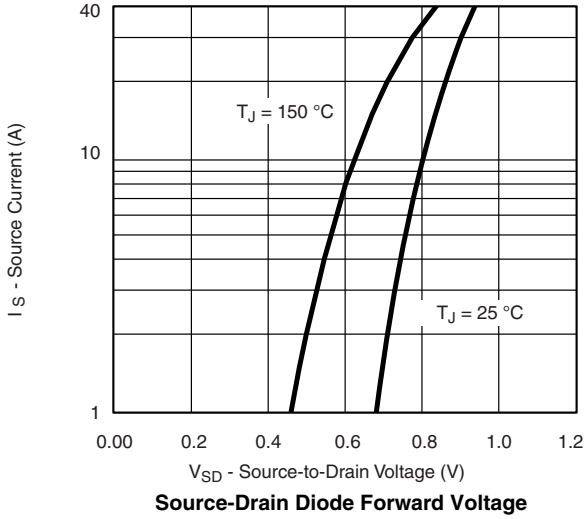
Gate Charge



On-Resistance vs. Junction Temperature

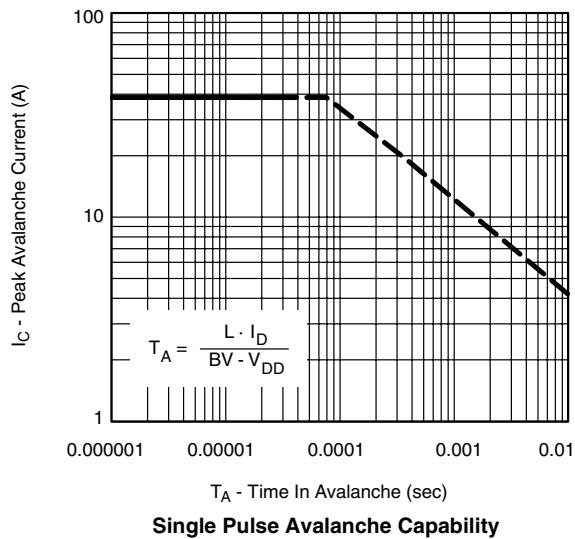
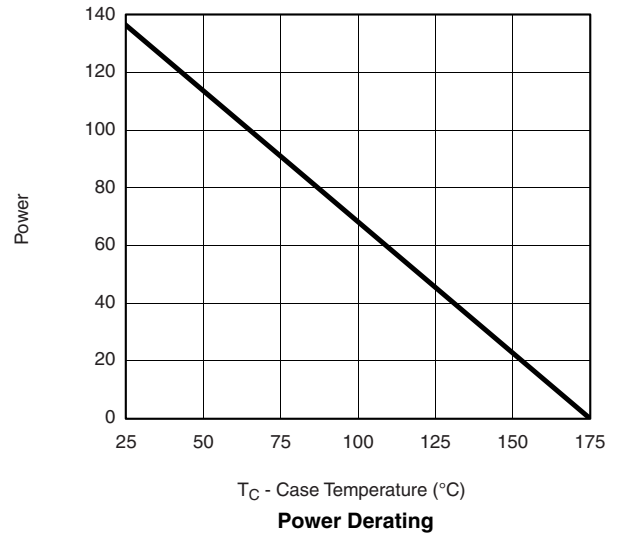
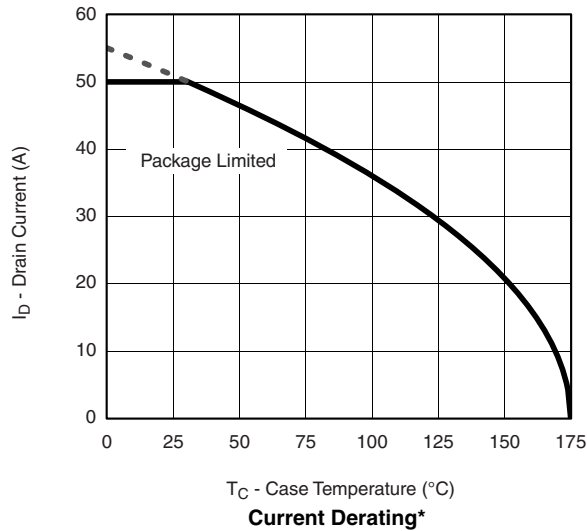


TYPICAL CHARACTERISTICS 25 °C unless noted





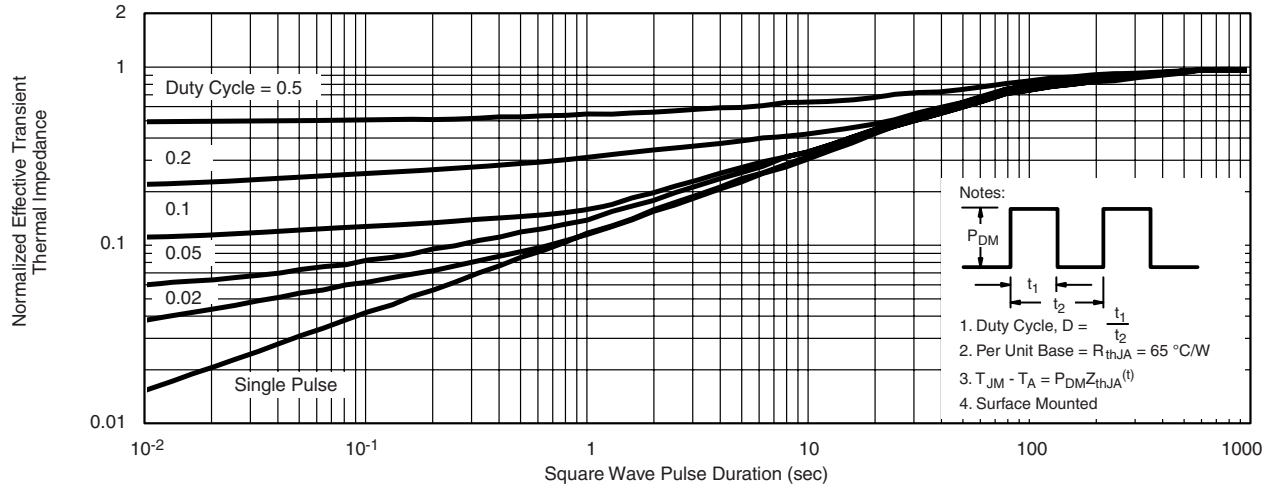
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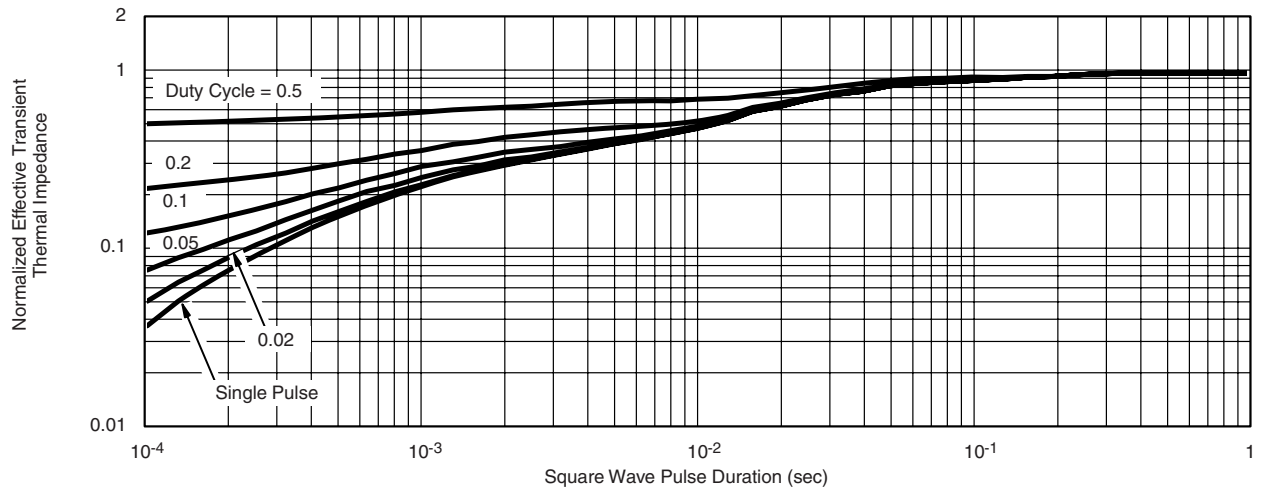
*The power dissipation P_D is based on $T_{J(max)} = 175\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C unless noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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