EFM32WG Errata

This document contains information on the EFM32WG errata. The latest available revision of this device is revision B.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: March 2021.

1. Errata Summary

The table below lists all known errata for the EFM32WG and all unresolved errata in revision B of the EFM32WG.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:	
			A	B
ADC_E118	Requirements for ADC_CLK > 7 MHz	Yes	X	X
BU_E105	LFXO Missing Cycles During IOVDD Ramping	Yes	X	X
CMU_E114	Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK	Yes	X	X
CMU_E115	HFRCO 1 MHz Band Switching	Yes	X	X
DAC_E109	DAC Output Drift Over Lifetime	Yes	X	X
DMA_E102	2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel	Yes	X	X
EMU_E107	Interrupts During EM2 Entry	Yes	X	X
EMU_E110	Potential Hard Fault when Exiting EM2 or EM3	Yes	X	—
LCD_E103	Indeterminate Animation Engine Start-Up	Yes	X	X
LCD_E104	Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO	Yes	X	X
LES_E104	LFPRESC Can Extend Channel Start-Up Delay	Yes	X	X
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	X	X
RMU_E101	POR Calibration Initialization Issue	Yes	X	—
RMU_E102	Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers	Yes	X	—
RMU_E103	Reset May Fail to Trigger During Supply Voltage Brownouts	Yes	X	—
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	No	X	X
USART_E113	IrDA Modulation and Transmission of PRS Input Data	Yes	X	X
USB_E103	HNP Sequence Fails if A-Device Connects After 3.4 ms	No	X	X
USB_E104	USB A-Device Delays the HNP Switch Back Process	No	X	X
USB_E105	B-Device as Host Driving K-J Pairs During Reset	No	X	X
USB_E109	Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1	Yes	X	X
USB_E110	Unexpected USB_HCx_INT.CHHLTD Interrupt	Yes	X	X

2. Current Errata Descriptions

2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

Description of Errata
If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification.
Affected Conditions / Impacts
Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits.
Workaround
For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements.
Resolution
There is currently no resolution for this issue.

2.2 BU_E105 — LFXO Missing Cycles During IOVDD Ramping

Description of Errata
LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.
Affected Conditions / Impacts
When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.
Workaround
Set PRESC in BURTC_CTRL to greater than 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
Resolution
There is currently no resolution for this issue.

2.3 CMU_E114 — Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK

Description of Errata
Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK.
Affected Conditions / Impacts
If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2.
Workaround
Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.
Resolution
There is currently no resolution for this issue.

2.4 CMU_E115 — HFRCO 1 MHz Band Switching

Description of Errata
Switching to or from the 1 MHz band of the HFRCO or AUXHFRCO may cause a hard fault even at the maximum supported number of wait states.
Affected Conditions / Impacts
When the HFRCO or AUXHFRCO is selected as a clock source (e.g., the HFRCO has been selected as the HFCLK source) and the device is running with the maximum supported number of wait states, switching to or from the 1 MHz band can possibly cause a clock glitch that results in unexpected behavior or a hard fault.
Workaround
Before switching to or from the 1 MHz band when the HFRCO or AUXHFRCO is selected as the clock source, first switch to another stable clock source (such as the LFRCO). For example, when switching from the 21 MHz band to the 1 MHz band, the following procedure needs to be followed: 1. Select another stable clock source by writing to the HFCLKSEL field of the CMU_CMD register. 2. Wait until the clock source shows that it has been selected in the CMU_STATUS register, (e.g., CMU_STATUS_LFRCOSEL = 1). 3. Program the CMU_HFRCOCTRL register to select the 1 MHz band and tuning value. 4. Wait until the HFRCO has stabilized at the new frequency by waiting for the HFRCORDY bit in the CMU_STATUS register to change for 0 to 1. 5. Select the HFRCO as the clock source by writing to the HFCLKSEL field of the CMU_CMD register.
Resolution
There is currently no resolution for this issue.

2.5 DAC_E109 — DAC Output Drift Over Lifetime

Description of Errata
The voltage output of the DAC might drift over time.
Affected Conditions / Impacts
When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.
Workaround
Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
Resolution
There is currently no resolution for this issue.

2.6 DMA_E102 — 2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel

Description of Errata
When performing a 2D copy (rectangular copy) on one DMA channel, more data than is specified is occasionally transferred from the source buffer if another channel is being used in ping-pong or scatter-gather mode.
Affected Conditions / Impacts
The incorrect number of bytes is transferred during the 2D copy when there is corruption caused by concurrent ping-pong or scatter-gather operation. This would be most noticeable when 2D copy is used for moving a graphic image to a display but could cause problems in other use cases.
Workaround
Do not allow ping-pong or scatter-gather mode DMA transfers to occur concurrently with a 2D copy. If both types operations are required, interleave them such that the 2D copy is complete before enabling a channel in ping-pong or scatter-gather mode or vice versa.
Resolution
There is currently no resolution for this issue.

2.7 EMU_E107 — Interrupts During EM2 Entry

Description of Errata
An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag.
Affected Conditions / Impacts
During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0.
Workaround
Before entering EM2, disable all high frequency peripheral interrupts in the core.
Resolution
There is currently no resolution for this issue.

2.8 LCD_E103 — Indeterminate Animation Engine Start-Up

Description of Errata
The LCD controller animation engine starts counting based on when the writes to LCD_AREGA and LCD_AREGB occur in relation to the clock for the animation frame counter. Because the animation engine cannot know when the writes occur, it is not possible to know whether the A or B register will shift first, which can result in one of the registers shifting twice before the other shifts once.
Affected Conditions / Impacts
Animations that require specific sequencing may not start in the correct state such that frames are not displayed in the correct order.
Workaround
If animation sequences must be seen in a specific order, consider handling this in software instead of using the animation engine. If the purpose of the animation is to denote ongoing activity, use segments that can be cycled in a generic fashion such that the output achieves the desired effect without depending on a specific frame order.
Resolution
There is currently no resolution for this issue.

2.9 LCD_E104 — Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO

Description of Errata
A leakage path to IOVDD exists when the LCD controller is configured to use the internally boosted or external power supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is due to PMOS transistors in the LCD pin logic having their source/bulk terminals connected to the highest VDD (thus the LCD power supply when external/boost mode is used) while their gates are connected to IOVDD.
Affected Conditions / Impacts
Use of LCD pins for GPIO results in increased current draw when the LCD controller is configured to use the internally boosted or external supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is particularly noticeable when the device is operating in EM2 as the LCD to IOVDD supply leakage can amount to tens of microamps. While the GPIO functionality of the LCD pins is not impaired, for certain applications, the increased current draw can be undesirable.
Workaround
Do not use LCD pins for GPIO functionality if the LCD controller is configured to use an external power supply or boost mode, and the resulting VLCD can be greater than the IOVDD supply.
Resolution
There is currently no resolution for this issue.

2.10 LES_E104 — LFPRESC Can Extend Channel Start-Up Delay

Description of Errata
Setting LESENSE_TIMCTRL_LFPRESC to a value other than DIV1 may delay channel start-up longer than the number of $LFACLK_{LESENSE}$ clock cycles specified by LESENSE_TIMCTRL_STARTDLY.
Affected Conditions / Impacts
Delaying channel start-up delays the subsequent excitation and measurement phases and may have an impact on the data returned by the LESENSE.
Workaround
If a channel start-up delay is used (LESENSE_TIMCTRL_STARTDLY > 0), LESENSE_TIMCTRL_LFPRESC must be set to DIV1.
Resolution
There is currently no resolution for this issue.

2.11 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.12 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e., ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

2.13 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

Description of Errata
If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled.
Affected Conditions / Impacts
It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0.
Workaround
Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data. If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART.
Resolution
There is currently no resolution for this issue.

2.14 USB_E103 — HNP Sequence Fails if A-Device Connects After 3.4 ms

Description of Errata
HNP Sequence fails if A-Device connects after 3.4 ms.
Affected Conditions / Impacts
The B-Device core only waits for up to 3.4 ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.15 USB_E104 — USB A-Device Delays the HNP Switch Back Process

Description of Errata
The D+ line disconnects after 200 ms, delaying the HNP switch back process.
Affected Conditions / Impacts
The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.16 USB_E105 — B-Device as Host Driving K-J Pairs During Reset

Description of Errata
The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode.
Affected Conditions / Impacts
If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.17 USB_E109 — Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1

Description of Errata
A Host-initiated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt.
Affected Conditions / Impacts
When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt.
Workaround
If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
Resolution
There is currently no resolution for this issue.

2.18 USB_E110 — Unexpected USB_HCx_INT.CHHLTD Interrupt

Description of Errata
In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set.
Affected Conditions / Impacts
In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR, USB_HCx_INT.DATATGLERR, or USB_HCx_INT.XFERCOMPL interrupts enabled.
Workaround
If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt.
Resolution
There is currently no resolution for this issue.

3. Resolved Errata Descriptions

This section contains previous errata for EFM32WG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 EMU_E110 — Potential Hard Fault when Exiting EM2 or EM3

Description of Errata
The flash is powered down in EM2 and EM3 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2 or EM3, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 or EM3 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2 or EM3, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 or EM3 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2017/05/09/emu_e110_-_potential-i2Pn
Resolution
This issue has been resolved. Devices with a date code greater than or equal to 1742 will not have this issue.

3.2 RMU_E101 — POR Calibration Initialization Issue

Description of Errata
Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.
Affected Conditions / Impacts
The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.
Workaround
Additional information including a software workaround is available from the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2015/10/09/rmu_e101_-_por_calib-cEpZ
Resolution
This issue has been resolved. Devices with a date code and PROD_REV greater than or equal to 1539 and 0x96 respectively will not have this issue.

3.3 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

Description of Errata
Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset.
Affected Conditions / Impacts
The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7
Workaround
Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again.
Resolution
This issue is resolved in revision B devices.

3.4 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

Description of Errata
Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range.
Affected Conditions / Impacts
If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL: https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD
Workaround
Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again.
Resolution
This issue is resolved in revision B devices.

4. Revision History

Revision 1.50

March, 2021
- Added CMU_E115

Revision 1.40

November, 2019
- Updated to product revision B.
- Added ADC_E118 and LES_E104.
- Resolved RMU_E102 and RMU_E103.
- Migrated to new errata document format.

Revision 1.30

January, 2019
- Added DMA_E102, LCD_E103, LCD_E104, RMU_E102, RMU_E103, and USART_E113.
- Resolved EMU_E110 and updated language to refer to both EM2 and EM3.
- RMU_E101 workaround URL updated.

Revision 1.20

April, 2017
- Added EMU_E110.
- Updated errata formatting.
- Merged all errata documents for EFM32WG devices into one document.
- Merged errata history and errata into one document.

Revision 1.10

October, 2015
- Added DAC_E109, EMU_E107, PCNT_E102, RMU_E101, and TIMER_E103.

Revision 1.00

October, 2014
- Initial release for EFM32WG360 and EFM32WG900 devices.

Revision 0.30

March, 2014
- Corrected typos in document.

Revision 0.20

August, 2013
- Added USB_E109 and USB_E110.
- Updated disclaimer, trademark and contact information.
- Updated errata naming convention.

Revision 0.10

April, 2013
- Initial preliminary release.

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