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APPLICATION NOTE 3915

DS26303 Short-Haul Line Interface Unit vs. LXT384

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Abstract: This document provides an explanation of the differences between the DS26303 and the LXT384 with emphasis on the information required to use the DS26303 in an existing LXT384 application. Descriptions of the feature differences, register considerations, and hardware considerations are provided.

Introduction

This document provides an explanation of the differences between the DS26303 and the LXT384 with emphasis on the information required to use the DS26303 in an existing LXT384 application. The DS26303 is an 8-channel short-haul line interface unit (LIU) that supports E1/T1/J1 from a single 3.3V power supply. This device supports the functions of the LXT384 without software modification while providing additional features made available using additional register banks. The DS26303 can be used in an existing LXT384 application without changing PCB layout, but by simply replacing external component values for the desired application.

Descriptions of the feature differences are provided in three separate sections. **Table 1** provides a list of DS26303 features not present in the LXT384. **Table 2** gives a list of LXT384 features not present in the DS26303. **Table 3** provides a list of features present in both the DS26303 and LXT384 that are not implemented the same on both devices.

The difference between registers of the DS26303 and LXT384 is described in **Tables 6** through **10**, along with the additional functionality provided by the expanded register set of the DS26303. **Figure 1** and **Table 11** provide the minor changes in component values required when using the DS26303 in an existing LXT384 application.

Table 1. DS26303 Features Not Present in LXT384

DS26303	LXT384
Programmable options to clear interrupt status on write or read. Clear on read is default.	Not supported.
Individual channel control for jitter attenuator: • Enable/disable • FIFO depth • FIFO limit trip	All channels have global control.

Internal software-selectable transmit and receive side termination for 100Ω T1 twisted-pair, 110Ω J1 twisted-pair, 120Ω E1 twisted–pair, and 75Ω E1 coaxial applications.	Not supported.
In HPS mode, the transmitter output and the internal impedance of the receiver can be turned off with only the OE pin.	Requires that both receivers use the same front-end termination.
Built-in BERT tester for diagnostics.	Not supported.
Individual channel control for: • Short-circuit protection • AIS enable on LOS • RCLK inversion • TCLK inversion	All channels have global control.
Individual channel-line violation detection.	Not supported.
Flexible MCLK See **Table 4** for available input frequencies.	Not supported.
Programmable TECLK output pin (1.544MHz or 2.048MHz)	Not supported.
Programmable CLKA output pin See **Table 5** for available output frequencies.	Not supported.
Flexible interrupt pin	Not supported.

Table 2. LXT384 Features Not Present in DS26303

DS26303	LXT384
Uses single optimal value.	Capability to select the jitter attenuator bandwidth.
—	Analog JTAG

MLCK Pin Functionality

The DS26303 and LXT384 both require MCLK to for data with clock recovery as well as AIS detection. The MCLK pin of the LXT384 provides additional functionality not present in the DS26303.

LXT384 MCLK held high.

- The LXT384 operates as a simple data receiver. The clock-recovery circuit is disabled and RPOS/RNEG are internally connected to an EXOR that is fed to the RCLK pin for external clock recovery. The PLL recovery circuit is disabled in this mode.

LXT384 MCLK held low.

- RPOS/RNEG and RCLK go to a high-impedance state.

Table 3. Feature Differences Between DS26303 and LXT384

DS26303	LXT384
3.3V LIU power only, 5V not provided.	5V LIU power.
Non-mux Intel® write address to WRB rising-edge setup time is 17ns.	Non-mux Intel write address to WRB rising-edge setup time is 6ns.
Expects non-mux Intel read address to be valid when RDB is	Non-mux Intel read address to RDB rising-edge setup time is 6ns. This might be an error in datasheet because data is out before this

active.	setup time.
Inactive RDY to tri-state delay time 12ns (max).	Inactive RDY to tri-state delay time 3ns (max).
Clears the interrupt pin when reading or writing the interrupt status.	Clears interrupt pin when reading the status register.
Jitter attenuator FIFO depths of 32 bits or 128 bits.	Jitter attenuator FIFO depths of 32 bits or 64 bits.
Individual channel control for jitter attenuator: • Enable/disable • FIFO depth • FIFO limit trip	All channels have global control.

Table 4. MCLK Selections for the DS26303

PLLE	MPS1, MPS0	MCLK MHz (±50ppm)	FREQS	T1 or E1 Mode
0	xx	1.544	x	T1
0	xx	2.048	x	E1
1	00	1.544	1	T1/J1 or E1
1	01	3.088	1	T1/J1 or E1
1	10	6.176	1	T1/J1 or E1
1	11	12.352	1	T1/J1 or E1
1	00	2.048	0	T1/J1 or E1
1	01	4.096	0	T1/J1 or E1
1	10	8.192	0	T1/J1 or E1
1	11	16.384	0	T1/J1 or E1

Table 5. DS26303 Clock A Selections

CLKA3 to CLKA0	MCLK (Hz)
0000	2.048M
0001	4.096M
0010	8.192M
0011	16.384M
0100	1.544M
0101	3.088M
0110	6.176M
0111	12.352M
1000	1.536M
1001	3.072M
1010	6.144M
1011	12.288M

1100	32k
1101	64k
1110	128k
1111	256k

Register Considerations

The DS26303 contains four major register banks.

- Primary Registers (DS26303 and LXT384)
- Secondary Registers (DS26303 only)
- Individual LIU Registers (DS26303 only)
- BERT Registers (DS26303 only)

The Primary Registers of the DS26303 are the same as the registers in the LXT384 with one exception. Register address 1Fh that is reserved in the LXT384 is instead used in the DS26303 as an address pointer (ADDP) for the DS26303's additional register banks. If the DS26303 is used in the place of an existing LXT384, the application software does not require modification. Table 6 provides a list of the Primary Registers contained in the DS26303 and the LXT384.

Table 6. Primary Registers of the DS26303 and the LXT384

Address (Hex)	DS26303	LXT384
00–15	Primary Registers	Registers
16–1E	Reserved	Reserved
1F	ADDP (Address pointer for additional register banks). This register must be set to point to the desired register bank. 00h) Primary Bank AAh) Secondary Bank 01h) Individual LIU Bank 02h) BERT Bank	Reserved

To take advantage of the DS26303's additional features and flexibility, additional code must be added to any original source code written for an LXT384 application. The address of the ADDP register in the DS26303 is 1F (hex), which is a reserved address in the LXT384. ADDP is used as a pointer to access the different banks of registers. Table 7 provides a list of the DS26303 Register Banks and the required ADDP value required for access to the desired Register Bank.

Table 7. DS26303 Address Pointer Bank Selection

ADDP7 to ADDP0 (Hex)	Bank Name
00	Primary Bank
AA	Secondary Bank
01	Individual LIU Bank
02	BERT Bank

Table 8 provides a list of the registers contained in the Secondary Register Bank. Table 9 presents a list of the registers contained in the Individual LIU Register Bank and Table 10 has a list of the registers contained in the BERT Register Bank.

Table 8. Secondary Register Bank of the DS26303

Address (Hex)	Register Name
00	Single-Rail Mode Select
01	Line-Code Selection
02	Not used
03	Receiver Power-Down Enable
04	Transmitter Power-Down Enable
05	Excessive Zero-Detect Enable
06	Code-Violation-Detect Enable Bar
07–1E	Not used
1F	Set to AAh for access to Secondary Register Bank

Table 9. Individual LIU Register Bank of the DS26303

Address (Hex)	Register Name
00	Individual JA Enable
01	Individual JA Position Select
02	Individual JA FIFO Depth Select
03	Individual JA FIFO Limit Trip
04	Individual Short-Circuit-Protection Disable
05	Individual AIS Select
06	Master Clock Select
07	Global-Management Register
08–0F	Reserved
10	Bit-Error-Rate Tester Control Register
12	Line-Violation Detect Status
13	Receive Clock Invert
14	Transmit Clock Invert
15	Clock-Control Register
16	RCLK Disable Upon LOS Register
1E	Global-Interrupt Status Control
1F	Set to 01h for access to Individual LIU Register Bank

Table 10. BERT Register Bank of the DS26303

Address (Hex)	Register Name
00	BERT Control Register
01	Reserved
02	BERT Pattern Configuration 1
03	BERT Pattern Configuration 2
04	BERT Seed/Pattern 1

05	BERT Seed/Pattern 2
06	BERT Seed/Pattern 3
07	BERT Seed/Pattern 4
08	Transmit-Error Insertion Control
09–0A	Reserved
0C	BERT Status Register
0D	Reserved
0E	BERT Status Register Latched
10	BERT Status Register Interrupt Enable
11–13	Reserved
14	Receive Bit-Error Count Register 1
15	Receive Bit-Error Count Register 2
16	Receive Bit-Error Count Register 3
17	Receive Bit-Error Count Register 4
18	Receive Bit Count Register 1
19	Receive Bit Count Register 2
1A	Receive Bit Count Register 3
1B	Receive Bit Count Register 4
1C–1E	Reserved
1F	Set to 02h for access to BERT Register Bank

Hardware Considerations

The DS26303 can replace the LXT384 in an existing application without PCB layout changes. All that is needed is to replace external component values for the desired application. Figure 1 provides the recommended DS26303 network termination circuit and Table 11 provides the component values required for proper termination of the DS26303.

Transmitter

The LXT384 requires transmit-side resistors in series with TTIP and TRING outputs. The LXT384 recommends that these resistors should be 0Ω (T1 3.3V mode), 11Ω (E1 75Ω coaxial), or 11Ω (E1 120Ω twisted pair). The DS26303 does not require resistors, so any present should be 0Ω in all modes. The LXT384 requires a DC-blocking capacitor when pulse shaping is disabled. The DS26303 does not require a DC-blocking capacitor, so it should be replaced with a 0Ω resistor if present in the PCB circuit of an existing LXT384 application..

Receiver

On the receive side, the LXT384 requires termination resistance of 12.4Ω (T1 3.3V mode), 9.31Ω (E1 75Ω coaxial), or 15Ω (E1 120Ω twisted pair). The DS26303 requires 15Ω termination resistors for all modes when using external impedance mode. If the DS26303's software-selectable impedance-matching mode is used, these resistors are not required. The LXT384 requires 1kΩ resistors in series with the RTIP and RRING pins. If software termination/impedance matching is desired, these 1kΩ resistors should be replaced with 0Ω resistors.

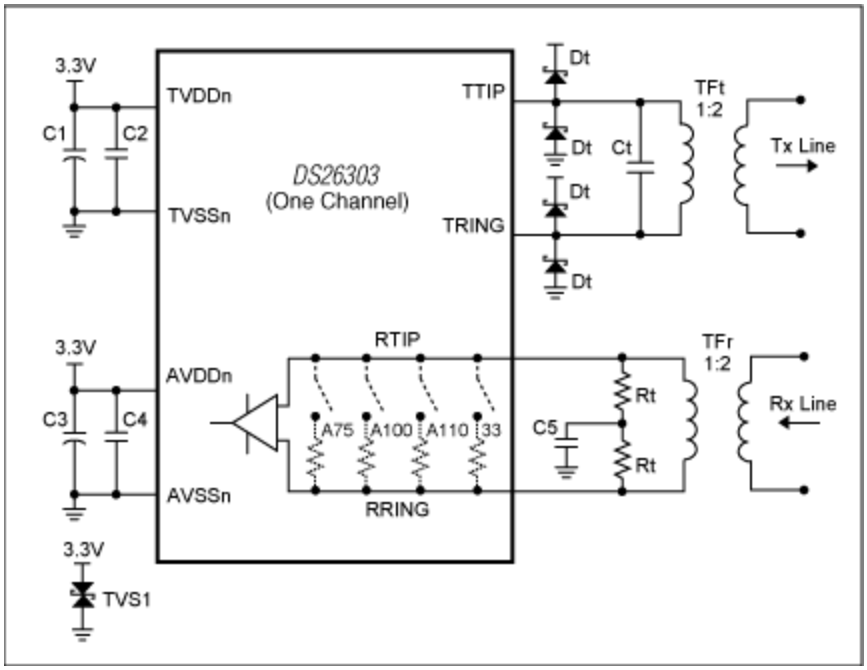

Figure 1. LIU front-end

Table 11. LIU Front-End Values

Mode	Component	75Ω Coax	120Ω Twisted Pair	100Ω/110Ω Twisted Pair
Tx Capacitance	Ct	560pF (typ). Adjust for board parasitics for optimal return loss.		
Tx Protection	Dt	International Rectifier: 11DQ04 or 10BQ060 Motorola: MBR0540T1		
Rx Transformer 1:2	TFr	Pulse: T1124 (0°C to +70°C)		
Tx Transformer 1:2	TFt	Pulse: T1114 (-40°C to +85°C)		
Tx Decoupling (ATVDD)	C1	Common decoupling for all eight channels is 68µF.		
Tx Decoupling (ATVDD)	C2	Recommended decoupling per channel is 0.1µF.		
Rx Decoupling (AVDDn)	C3	Common decoupling for all eight channels is 68µF.		
Rx Decoupling (AVDDn)	C4	Common decoupling for all eight channels is 0.1µF.		
Rx Termination	C5	When in external impedance mode, Rx capacitance for all eight channels is 0.1µF. Do not populate if using internal impedance mode.		
Rx		When in external impedance mode, the two resistors for all modes is		

Termination	Rt	15.0Ω ±1%. Do not populate if using internal impedance mode.
Voltage Protection	TVS1	SGS-Thomson: SMLVT 3V3 (3.3V transient suppressor)

DS26303 Further Information

For more information about Maxim communication products, please consult the data sheets available on our website at T/E Carrier and Packetized Products. If you have further questions concerning the operation of these communication devices, please contact the Telecommunication Applications support team.

Related Parts		
DS26303	3.3V, E1/T1/J1, Short-Haul, Octal Line Interface Unit	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 3915: http://www.maximintegrated.com/an3915
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