Keywords: DVI, HDMI, display port, DP, RGBHV, VGA, display cable interface, phase-locked loop, PLL, LVDS, vertical, horizontal synchronization, flat screen, ADC, analog to digital conversion, I2C, blanking, TMDS, hot plug detect, EDID, DDC, GPU

APPLICATION NOTE 4306

Video Display Signals and the MAX9406 DP-HDMI/DVI Level Shifter—Part I

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Abstract: This application note is the first of a two-part article. Part I examines the current TV and PC display-cable interfaces and covers the features of RGBHV, HDMI™, and VGA. Refer to Part II of this article (application note 4313) for detailed background on DVI™ and how the MAX9406 is used as a suitable digital-display cable driver.

Introduction

Both TV and PC displays are moving toward a flat screen with digital cable interface. A flat-screen TV can be connected to a PC or a high-definition TV (HDTV) set-top box using a high-definition multimedia interface (HDMI) cable. A PC can be connected to an external monitor by a VGA or a digital video interface (DVI) cable. The DVI can be considered the digital equivalent of a VGA interface. Note that the video portion of HDMI is identical to DVI.

This is Part 1 of the article. This application note examines current TV and PC display cable interfaces and covers the features of RGBHV, HDMI, and VGA. Refer to Part 2 of this article, application note 4313, "Video Display Signals and the MAX9406 DP-HDMI/DVI Level Shifter—Part II" for detailed background on DVI and how the MAX9406 is utilized as a suitable digital-display cable driver.

RGBHV

The RGBHV format is an advanced analog video-display interface for high-definition displays. RGBHV video signals are carried across five separate pairs of cables, namely R, G, B, H, and V. Each of these cables is terminated by a BNC or RCA jack. Cables R, G, and B carry red, green, and blue signals, respectively; cable H carries the horizontal and V the vertical synchronization pulses.

One end of these RGBHV cables can also be terminated by a VGA plug. **Figure 1** shows the typical color code of RGBHV video cables. The R is coded to red, G to green, B to blue, H to gray, and V to black. All termination impedances are 75Ω.

Figure 1. Color code of component video cables.

The RGBHV is the most up-to-date analog video-signal format that can carry HDTV programs with little or no degradation in picture quality. **Figure 2** shows the relationship between the RGBHV and other analog video signal formats.

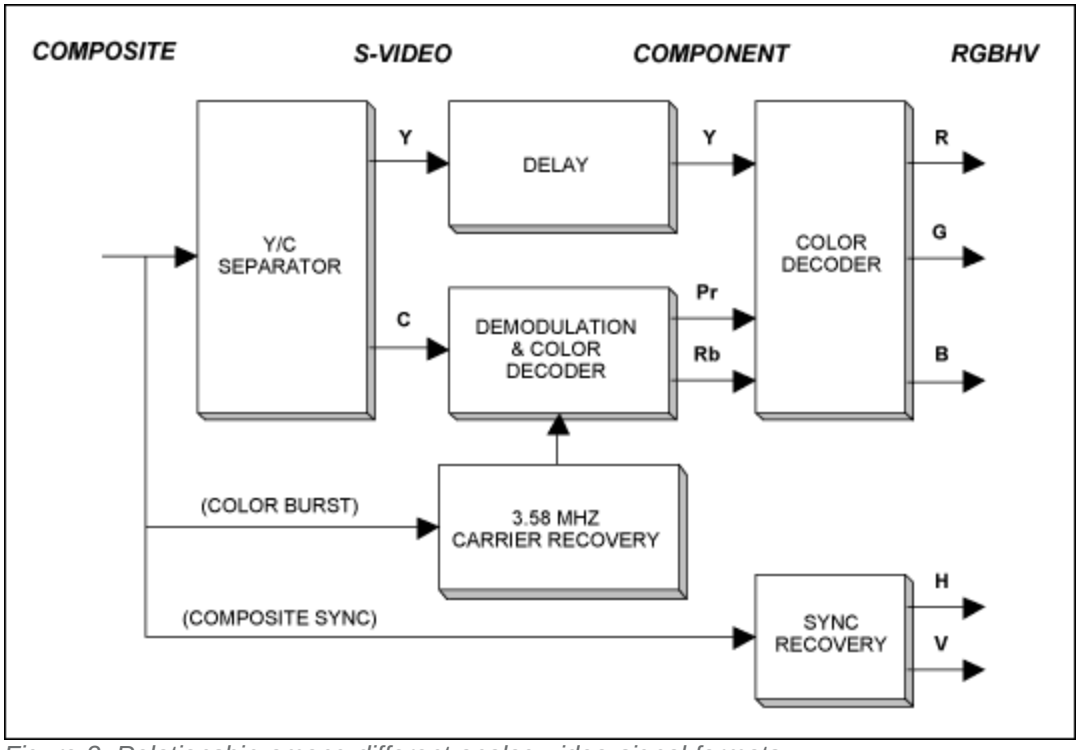

Figure 2. Relationship among different analog video signal formats.

The arrows in Figure 2 show the direction of the evolution in this technology. In practice, all different types of analog video signals are created using the basic red, green, blue, horizontal, and vertical

synchronization components. The Y/C separator functional block is a concept for the total separation of luminance and chrominance from the composite signal. Although the combination is straightforward, the total separation is difficult to achieve in reality. The carrier recovery from the color burst is possible, and the I and Q components of the chrominance can be recovered through a demodulation process. However, I and Q are not equivalent to Pr and Pb before some recombinations. Also, the synchronization pulses of the composite signal are not just the addition of the horizontal and vertical components. Instead, pre- and post-equalization pulses are added before and after the vertical synchronization pulse to enable the continuous operation of the phase locked loop (PLL) for the horizontal synchronization recovery.

With the introduction of HDTV, video information is processed in the digital domain after the demodulation from the RF (radio frequency) carrier. However, flat-screen displays are digital natives. Using a digital-video signal cable can avoid the extra steps of digital-to-analog conversion (DAC) at the HDTV side and analog-to-digital conversion (ADC) at the flat-screen-display side while eliminating possible degradations introduced by the conversion processes.

HDMI

The HDMI consists of four low-voltage differential signal (LVDS) pairs. Red, green, and blue signals are each carried by channels 2 through 0 (LVDS pairs), respectively. A dedicated clock (synchronized to data bits on channels 0 through 2) LVDS pair is used to provide reliable transmission between an HDTV and a flat screen. The amplitude for each color pixel is digitized to 8-bit resolution with the ADC function. The color information is expanded to 10-bit resolution by the so-called transition minimized differential signalling (TMDS®) encoder for bandwidth minimization and DC balancing. The encoded color bits are serialized and sent to the LVDS driver circuit. See **Figure 3**.

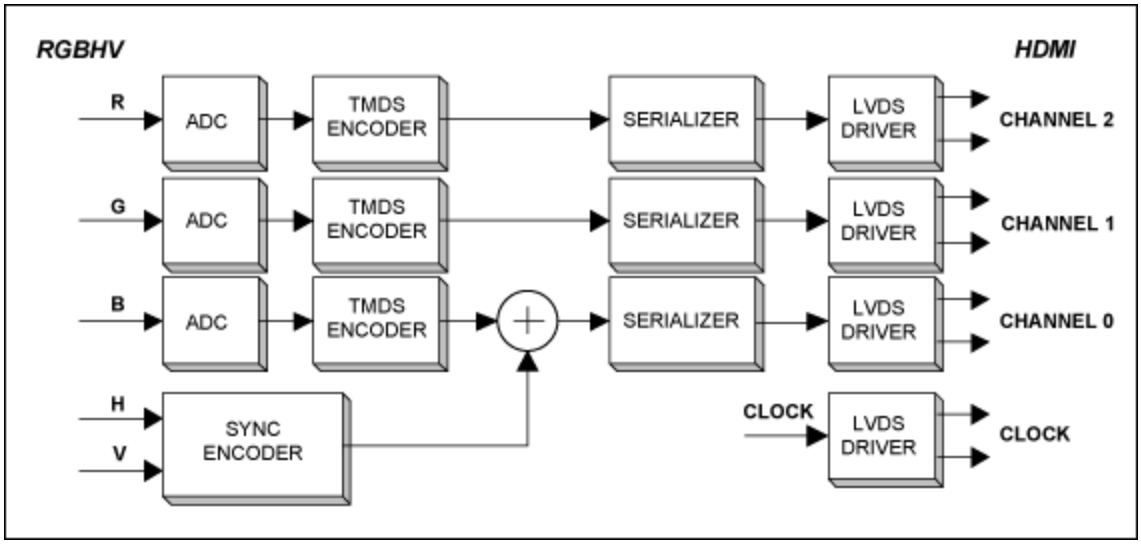

Figure 3. RGBHV-to-HDMI conversion.

The data rate for each LVDS channel can be high. For a HDTV screen resolution of 1920 × 1080 with a refresh rate of 60Hz, the pixel rate is 124.416MHz. The respective pixel rates are 130MHz or 143MHz with synchronization and blanking overheads of 5% or 15%. At 10 bits per pixel color, the data rate for each LVDS channel ranges from 1.3Gbps and 1.43Gbps, depending on the amount of the desired overhead. For flat-screen displays, the blanking for an electron beam to swing back is not necessary. Therefore, the overhead is usually small as long as the synchronization timing can be recovered properly.

The timing sequence of the analog video signals is exactly followed in the digital video signal format. In HDMI format, pixels are sent from left to right with horizontal synchronization codes between every line; lines are sent from top to bottom with vertical synchronization codes between every screen. During the times corresponding to the blanking of the analog video signal between every line and between every screen, horizontal and vertical synchronization pulses are encoded in channel 0. Four 10-bit code words, 1101010100, 0010101011, 0101010100, and 1010101011, represent (H = 0, V = 0), (H = 1, V = 0), (H = 0, V = 1), and (H = 1, V = 1), respectively. Using these codes, the horizontal and vertical synchronization pulses can be represented in the time domain with the accuracy of the pixel clock.

Since only the starting point of the synchronization pulses is most important, it is not necessary to code these pulses for the entire duration, as defined by the analog format. In HDMI format, a portion of the blanking time after the definition of the start of a synchronization pulse has been dedicated to send an audio signal. The period corresponding to the blanking period of analog formats is divided into a control period for synchronization and a data island period for sending audio information bits.

Figure 4 shows the timing of the synchronization and audio packet bits within a horizontal blank period, as defined by an analog video format. The horizontal synchronization bits are carried on channel 0 immediately after the video information bits. This synchronization information-only period can last 62 pixel clock periods in a typical blanking period of 138 pixels. After that, 64 pixels are dedicated to carrying audio packets. The header of the audio packets, together with synchronization information, is then carried on channel 0 and the audio packet bits are carried on channels 1 and 2. During the data island period for each channel, every group of four information bits is coded into 10 bits using the TMDS Error Reduction Coding (TERC4). During the same time period, two audio header bits and two horizontal synchronization bits are combined as input to the TERC4 encoder for channel 0. The blanking period ends with a small number of horizontal synchronization pixels (12).

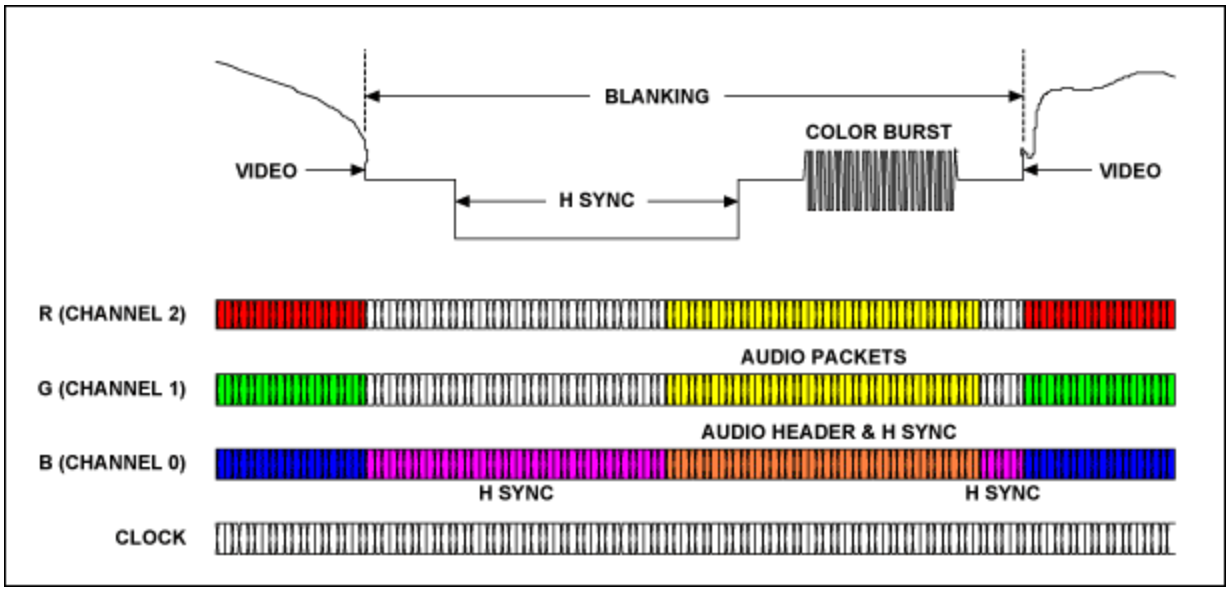

Figure 4. HDMI video data, control, and data island periods.

With a screen refresh rate of 60Hz, 1080 lines per screen, 64 pixels per line, and 8 bits per pixel for an HDTV signal, then the maximum audio information bit rate can be calculated using the following formula:

$R_{Audio} = 60 \times 1080 \times 64 \times 8 = 33.1776\text{Mbps}$

This data rate is high enough to carry any multichannel high-quality audio signals.

The information of every pixel can also be represented by more than 8 bits per color in HDMI. For these higher color-resolution formats, the number of bits per pixel color is spread into more than one 8-bit 8B10B encoding unit. For example, to have 10 bits per color, data bits of four pixels are spread to five 8B10B encoding units, resulting in a clock-rate increase of 20%. Similarly, 12 bits per color will spread two pixels to three 8B10B encoding units with a clock rate increase of 50%. The capability of higher color resolution in a flat-panel display is indicated by the contents of its extended display identification data (EDID).

Figure 5 and **Table 1** show pin assignments for an HDMI type A plug. The SCL and the SDA are used to obtain the flat-panel display information for an HDTV set using the I²C protocol. The flat-screen display information (the EDID) are all stored in an EEPROM of typically 128 bytes with an I²C device address of 0×A0. The hot-plug-detect pin is useful for the HDTV set to sense the presence of a flat-screen display. A turned-on flat-panel display sets the hot-plug pin to between 2.4V and 5.3V. CEC indicates consumer electronics control and is used to pass user controls to all interconnected electronic devices.

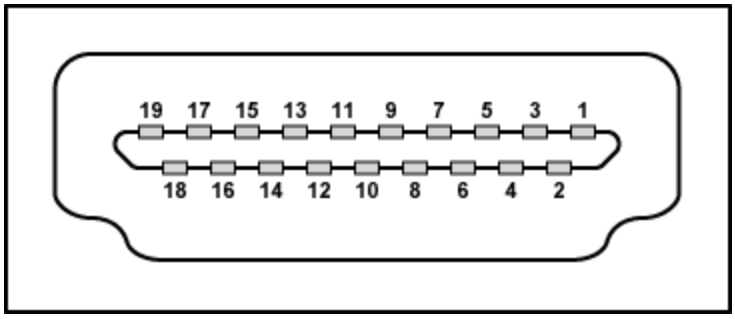

Figure 5. HDMI type A plug pin numbers.

Table 1. HDMI Type A Plug Pin Assignment

Pin Number	Assignment
1	Data2+
2	Data2 shield
3	Data2-
4	Data1+
5	Data1 shield
6	Data1-
7	Data0+
8	Data0 shield
9	Data0-
10	Clock+
11	Clock shield
12	Clock-
13	CEC
14	Not connected
15	SCL
16	SDA
17	Ground
18	+5V
19	Hot-plug detect

The HDMI signals are directly compatible with those of DVI. (See part 2 of this article series for more details regarding DVI.) **Figure 6** shows a HDMI-DVI conversion cable. A PC with a DVI output can be connected to a flat-planel display with a HDMI input using such a conversion cable.

Figure 6. A HDMI-to-DVI conversion cable.

VGA

Figure 7 shows the functional block diagram of a VGA plug-in card. To avoid burdening the CPU with pixel-writing tasks (e.g., moving graphics), a dedicated graphics processing unit (GPU) is utilized. The

CPU can just send the attribute of a particular display for a partial or a full screen and the GPU will fill the video RAM with the proper pixel contents. The display timing generation function can be a part of the GPU. To enable automatic detection of the monitor's capability, an I²C channel named as display data channel (DDC), is available on every VGA plug. The monitor's EDID information (128 bytes with an address of 0×A0) is usually stored in an EEPROM.

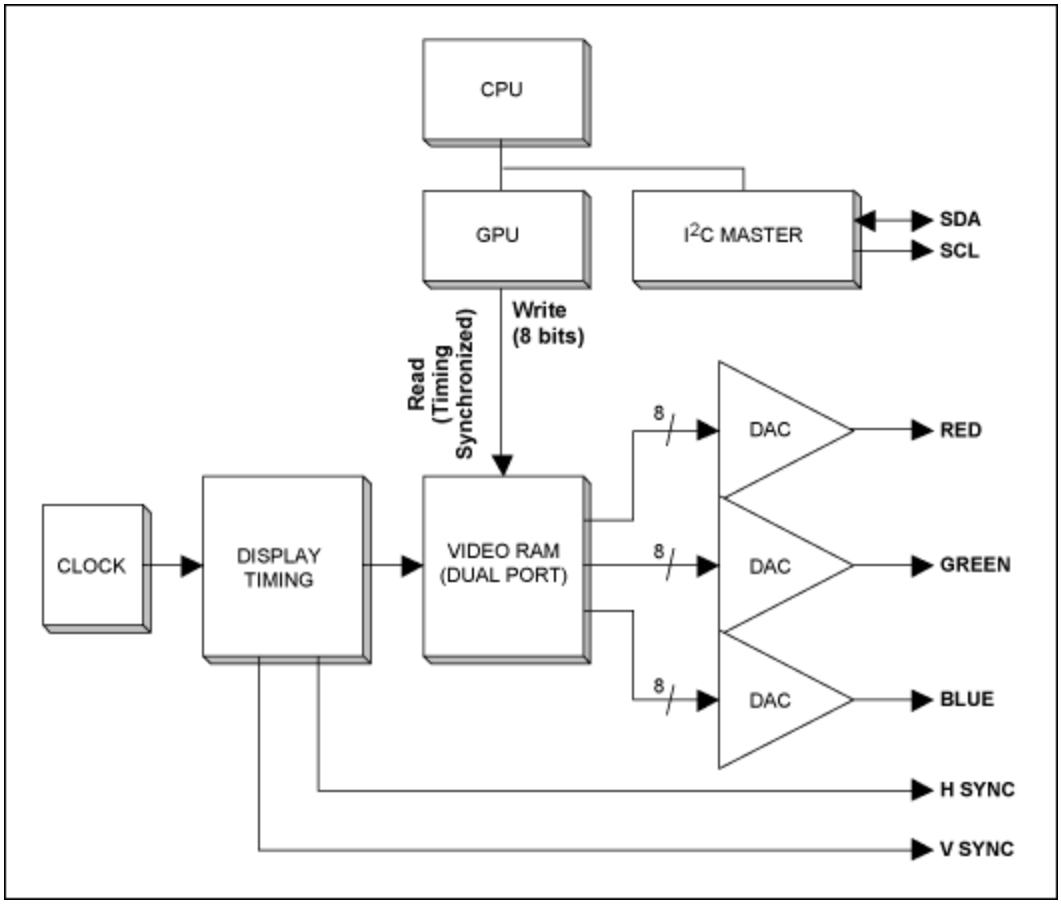

Figure 7. Functions of a VGA plug-in card.

The VGA cable terminates with a 15-pin plug. **Figure 8** and **Table 2** show the pin assignment for VGA signals. The signal levels on the red, green, blue, horizontal, and vertical synchronization pins are $0.7V_{P-P}$. Terminal impedance for these video signal pins is 75Ω. The same 15-pin VGA plug has been used for its enhanced versions such as SVGA (800 × 600), XGA (1024 × 768), SXGA (1280 × 1024), UXGA (1600 × 1200), WXGA (1366 × 768), WSXGA (1680 × 1050), and WUXGA (1920 × 1200) signal formats with higher screen-pixel resolutions.

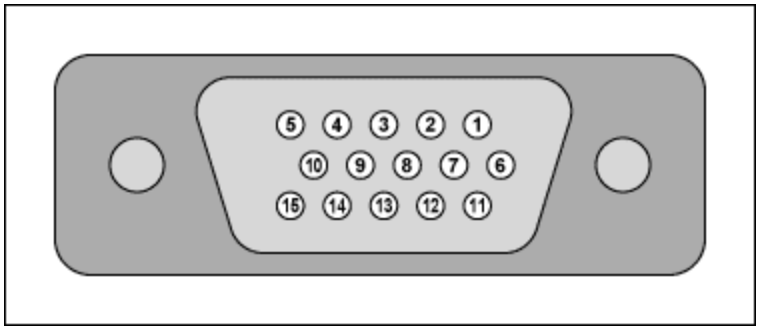

Figure 8. VGA plug pinout.

Table 2. VGA Plug Pin Assignment

Pin Number	Assignment
1	Red
2	Green
3	Blue
4	
5	Ground
6	Ground (red)
7	Ground (green)
8	Ground (blue)
9	+5V
10	Ground (shield)
11	
12	SDA
13	H
14	V
15	SCL

Summary

Looking back we see the evolution of the TV display signal from composite, S-video, component, RGBHV, and eventually to HDMI, which is a digital version of the high-definition RGBHV signal. The TV display signal has evolved from analog to digital with better resolution after each step. The still popular PC VGA monitor display signal is in analog format. VGA has evolved from earlier CGA (color graphics adaptor) and EGA (enhanced graphics adaptor) formats, both of which are actually digital formats but with no bandwidth-efficient bit-encoding schemes. Without using DACs, the resolution of the VGA will demand too many pins on a cable plug. The digital version of VGA, which will be introduced in Part II of this article, is DVI which replaces DACs with bandwidth-efficient bit encoders.

Related Parts		
MAX9406	DisplayPort to DVI™/HDMI Level Shifter	Free Samples

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