# TPS2116 1.6 V to 5.5 V, 2.5-A Low $I_Q$ Power Mux with Manual and Priority Switchover

## 1 Features

- Input voltage range: 1.6 V to 5.5 V
- Maximum continuous current: 2.5 A
- On-resistance: 40 mΩ (typical)
- VIN2 standby current: 50 nA (typical)
- Quiescent current: 1.32 uA (typical)
- Switchover modes:
  - Priority mode
  - Manual mode
- Controlled output slew rate:
  - 1.3 ms (typical) at 3.3 V
- Reverse Current Blocking when VOUT > VINx
- Thermal shutdown

## 2 Applications

- Backup battery systems
- E-Meters
- Motor Drives
- Building Automation

## 3 Description

The TPS2116 is a power mux device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

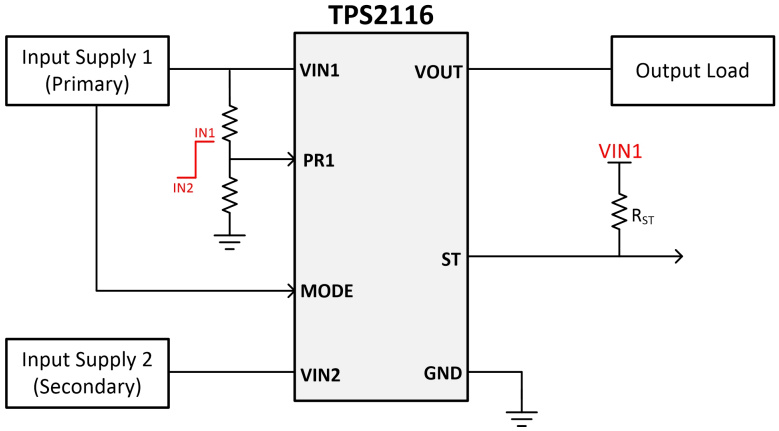
Due to its low quiescent of 1.32 uA (typical) and low standby current of 50 nA (typical), the TPS2116 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

The TPS2116 can be configured for two different switchover behaviors depending on the application. Automatic priority mode prioritizes the supply connected to VIN1 and switches over to the secondary supply (VIN2) when VIN1 drops. Manual mode allows the user to toggle a GPIO or enable signal to switch between channels.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS2116 | SOT (8) | 2.1 mm x 1.6 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Basic Application**

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## 4 Revision History

| Changes from Revision * (January 2021) to Revision A (May 2021) | Page |
|---|---|
| • Changed status from "Advance Information" to "Production Data" | 1 |

## 5 Pin Configuration and Functions

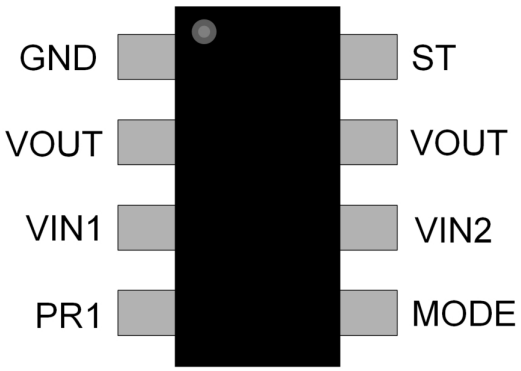



**Figure 5-1. DRL Package 8-Pin SOT Top View**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1 | - | Device ground. |
| VOUT | 2, 7 | O | Output power. |
| VIN1 | 3 | I | Channel 1 input power. |
| PR1 | 4 | I | Selects between VIN1 and VIN2. When PR1 is high VIN1 is selected, and when PR1 is low VIN2 is selected. |
| MODE | 5 | I | Device is put into Priority mode when MODE is tied to VIN1 and manual mode when MODE is pulled up to an external voltage. |
| VIN2 | 6 | I | Channel 2 input power. |
| ST | 8 | O | Open drain status pin. Pulled low when VIN1 is not being used. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN1}$, $V_{IN2}$ | Input Voltage | –0.3 | 6 | V |
| $V_{OUT}$ | Output Voltage | –0.3 | 6 | V |
| $V_{ST}$, $V_{PR1}$, $V_{MODE}$ | Control Pin Voltage | –0.3 | 6 | V |
| $I_{MAX}$ | Maximum Current | | 2.5 | A |
| $I_{MAX,PLS}$ | Maximum Pulsed Current<br>Max duration 1ms, Duty cycle of 2% | | 4 | A |
| $T_J$ | Junction temperature | | Internally Limited | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN1}$, $V_{IN2}$ | Input Voltage | 1.6 | | 5.5 | V |
| $V_{OUT}$ | Output Voltage | 0 | | 5.5 | V |
| $V_{ST}$, $V_{MODE}$, $V_{PR1}$ | Control Pin Voltage | 0 | | 5.5 | V |
| $T_A$ | Ambient Temperature | –40 | | 105 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPS2116 DRL (SOT) 8-PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 111.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 19.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 35.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 19.1 | °C/W |

## 6.4 Thermal Information (continued)

| THERMAL METRIC(1) | | TPS2116 DRL (SOT) 8-PINS | UNIT |
|---|---|---|---|
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Power Consumption** | | | | | | | |
| $I_{STBY, VIN1}$ | VIN1 Standby Current | VIN2 powers VOUT<br>VIN1 > VIN2 + 0.1V | 25°C | | 1.1 | | uA |
| | | | -40°C to 85°C | | | 1.9 | uA |
| | | | -40°C to 105°C | | | 2 | uA |
| | | VIN2 powers VOUT<br>VIN2 > VIN1 + 0.2V | 25°C | | 0.22 | | uA |
| | | | -40°C to 85°C | | | 0.31 | uA |
| | | | -40°C to 105°C | | | 0.32 | uA |
| $I_{STBY, VIN2}$ | VIN2 Standby Current | VIN1 powers VOUT<br>VIN2 > VIN1 + 0.2V | 25°C | | 1.2 | | uA |
| | | | -40°C to 85°C | | | 2 | uA |
| | | | -40°C to 105°C | | | 2.1 | uA |
| | | VIN1 powers VOUT<br>VIN1 > VIN2 + 0.1V | 25°C | | 0.05 | | uA |
| | | | -40°C to 85°C | | | 0.07 | uA |
| | | | -40°C to 105°C | | | 0.09 | uA |
| $I_{Q, VIN1}$ | VIN1 Quiescent Current | VIN1 powers VOUT<br>VIN1 > VIN2 + 0.1V | 25°C | | 1.32 | | uA |
| | | | -40°C to 85°C | | | 3.6 | uA |
| | | | -40°C to 105°C | | | 4.4 | uA |
| | | VIN1 powers VOUT<br>VIN2 > VIN1 + 0.2V | 25°C | | 0.3 | | uA |
| | | | -40°C to 85°C | | | 0.51 | uA |
| | | | -40°C to 105°C | | | 0.55 | uA |
| $I_{Q, VIN2}$ | VIN2 Quiescent Current | VIN2 powers VOUT<br>VIN2 > VIN1 + 0.2V | 25°C | | 1.35 | | uA |
| | | | -40°C to 85°C | | | 3.7 | uA |
| | | | -40°C to 105°C | | | 4.5 | uA |
| | | VIN2 powers VOUT<br>VIN1 > VIN2 + 0.1V | 25°C | | 0.1 | | uA |
| | | | -40°C to 85°C | | | 0.27 | uA |
| | | | -40°C to 105°C | | | 0.29 | uA |
| $I_{SD,VIN1}$ | VIN1 Shutdown Current | MODE = 0V, PR1 = 5V<br>VIN1 > VIN2<br>VOUT = 0V | 25°C | | 0.1 | | uA |
| | | | -40°C to 85°C | | | 1.3 | uA |
| | | | -40°C to 105°C | | | 2.9 | uA |
| | | MODE = 0V, PR1 = 5V<br>VIN1 < VIN2<br>VOUT = 0V | 25°C | | 0.05 | | uA |
| | | | -40°C to 85°C | | | 1 | uA |
| | | | -40°C to 105°C | | | 2.4 | uA |

## 6.5 Electrical Characteristics (continued)

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{SD,VIN2}$ | VIN2 Shutdown Current | MODE = 0V, PR1 = 5V<br>VIN2 > VIN1<br>VOUT = 0V | 25°C | | 0.05 | | uA |
| | | | -40°C to 85°C | | | 1.3 | uA |
| | | | -40°C to 105°C | | | 2.9 | uA |
| | | MODE = 0V, PR1 = 5V<br>VIN2 < VIN1<br>VOUT = 0V | 25°C | | 0.05 | | uA |
| | | | -40°C to 85°C | | | 0.7 | uA |
| | | | -40°C to 105°C | | | 2.1 | uA |
| $I_{REV}$ | Reverse leakage current out of VINx | $V_{OUT}$ = 5.5V<br>$V_{INx}$ = 0V, $V_{INy}$ = Open | 25°C | | 0.001 | | uA |
| | | | 85°C | | 0.05 | | uA |
| | | | 105°C | | 0.15 | | uA |
| | Reverse leakage current into VOUT | $V_{OUT}$ = 5.5V<br>$V_{INx}$ = 0V, $V_{INy}$ = Open | 25°C | | 0.01 | | uA |
| | | | 85°C | | 0.1 | | uA |
| | | | 105°C | | 0.25 | | uA |
| $I_{PR1}$ | PR1 pin leakage | | -40°C to 105°C | | | 0.1 | uA |
| $I_{MODE}$ | MODE pin leakage | | -40°C to 105°C | | | 0.1 | uA |
| $I_{ST}$ | ST pin leakage | | -40°C to 105°C | | | 0.03 | uA |
| **Performance** | | | | | | | |
| $R_{ON}$ | On-Resistance | VINx = 5V<br>$I_{OUT}$ = 200mA | 25°C | | 37 | 46 | mΩ |
| | | | -40°C to 85°C | | | 55 | mΩ |
| | | | -40°C to 105°C | | | 60 | mΩ |
| | | VINx = 3.3V<br>$I_{OUT}$ = 200mA | 25°C | | 40 | 48 | mΩ |
| | | | -40°C to 85°C | | | 55 | mΩ |
| | | | -40°C to 105°C | | | 59 | mΩ |
| | | VINx = 1.8V<br>$I_{OUT}$ = 200mA | 25°C | | 41 | 51 | mΩ |
| | | | -40°C to 85°C | | | 61 | mΩ |
| | | | -40°C to 105°C | | | 66 | mΩ |
| | | VINx = 1.6V<br>$I_{OUT}$ = 200mA | 25°C | | 42 | 52 | mΩ |
| | | | -40°C to 85°C | | | 68 | mΩ |
| | | | -40°C to 105°C | | | 74 | mΩ |
| $V_{OL,ST}$ | Status pin $V_{OL}$ | $I_{ST}$ = 1mA | -40°C to 105°C | | | 0.1 | V |
| $t_{ST}$ | Status pin response time | ST pin pulled high to low<br>$R_{ST}$ = 10kΩ | -40°C to 105°C | | 5 | | us |
| $V_{REF}$ | PR1 reference voltage | | -40°C to 105°C | 0.92 | 1 | 1.08 | V |
| $V_{IH,MODE}$ | MODE logic high threshold | | -40°C to 105°C | 1 | | 5.5 | V |
| $V_{IL,MODE}$ | MODE logic low threshold | | -40°C to 105°C | 0 | | 0.35 | V |
| **Protection** | | | | | | | |
| $t_{RCB}$ | Reverse current blocking response time | VOUT > Selected VIN + 1V | -40°C to 105°C | | 2 | | us |
| $V_{RCB,R}$ | Reverse current blocking rising threshold ($V_{OUT}$ - $V_{IN}$) | | -40°C to 105°C | | 42 | 70 | mV |
| $V_{RCB,F}$ | Reverse current blocking falling threshold ($V_{OUT}$ - $V_{IN}$) | | -40°C to 105°C | | 17 | 40 | mV |
| $I_{RCB}$ | Reverse current blocking activation current | | -40°C to 105°C | | 1.4 | 4 | A |
| TSD | Thermal shutdown | | - | | 170 | | °C |

## 6.5 Electrical Characteristics (continued)

Over operating free-air temperature range and operating voltage range of 1.6V to 5.5V (unless otherwise noted). Typical specifications are at an input voltage of 3.3V and ambient temperature of 25°C.

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $TSD_{HYS}$ | Thermal shutdown hysteresis | | - | | 20 | | °C |

## 6.6 Switching Characteristics

Typical switching characteristics are defined at an ambient temperature of 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Switchover** | | | | | | |
| $t_{SW}$ | Switchover time, VINx = 5 V | $R_L$ = 10 Ω, $C_L$ = 10 uF | | 8 | | us |
| $t_{SW}$ | Switchover time, VINx = 3.3 V | $R_L$ = 10 Ω, $C_L$ = 10 uF | | 6.2 | | us |
| $t_{SW}$ | Switchover time, VINx = 1.8 V | $R_L$ = 10 Ω, $C_L$ = 10 uF | | 17.7 | | us |
| $t_D$ | Delay time, VINx = 5 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 1 | | ms |
| $t_D$ | Delay time, VINx = 3.3 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 1.2 | | ms |
| $t_D$ | Delay time, VINx = 1.8 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 1.4 | | ms |
| $t_{SS}$ | Soft-start time, VINx = 5 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 1.7 | | ms |
| $t_{SS}$ | Soft-start time, VINx = 3.3 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 1.3 | | ms |
| $t_{SS}$ | Soft-start time, VINx = 1.8 V | $R_L$ = 100 Ω, $C_L$ = 10 uF | | 0.9 | | ms |

## 6.7 Timing Diagrams

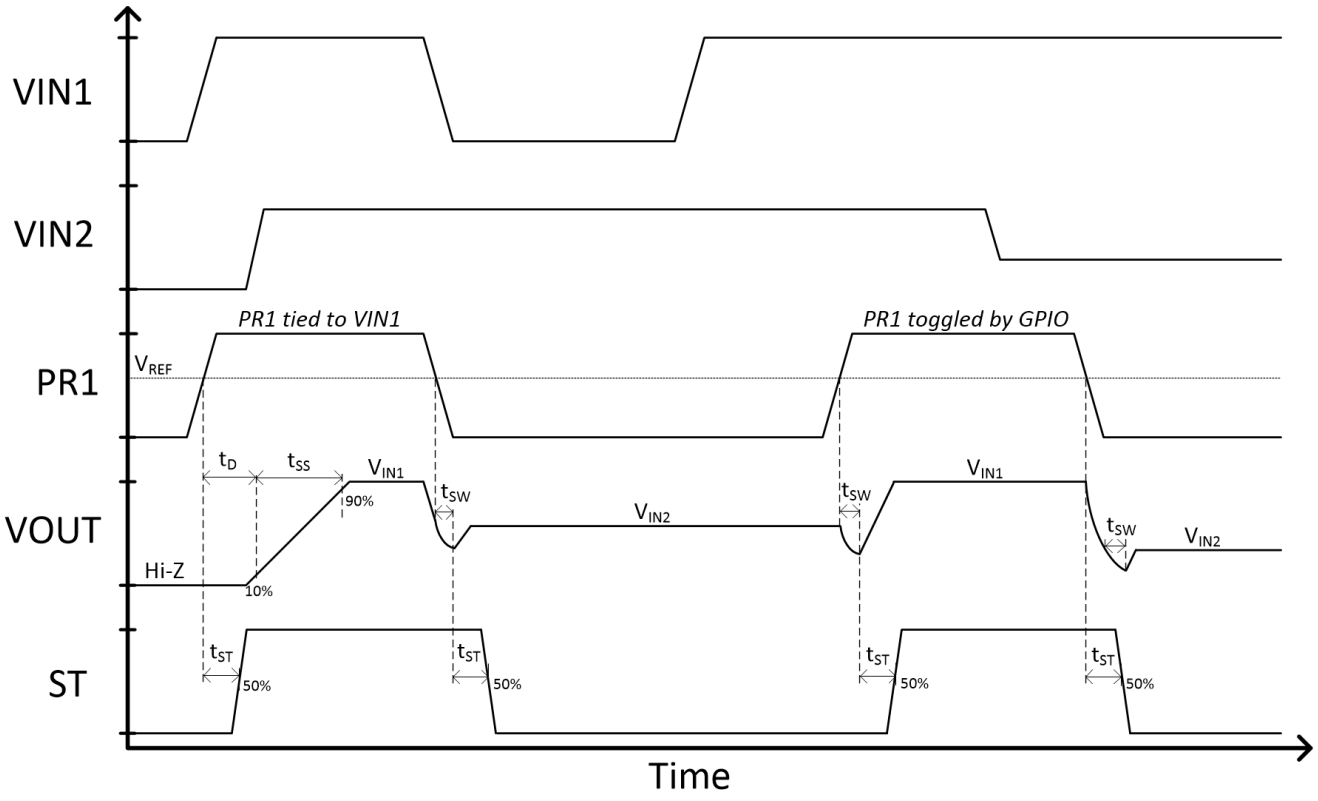
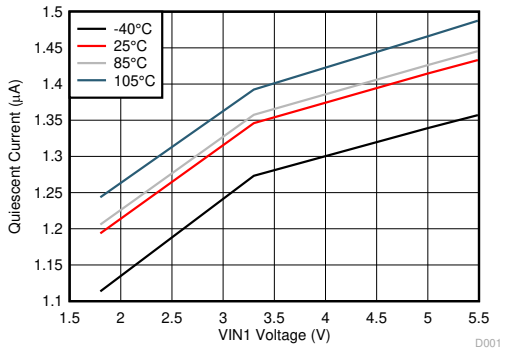


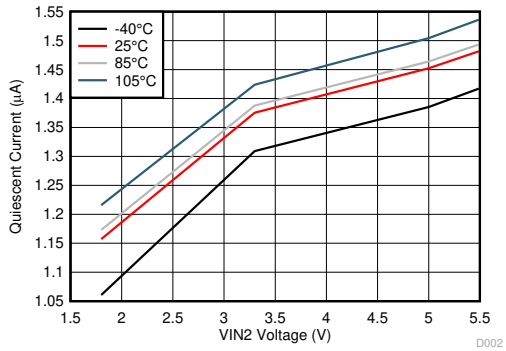

**Figure 6-1. TPS2116 Timing Diagram**

## 6.8 Typical Characteristics



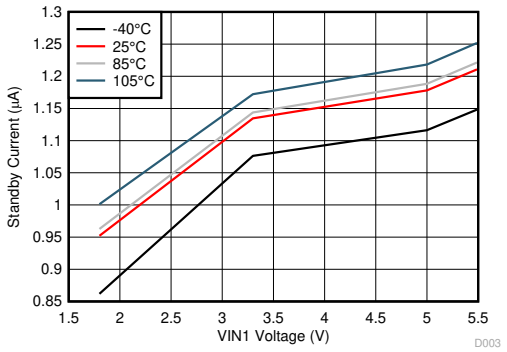

VIN2 = 1.6 V VOUT = Open

**Figure 6-2. VIN1 Quiescent Current vs Input Voltage**



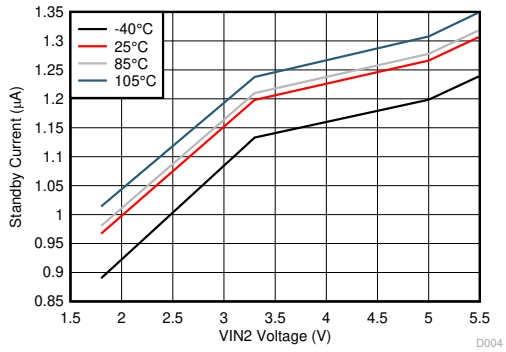

VIN1 = 1.6 V VOUT = Open

**Figure 6-3. VIN2 Quiescent Current vs Input Voltage**



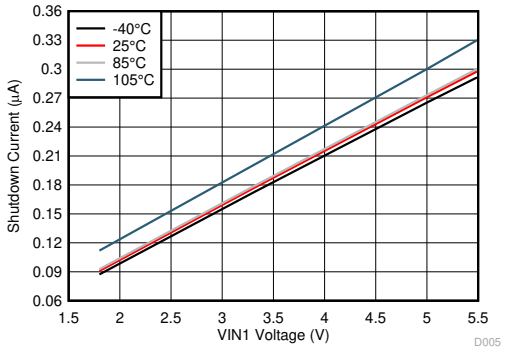

VIN2 = 1.6 V VOUT = Open

**Figure 6-4. VIN1 Standby Current vs Input Voltage**



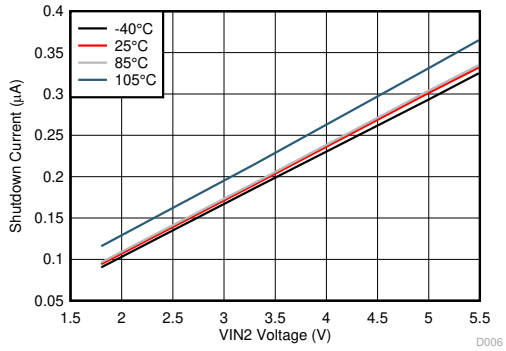

VIN1 = 1.6 V VOUT = Open

**Figure 6-5. VIN2 Standby Current vs Input Voltage**




VIN2 = 1.6 V VOUT = Open

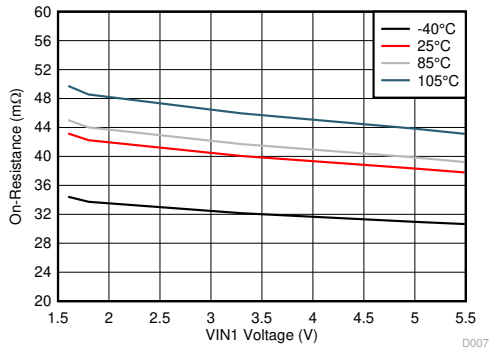
**Figure 6-6. VIN1 Shutdown Current vs Input Voltage**




VIN1 = 1.6 V VOUT = 0 V

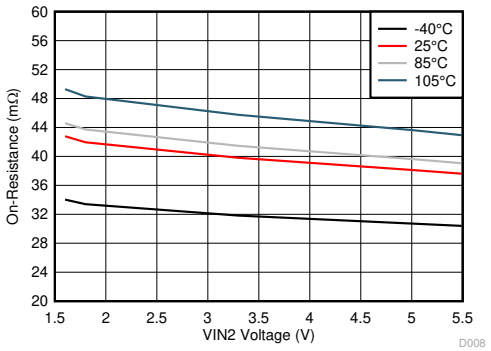
**Figure 6-7. VIN2 Shutdown Current vs Input Voltage**

## 6.8 Typical Characteristics (continued)



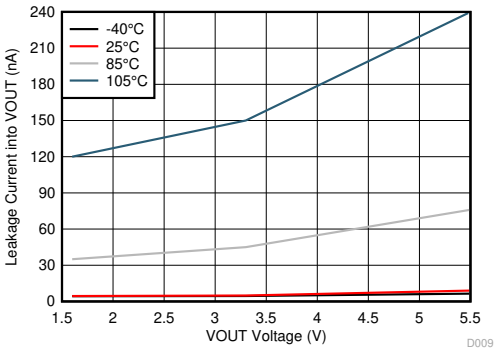

$I_{OUT}$ = 200 mA

**Figure 6-8. Channel 1 On-Resistance vs Input Voltage**



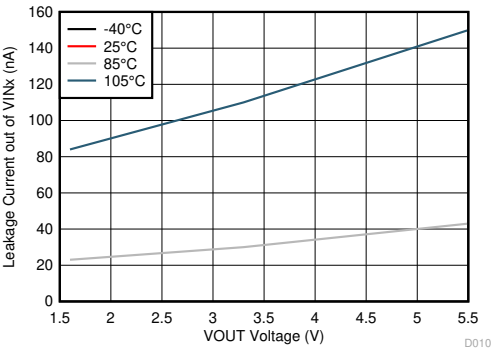

$I_{OUT}$ = 200 mA

**Figure 6-9. Channel 2 On-Resistance vs Input Voltage**




$V_{INx}$ = 0 V $V_{INy}$ = Open

**Figure 6-10. Reverse Leakage Current into VOUT**




$V_{INx}$ = 0 V $V_{INy}$ = Open

**Figure 6-11. Reverse Leakage Current out of VINx**

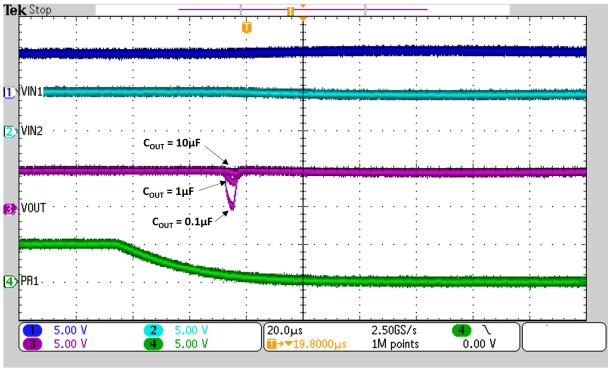



**Figure 6-12. Output Voltage Drop vs Output Capacitance (MODE = 5 V, $R_L$ = 10 Ω)**

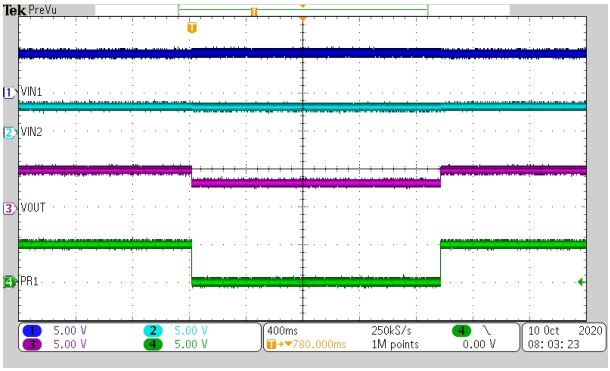



**Figure 6-13. Manual Mode Switchover Behavior (MODE = 5 V, $R_L$ = 10 Ω, CL = 10 uF)**

# 7 Detailed Description

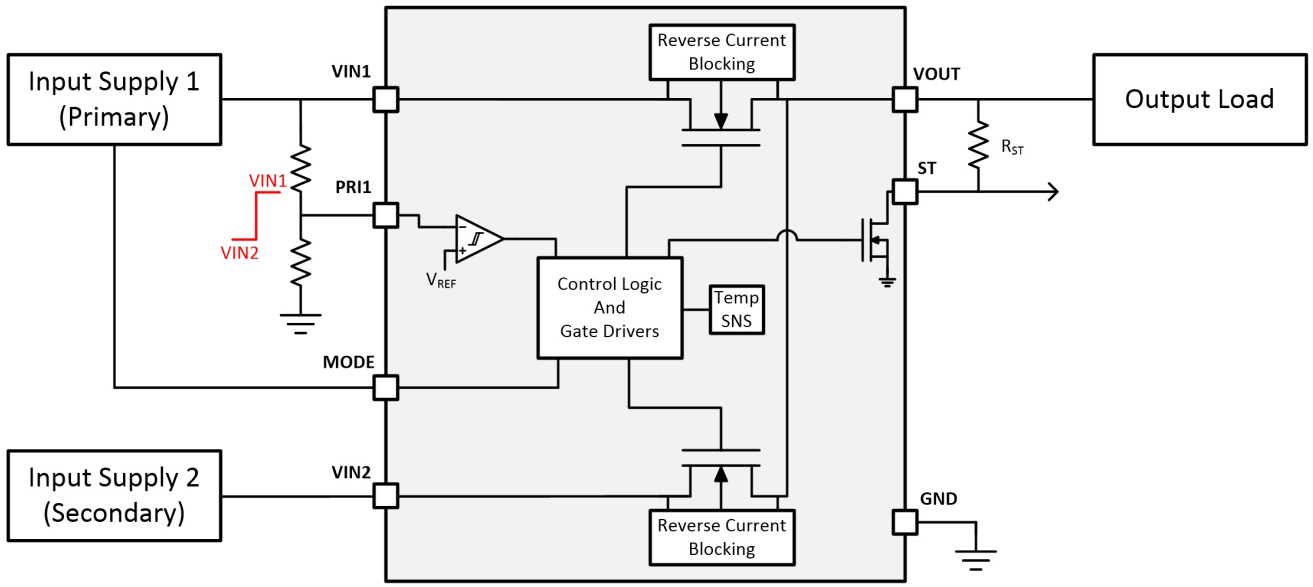
## 7.1 Overview

The TPS2116 is a power mux device with a voltage rating of 1.6 V to 5.5 V and a maximum current rating of 2.5 A. The device uses N-channel MOSFETs to switch between supplies while providing a controlled slew rate when voltage is first applied.

The TPS2116 can be configured for two different switchover behaviors depending on the application. Automatic priority mode prioritizes the supply connected to VIN1 and switches over to the secondary supply (VIN2) when VIN1 drops. Manual mode allows the user to toggle a GPIO or enable signal to switch between channels.

Due to its low quiescent of 1.32 uA (typical) and standby current of 50 nA (typical), the TPS2116 is ideal for systems where a battery is connected to one of the inputs. These low currents extend the life and operation of the battery when in use.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The below sections detail the features of the TPS2116.

### 7.3.1 Truth Table

The below table shows the expected behavior of the TPS2116. For Priority mode, VIN1 is connected to PR1 through a resistor divider.

| MODE | VIN1 | VIN2 | PR1 | ST | VOUT |
|---|---|---|---|---|---|
| VIN1 (Priority mode) | High ($V_{PR1} > V_{REF}$) | X | VIN1 through resistor divider | High | VIN1 |
| | Low ($V_{PR1} < V_{REF}$) | ≥ 1.6 V | | Low | VIN2 |
| External Bias ≥ 1 V (Manual mode) | ≥ 1.6 V | X | High | High | VIN1 |
| | X | ≥ 1.6 V | Low | Low | VIN2 |
| External Bias ≤ 0.35 V (Manual mode) | X | X | High | Low | Hi-Z |
| | > $V_{IN2}$ | X | Low | High | VIN1 |
| | X | > $V_{IN1}$ | Low | Low | VIN2 |

X = do not care

### 7.3.2 Soft Start

When an input voltage is applied to the TPS2116 and the output voltage is lower than 1 V, the output will be brought up with soft start to minimize the inrush current due to output capacitance. However, when the device switches from one power supply to another (switchover) and VOUT > 1 V, soft start is not used to minimize the output voltage drop. For linear soft start behavior, it is recommended to have an output capacitance of at least 0.1 µF.

### 7.3.3 Status Indication

The ST pin is an open drain output that should be pulled up to an external voltage for proper operation. When the TPS2116 is powering the output using VIN1, the ST pin will be pulled high by the external voltage source. Even if the device is blocking reverse current from VOUT to VIN1, selection of VIN1 will keep the ST pin pulled high. When the TPS2116 is powering the output using VIN2 or both channels are disabled, the ST pin will be pulled low. During thermal shutdown, the ST pin will be pulled low regardless of the channel being used.

### 7.3.4 Reverse Current Blocking

The TPS2116 initiates reverse current blocking (RCB) when the VOUT voltage is externally biased and exceeds the input voltage supply being used. Once the output voltage is higher than the input voltage by 42mV ($V_{RCB,R}$), the device will shut off. During this state, the leakage into VOUT and out of VIN is defined by $I_{REV}$. Once the voltage difference between the output and input lowers to 17mV ($V_{RCB,F}$), the channel will turn back on.

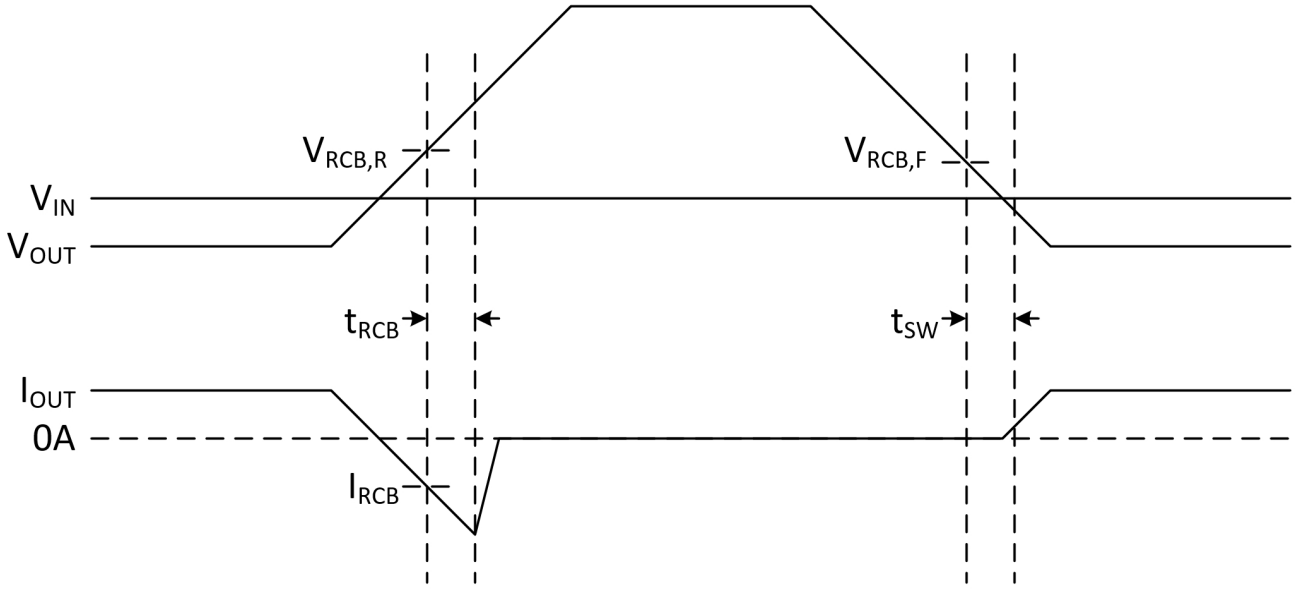



**Figure 7-1. Reverse Current Blocking Behavior**

If RCB is expected to occur, it is recommended to clamp the output or use a high output capacitance (about 100µF). This will prevent voltage spikes from damaging the device due to output inductance.

## 7.4 VINx Collapse Rate

The TPS2116 uses the highest voltage supply to power the device. When one supply drops below the other, the device changes the supply used to power the device. If the supply powering the device drops at a rate faster than 1 V/10 µs, the other supply must be at 2.5 V or higher to prevent the device from resetting. If the other supply is lower than 2.5 V, then the device may not be able to switch to the supply quickly enough, and the device will reset and turn on with soft start timing if VOUT < 1 V.

## 7.5 Output Voltage Drop

The output voltage drop during switchover from one supply to another is based on the load capacitance and load resistance. The stronger the resistive load, the faster the output will discharge. The higher the capacitance on the output, the less the voltage will drop during switchover.

## 7.6 Device Functional Modes

The below sections detail the two different configuraiton options for the device.

### 7.6.1 Priority/Manual Mode

When MODE is tied high, PR1 determines the channel selected. To configure VIN1 as the priority supply, connect MODE to VIN1 and set the proper threshold through a resistor divider from VIN1 to PR1. To configure manual selection, pull up MODE to an external supply and follow the truth table. When PR1 is pulled above $V_{REF}$, the voltage on VIN1 is used to power the output, and when it is pulled below $V_{REF}$, VIN2 is used to power the output. The expected behavior for the device is shown in the waveform below.

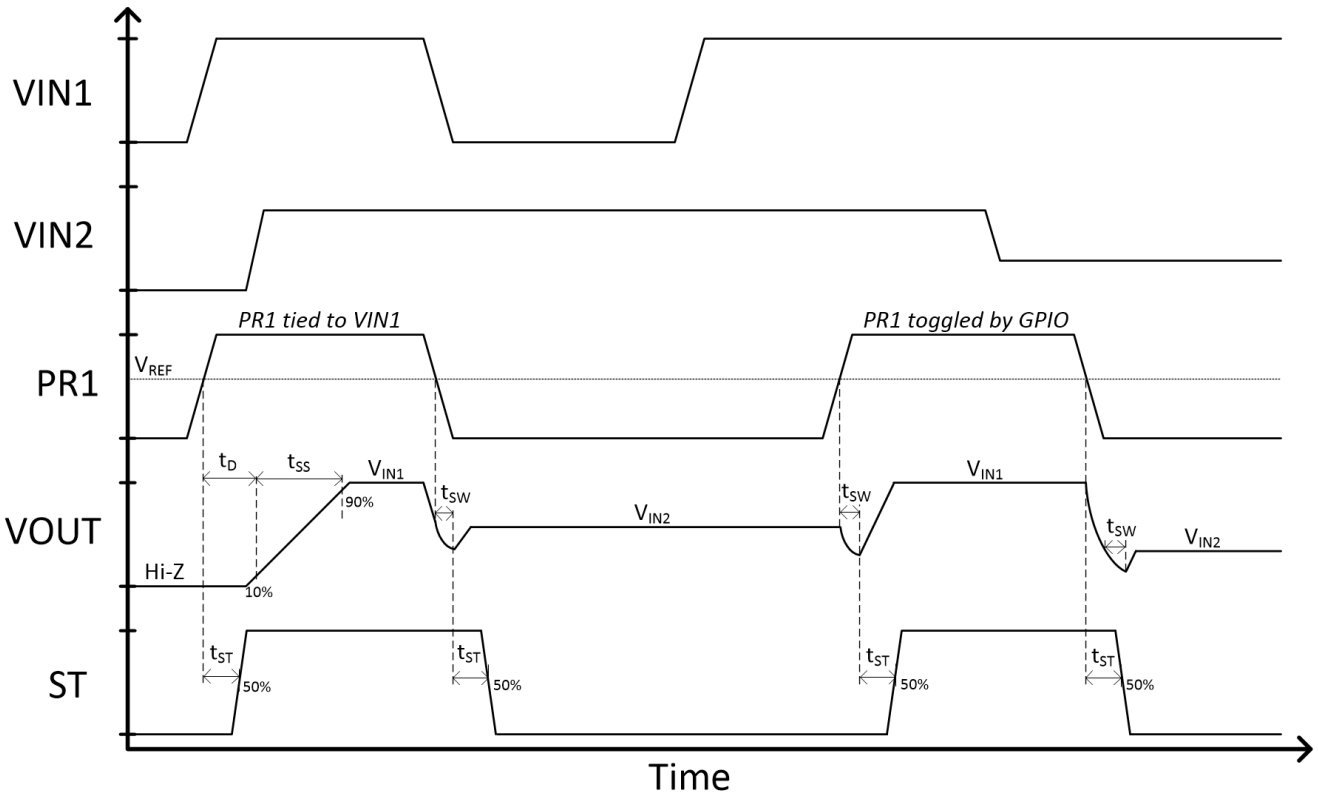



**Figure 7-2. Priority/Manual Mode Switching**

When PR1 is toggled, the device implements a break-before-make switchover which shuts off both channels before turning on the new channel to power the output. This means that for time $t_{SW}$, the output is unpowered and will dip depending on the load current and output capacitance. If the output voltage is greater than the input supply being switched to, then the device will not turn on the new channel until the output has discharged down to $V_{IN}$ + $V_{RCB}$ to prevent reverse current flow.

When MODE is pulled low and PR1 is pulled high, the device enters shutdown. Both channels are turned off and the output is high impedance. When the PR1 pin is pulled low, the higher voltage supply between VIN1 and VIN2 is passed to the output.

#### *7.6.1.1 Priority Switching*

In the case where VIN1 takes priority over VIN2, a resistor divider can be used to set the switchover voltage threshold. When VIN1 is first applied, PR1 is brought high and VOUT is powered by that input. As VIN1 begins

to drop, the voltage on PR1 is lowered until it crosses the $V_{REF}$ threshold. At this point, the device switches over to VIN2.

#### *7.6.1.2 Manual Switching*

For applications where a GPIO pin is used to select which input passes to the output, the GPIO pin can be directly connected to the PR1 pin when MODE is tied high (≥1V). When the GPIO is pulled high, VIN1 is used, and when the GPIO pin is pulled low, VIN2 is used.

Manual mode can also disable both channels by pulling the MODE pin low and keeping PR1 high. In this state, the output of the device is high impedance and the leakage on each input is the shutdown current, $I_{SD,VINx}$.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

## 8.2 Typical Application

This typical application demonstrates how the TPS2116 device can be used to control inrush current for high output capacitances.

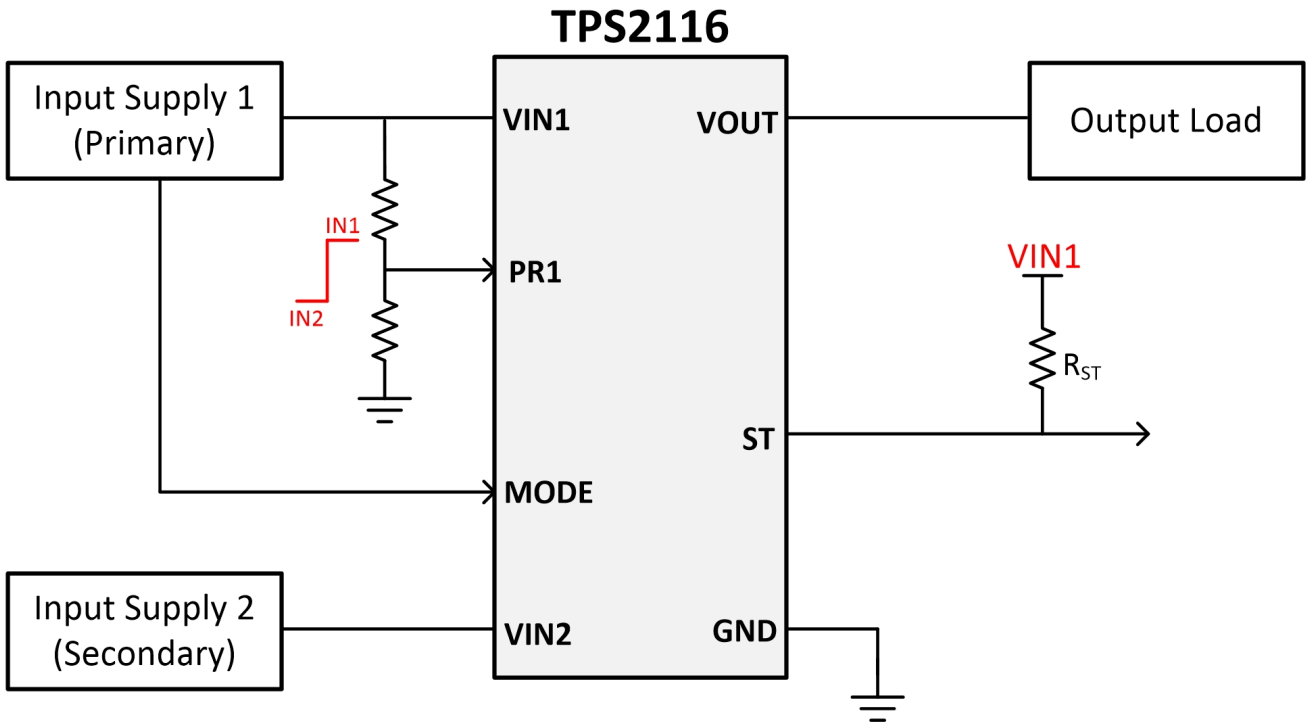



**Figure 8-1. TPS2116 Typical Application Diagram**

### 8.2.1 Design Requirements

For this example, the values below are used as the design parameters.

**Table 8-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| VIN1 Input Voltage | 5 V |
| Mode | Priority |
| Output Capacitance | 100 µF |
| Maximum Inrush Current | 500 mA |

### 8.2.2 Detailed Design Procedure

To determine how much inrush current is caused by the output capacitor, use the equation below.

$$I_{INRUSH} = C_{OUT} \times V_{OUT} / t_{SS} \quad (1)$$

where

- $I_{INRUSH}$ = amount of inrush current caused by $C_{OUT}$
- $C_{OUT}$ = capacitance on VOUT
- $t_{SS}$ = output voltage soft start time
- $V_{OUT}$ = final value of the output voltage

With a final output voltage of 5 V, the expected rise time is 1.7 ms. Using the inrush current equation, the inrush current caused by a 100-µF capacitance would be 294 mA, well below the 500-mA target.

### 8.2.3 Application Curves

The below oscilloscope capture shows 5 V being applied to VIN1. The output comes up with slew rate control and limits the inrush current to below 500 mA.

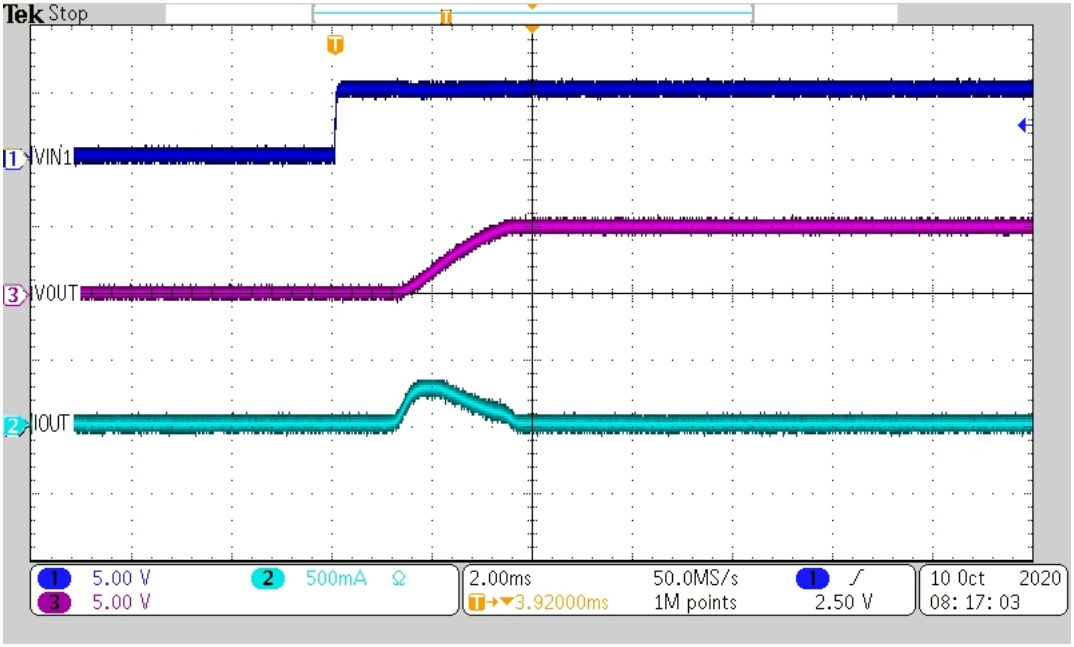



**Figure 8-2. TPS2116 Inrush Current Control**

## 9 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supplies must be well regulated and placed as close to the device terminals as possible. The power supplies must be able to withstand all transient load current steps. In most situations, using an input capacitance ($C_{IN}$) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

# 10 Layout

## 10.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN1, VIN2, VOUT, and GND helps minimize the parasitic electrical effects.

## 10.2 Layout Example

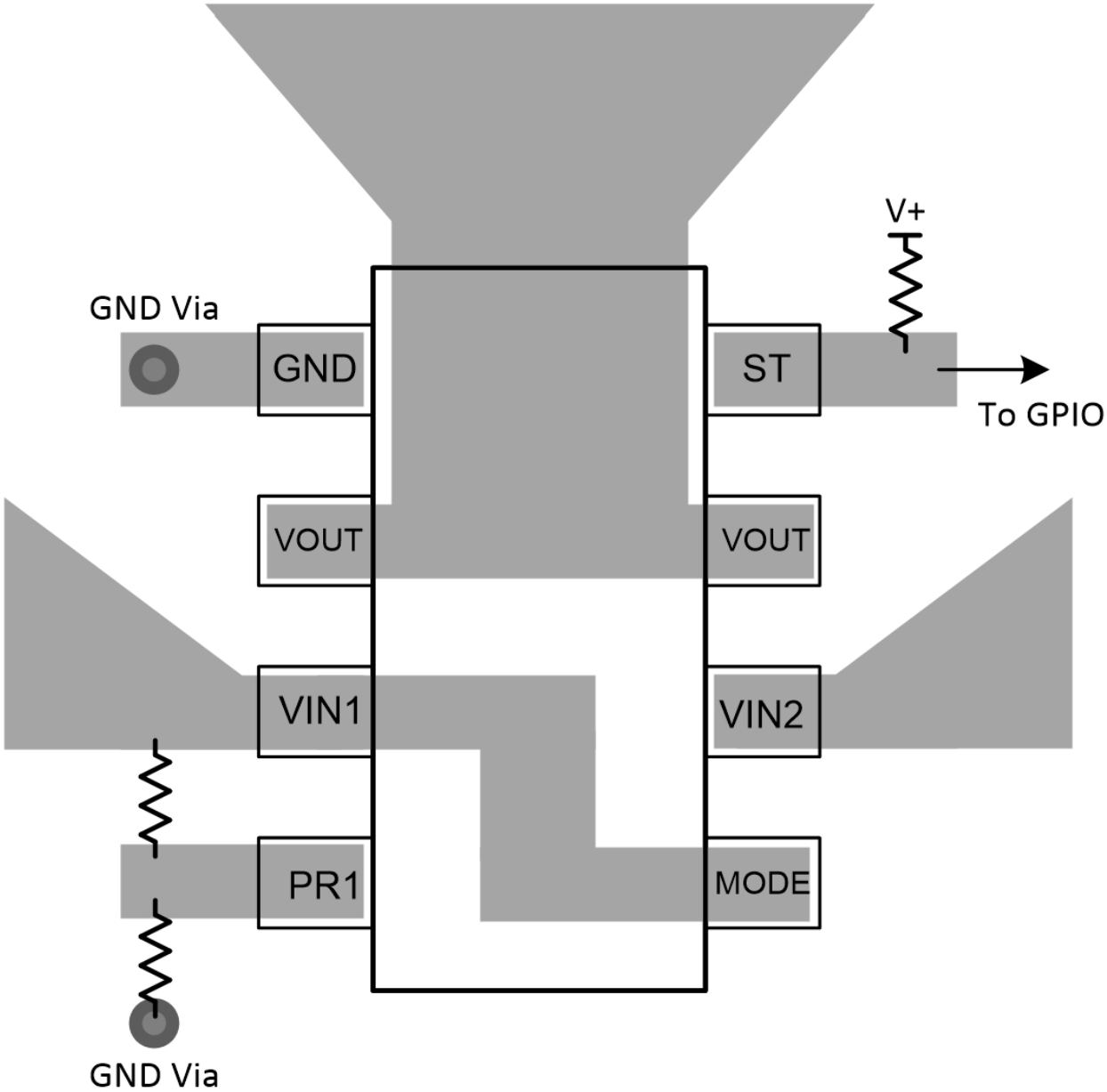



**Figure 10-1. TPS2116 Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- Basics of Power MUX
- 11 Ways to Protect Your Power Path

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Trademarks

All trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2116DRLR | ACTIVE | SOT-5X3 | DRL | 8 | 4000 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 2116 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

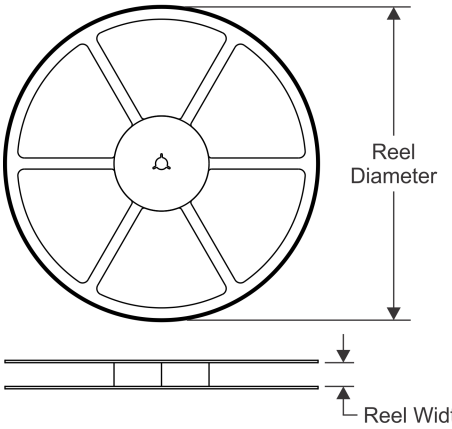
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

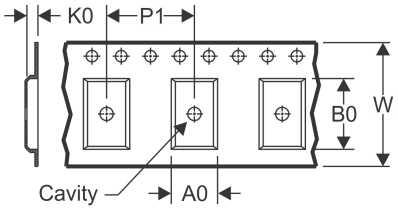
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

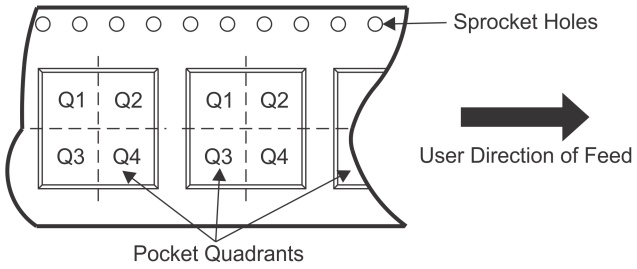



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

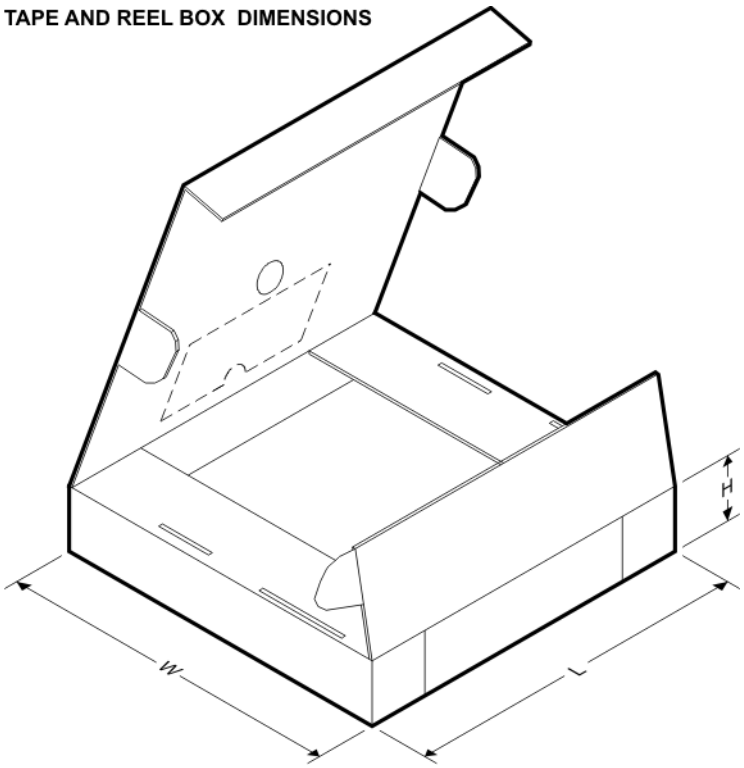
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2116DRLR | SOT-5X3 | DRL | 8 | 4000 | 180.0 | 8.4 | 2.75 | 1.9 | 0.8 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

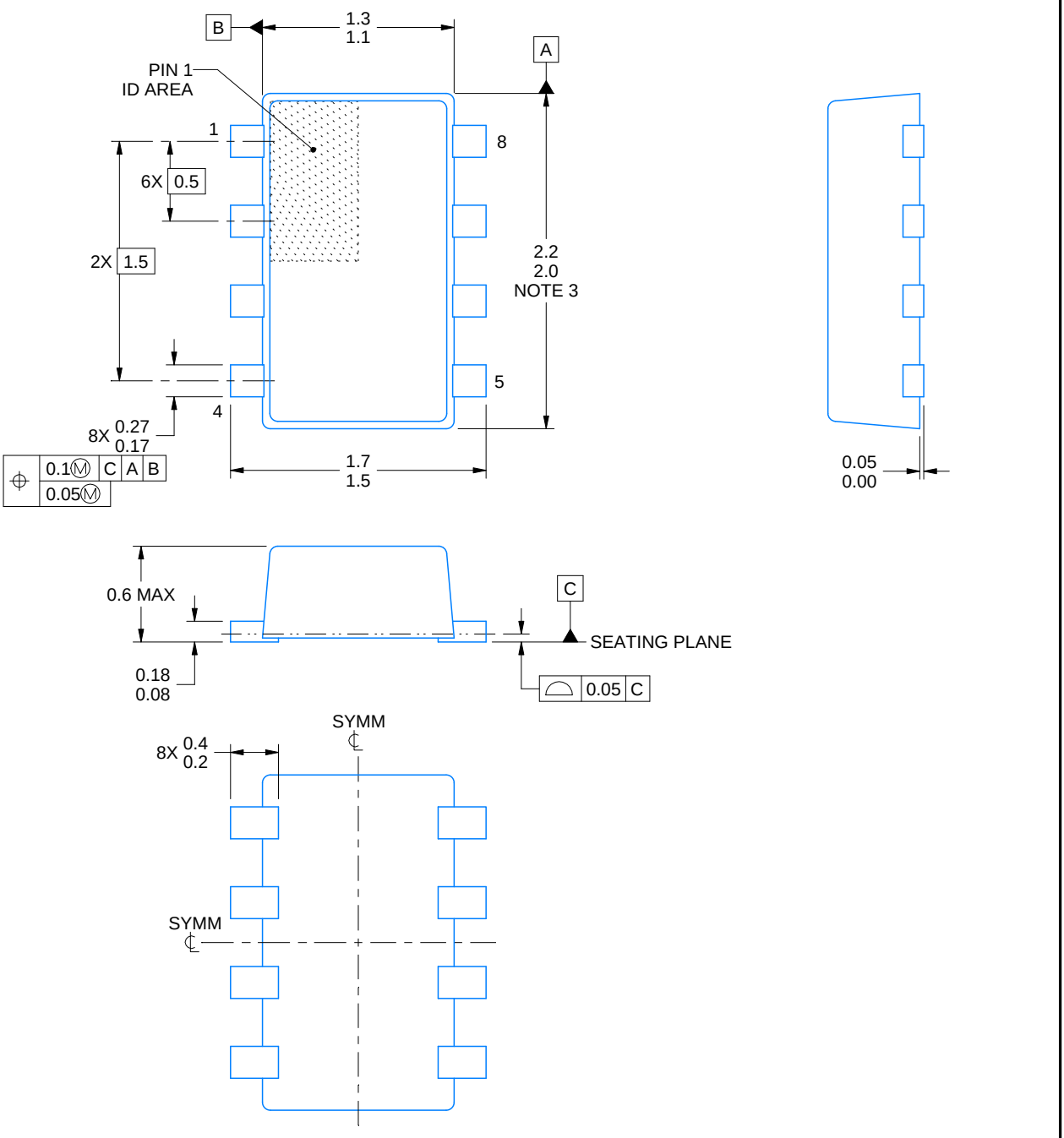
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2116DRLR | SOT-5X3 | DRL | 8 | 4000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DRL0008A

## SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE

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NOTES:

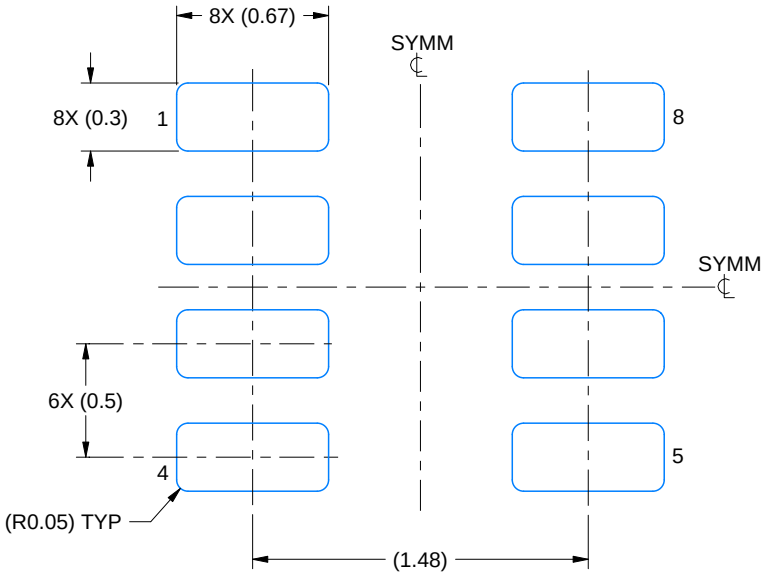
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

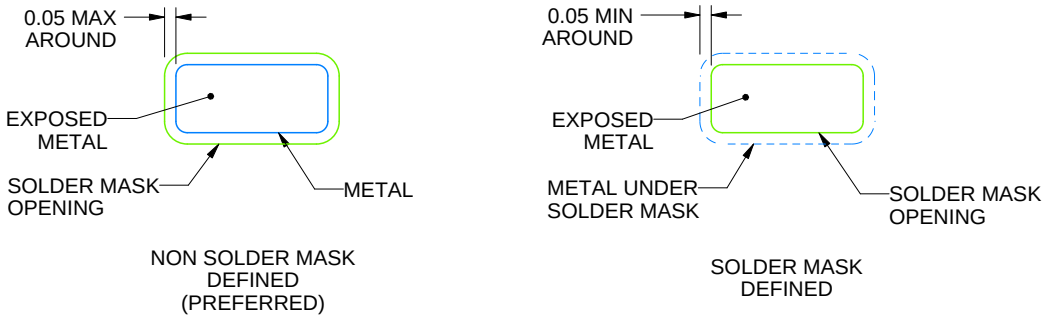
## DRL0008A

## SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X




SOLDERMASK DETAILS

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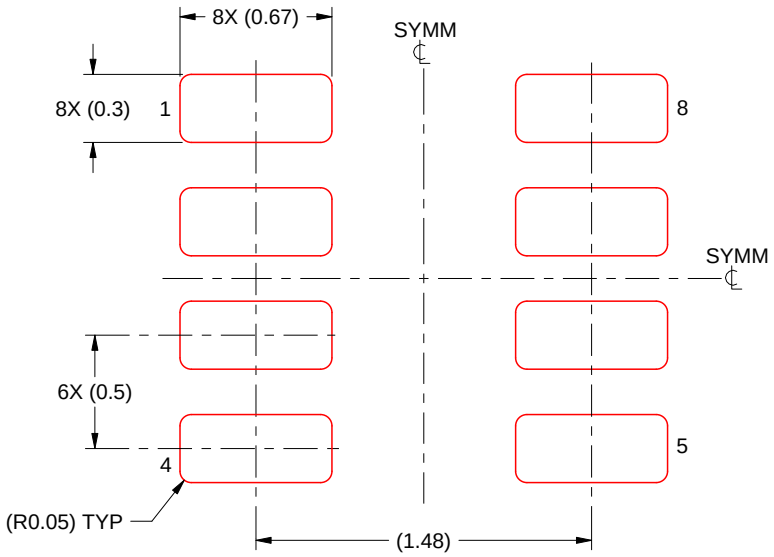
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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