

PCN Number:	20180221002	PCN Date:	February 23, 2018
Title:	Datasheet for ADS131A02, ADS131A04		
Customer Contact:	PCN Manager	Dept:	Quality Services
Proposed 1st Ship Date:	May 23, 2018		
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below.



ADS131A02, ADS131A04

SBAS590D | MARCH 2016 – REVISED JANUARY 2018

Changes from Revision C (November 2016) to Revision D

Page

• Changed document title from <i>2- or 4-Channel, 24-Bit, Simultaneously-Sampling, Delta-Sigma ADC</i> to <i>2- or 4-Channel, 24-Bit, 128-kSPS, Simultaneous-Sampling, Delta-Sigma ADC</i>	1
• Changed V_{AVDD} to AVDD, V_{AVSS} to AVSS, V_{GND} to GND, and V_{IOVDD} to IOVDD throughout document	1
• Changed <i>Features</i> section	1
• Changed <i>Description</i> section	1
• Deleted footnote 2	6
• Changed AVDD, AVSS, VNCP, and XTAL2 pin descriptions and footnote 1 for clarity	6
• Changed <i>CAP to GND Power supply voltage</i> parameter specifications from <i>GND – 0.3 V</i> to <i>0.3 V</i> for the minimum specification and from <i>GND + 2.0 V</i> to <i>2.0 V</i> for the maximum specification	7
• Changed <i>Analog input voltage</i> parameter descriptions from <i>REFEXT</i> to AVDD to <i>REFEXT</i> and from <i>REFN input</i> to AVSS to <i>REFN</i>	7
• Changed <i>Digital input voltage</i> parameter description to include the names of the digital input pins	7
• Deleted CMRR footnote from <i>Recommended Operating Conditions</i> table	8
• Added symbol to <i>Reference input voltage</i> parameter	8
• Changed <i>Offset drift</i> parameter typical specification from $1.2 \mu\text{V}/^\circ\text{C}$ to $2.5 \mu\text{V}/^\circ\text{C}$ and maximum specification from $3 \mu\text{V}/^\circ\text{C}$ to $4 \mu\text{V}/^\circ\text{C}$	9
• Changed <i>Gain drift</i> parameter typical specification from $0.25 \text{ ppm}/^\circ\text{C}$ to $0.5 \text{ ppm}/^\circ\text{C}$	9
• Deleted separate AVDD PSRR specification for the ADS131A02	9

- Changed *Reference buffer offset* parameter typical specification from 170 μV to 250 μV 9
- Changed *Reference buffer offset drift* parameter typical specification from 1.1 $\mu\text{V}/^\circ\text{C}$ to 4 $\mu\text{V}/^\circ\text{C}$ and maximum specification from 4.3 $\mu\text{V}/^\circ\text{C}$ to 7 $\mu\text{V}/^\circ\text{C}$ 9
- Changed *Temperature drift parameter* typical specification from 4 $\text{ppm}/^\circ\text{C}$ to 6 $\text{ppm}/^\circ\text{C}$ 10
- Deleted *VNCP* parameter minimum specification and changed typical specification from -1.95 V to -2 V 10
- Changed *Electrical Characteristics* table so all *Power-Supply* subsections are condensed to one *Power-Supply* subsection 10
- Changed *free-air* to *ambient* in condition statements of *Timing Requirements* tables 12
- Changed location of several interface timing parameters to the *Timing Requirements* and *Switching Characteristics* tables from the *Detailed Description* section 12
- Changed unit from *ns* to t_{CLKIN} in $t_{\text{c(SC)}}$ and $t_{\text{w(SCHL)}}$ rows of *Timing Requirements: Synchronous Master Interface Mode* table 13
- Added *$\overline{\text{DRDY}}$ Synchronization Timing for Synchronous Slave Mode (CLKSRC = 0) to $\overline{\text{RESET}}$ Pin and Command Timing* figures 16
 - Changed *Clock* section for clarification and changed setting of XTAL2 pin 26
 - Changed *Clock Mode Configurations* figure to include load capacitors for clarity 27
 - Changed *Analog Input* section for clarity 28
 - Changed *Equivalent Analog Input Circuitry* figure 28
 - Changed *Input Overrange and Underrange Detection* section for clarity 30
 - Changed location of *Reference* section 30
 - Changed *External Reference Driver* figure 31
 - Changed *Internal Reference* figure 31
 - Changed *Digital Decimation Filter* section for clarity 32
 - Deleted figure and table from *Reset ($\overline{\text{RESET}}$)* section 35
 - Changed *Fixed versus Dynamic-Frame Mode* section for clarity 36
 - Added *Cyclic Redundancy Check (CRC)* section for clarity 39
 - Changed *CRC with CRC_MODE = 0* and *CRC Using the WREGS Command* figures to using red shading instead of //Zero 39
 - Changed *Data Ready ($\overline{\text{DRDY}}$)* section for clarity 43
 - Changed *pull-down* to *pull-up* in bulleted list of *ADC Frame Complete ($\overline{\text{DONE}}$)* section 47
 - Changed description of *UNLOCK from POR or RESET* section 52
 - Changed description of *RREG: Read a Single Register* section 52
 - Changed *number of registers written plus one (n+1) to number of registers written minus one* in *WREGS: Write Multiple Registers* section 54
 - Changed *User Register Description* section for clarity 56
 - Changed *Unused Inputs and Outputs* section for clarity 67
 - Changed title of *Multiple Device Configuration* section and changed description for clarity 68
 - Changed first paragraph of *First Device Configured in Asynchronous Interrupt Mode* to condense data from last three paragraphs into one 68
 - Changed description of *First Device Configured in Synchronous Master Mode* section to condense all paragraphs into one 70
 - Changed description of *All Devices Configured in Synchronous Slave Mode* section to condense all paragraphs into one 72
 - Changed *ADS131A0x Configuration Sequence* figure 79
 - Changed *GND* to *AVSS* in *VNCP* pin description of *Negative Charge Pump* section 80
 - Changed title of *Internal Digital LDO* section 80
 - Changed description of *Power-Supply Sequencing* section 80
 - Changed *Bipolar Analog Power Supply to Unipolar Analog Power Supply with Negative Charge Pump Enabled* figures 81
- Changed first sentence of *Layout Example* section 83
- Changed *ADS131A0x Layout Example* figure to improve layout 83

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS131A02, ADS131A04	SBAS590C	SBAS590D

http://www.ti.com/product/ADS131A02			
Reason for Change:			
To accurately reflect device characteristics.			
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):			
Electrical specification performance changes as indicated above.			
Changes to product identification resulting from this PCN:			
None.			
Product Affected:			
ADS131A02IPBS	ADS131A02IPBSR	ADS131A04IPBS	ADS131A04IPBSR

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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